January 5, 1999

Silicon Subsystem Report

December 1998

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress.

1.1.1 Pixel System

Costs are currently within allocated amounts. However, there continue to be substantial uncertainties in the costs of prototypes of the mechanical support structure - the outer frame and related items. This uncertainty will not be resolved until March 1999 when vendor quotes have been evaluated. Completion of the design of the front-end, rad-hard electronics continues to be delayed. There are minor delays still present in the mechanics (selection of the concept for the prototype disk ring support), in the completion of the design of the 2nd prototype sensors and in the first prototype module design. No additional delays relative to last month are evident.

1.1.2 Silicon Strip System

Costs are within allocated limits. The submission of the 2nd prototype CAFÉ and ABC are delayed about 2-3 months and both have slipped by a few weeks since the last report. However, the submission of the CAFÉ-P is imminent and a date for a FDR of the ABC has been selected. The ABCD FDR was held on schedule and submission on schedule is possible, if technical issues related to performance with detectors attached can be resolved in time.

1.1.3 ReadOut Driver System

Costs are within allocated limits. Development of the implementation model for the preprototype ROD has been performed jointly with the implementation model of the production ROD. Joint development resulted in a delay in the preprototype design, which will in turn result in delay of the first preprototype articles by approximately two months. Because the baseline schedule contained a corresponding amount of float with respect to first use of the preprototypes, the final preprototype units are expected on schedule. This delay was first reported in October 1998 and has not changed.

Highlights of Detailed Reports

1.1.1 Pixel System

Results of the TV-holographic tests of prototype sector #8 from Energy Sciences Laboratory, Inc were documented by Hytec, Inc. The out-of-plane distortions measured after temperature change are within our tolerances, indicating this technique can meet our stiffness criteria.

The Market Survey for the 2nd prototype sensors was initiated.

Work on the DMILL prototype(FE-D) is progressing and there is now confidence that the required circuitry can fit within a 400 micron long pixel and that 20 buffers per column pair can fit as needed. Plans for the first design review of this chip have begun.

A preliminary layout of a revised flex hybrid(version 1.1) was completed and circulated for comment.

High precision X-ray inspection of active IC/detector single-chip assemblies and a 16-chip module were performed. These measurements successfully correlated dead and high-occupancy channels with poor flip-chip assembly. The ability to use high resolution(best is 2 micron precision) X-rays for diagnosis and quality control has been demonstrated.

1.1.2 Silicon Strip System

Two CAFÉ-M ICs were irradiated at PSI with pions and will be shipped to Santa Cruz for measurements in January. These measurements will be used to correlate with 55 MeV proton and Cobalt irradiations. The CAFÉ-P layouts and simulations are almost complete and submission is planned for the first week of January.

All design and layout, except for one block that will be done by automatic place and route has been completed. This was possible, in part, because the LBNL engineer involved spent all of December at RAL. A Final Design Review is planned for about January 20.

The Final Design Review for the ABCD was completed on December 15 with a marathon 9 hour TV session linking CERN, Penn and LBNL. The final simulation and verification steps are on track to be completed by about the end of January(on our schedule). However, tests of the so-called 2nd fab ABCDs(those processed by Temic with improved monitoring) on hybrids with detectors or external capacitative loads attached indicate instability problems that are not understood. A telephone meeting to review data taken at CERN and LBNL was held on December 17 and more work is needed. It is not yet clear if the instability is intrinsic to the design or the result of a hybrid/detector induced problem.

Work is continuing to process kapton hybrids for tests. A possible 2nd ceramic hybrid vendor has been identified and an RFQ requested.

Automatic glue dispensing systems were evaluated. A site visit and demonstration of an upgraded optical metrology tool was held and an RFQ requested to upgrade the existing device at LBNL.

1.1.3 ReadOut Drivers
Requirements and preliminary interface specifications, as well as a conceptual model incorporating all the essential functionality has been completed. Development of an implementation model is now well advanced. The ROD system design is complete except for some of its documentation. Design work presently focuses on optimizing the division of functionality between FPGAs and DSPs in the design. Support is ongoing for Pixel and SCT tests in laboratories and beams.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (D. Bintinger)

Milestones	Baseline	Current	Status
*ID Eng. Review at CERN	20-Oct-98	20-Oct-98	Complete
Select prototype ring concept	1-Nov-98	1-Feb-99	Delayed
Complete fab 1st prototype ring	1-Apr-99	1-Apr-99	On Schedule
Complete fab 1st prototype disk	1-July-99	1-July-99	On Schedule
*Select sector baseline concept	1-Sep-99	1-Sep-99	On Schedule
*Module attachment CDR	1-Sep-99	1-Sep-99	On Schedule
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	On Schedule

LBNL
1.1.1.1.1 Design
Disk layouts for the pixel MCM-D module design were calculated. The MCM-D module is wider than the flex-hybrid pixel module and hence requires a separate disk layout

1.1.1.1.2 Development and Prototypes
Rebuilt test mockups of aluminum tube sector 4 were tested by Hytec, Inc. for distortion due to temperature change with TV Holography. The test mockups were rebuilt with a stiffer core-to-facing adhesive and with a vitreous carbon foam core of twice the density (0.1 g/cc). Preliminary results from the tests indicate that the rebuilt mockups deform less due to temperature change than the original construction technique. The rebuilt mockups deformed by factors of 2 to 8 less per degree centigrade that the originals. Additional mockups will be tested.

Hytec, Inc. delivered a written report on the preliminary results for TV Holography tests of ESLI sector 8. Out-of-plane distortions varied from 0.70 microns per degC to 0.25 microns per degC depending on the temperature of the sector. The power on/power off distortions were approximately 2 microns. These preliminary results indicate that ESLI sector 8 is stiff enough to meet distortion criteria. Future test will include vibration mode analysis.

Tests of adhesive shear moduli were made on 5 module-to-sector structure adhesives.

1.1.1.1.3 Disk Production
No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

Milestones	Baseline	Current	Status
*Start market survey	2-Nov-98	20-Nov-98	Completed
*2nd prototype PDR	1-Dec-98	7-Dec-98	Completed
*Complete market survey	5-Mar-99	5-Mar-99	On schedule
*2nd prototype FDR	29-Mar-99	29-Mar-99	On schedule
*Compl. Test 1st prototypes	13-Apr-99	13-Apr-99	On schedule
*Compl. 2nd prototype design	27-Apr-99	27-Apr-99	On schedule
*Compl. Fab of 2nd prototypes	21-Sep-99	21-Sep-99	On schedule

1.1.1.2.1 Design

No activity.

1.1.1.2.2 Development and Prototypes

The preliminary design review of the Second Prototypes was concluded and the Market Survey was initiated.

Single chip structures and tiles from Prototype Version 1.5 were characterized prior to dicing and then shipped to Bonn for assembly. Both I-V and C-V measurements were taken. The data acquisition test stand was assembled at New Mexico and tested using a laser and a Sr-90 source. Static measurements of annealed irradiated single chip devices from Prototype Version 1.0 were concluded. Measurements were made in the temperature range –6 to –10 degrees Celsius to simulate the response to the ATLAS baseline environment. A summary of the study is in preparation.

1.1.1.2.3 Production

No activity.

1.1.1.3 Pixel Electronics (K. Einsweiler)

Milestones	Baseline	Current	Status
Submit 1st Honeywell SoI test die	15-Nov-98	15-Nov-98	Completed
Submit 2nd Honeywell SoI test die	15-Jan-99		Not known
1st design review of DMILL proto	25-Jan-99	8-Feb-99	Delayed
*FDR DMILL 1st prototype	25-Jan-99	15-Mar-99	Delayed
*Compl. Design DMILL 1st proto.	26-Feb-99	7-Apr-99	Delayed
1st design review of Honey. Proto	1-Jun-99	1-Jun-99	On schedule

*FDR Honeywell SoI 1st prototype	5-Mar-99	15-Jul-99	Delayed
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Sep-99	Delayed
*Compl. Fab of DMILL 1st proto.	23-Jul-99	7-Sep-99	Delayed
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	7-Jan-00	Delayed

The date for submission of a 2nd set of test die to Honeywell is not known at this time. We continue to negotiate with Honeywell for a date for a next multi-project wafer run. The schedule for the first DMILL design review has slipped by two weeks due to both difficulties in organizing the review and some delay in completing the deliverables for this review, particularly the documentation. Submission of the Honeywell rad-hard prototypes is delayed by comparison to our original schedule due to the decision to focus all resources on the DMILL submission first

LBNL

1.1.1.3.1 Design

Our highest priority remains the DMILL front-end chip submission ("FE-D"), but little progress has been made since the relatively tardy November report. At LBNL, time was lost over the holiday period due to licensing problems with our CAD software created by last minute system configuration changes before experts left on holiday. We have evaluated a more complete set of DMILL models (pre-rad, 10 MRad, 25 Mrad, with all speed corners covered for NMOS and PMOS). We find a variation of about 2.5 in speed between the best case pre-rad and the worst case post-rad. These models will provide the basis for analyzing our design margins. We can gain extra "contingency" in speed by slightly increasing the power supply voltages (and total power), so small errors in the corner analysis will not be fatal. The major next step towards completing the digital readout block is to finalize the layout in the region between the matrix and the end-of-column logic (referred to as the bottom of column region). After this, thorough verifications of the block will be carried out both using Verilog (the necessary models have now been tuned against HSPICE) and using full SPICE simulations. We would expect to complete this work by the end of January. During this period we will also perform SPICE simulations on the digital blocks which go in the chip periphery. Many of these blocks were originally designed at LBL, then given to Bonn for implementation in DMILL, and their performance must now be checked with a corner model analysis.

After a working week in Bonn in December 1998, we have demonstrated to our own satisfaction that we can fit the required circuitry into the 400 micron pixel size, and that we can fit 20 buffers per column pair into the chip periphery, in the DMILL process. The designs are less robust than those of FE-B, and careful analysis will be required to establish that their performance is acceptable. Nevertheless, we are now quite confident that we can implement almost all of the desired functions into FE-D.

1.1.1.3.2 Development and Prototypes

No significant new lab work has been carried out since the November report. However, after study of a number of working pixel devices with a high resolution X-ray scanner, numerous examples of bump-bonding failures have been found. These failures correlated very well with the observed problems in the assemblies. Simple examples include "bridged" bumps that short two adjacent channels, often leading to one channel which is dead and one which counts double when illuminated with a photon source. More complex examples include the large regions of dead channels seen on the modules. The first Tile2 module was X-ray scanned, and several particularly bad regions showed large areas with completely merged bumps. Note with the DC-coupled preamplifier design used in our front-end chips, connecting two inputs together typically leads to an unstable situation where the two channels fight each other, and one is stuck on while the other is stuck off, and neither is sensitive to external charge injection. It is apparent that the Indium bumping from Boeing was particularly marginal in this respect, with regions where an individual flip-chip placement resulted in too much "squeezing" of the bumps in one corner of an electronics die and too little in an opposite corner. Whether this is due to poor planarization during flip-chipping or to irregular bump heights is not yet clear. In addition, several prototypes fabricated with CVD diamond sensors showed particularly severe problems due apparently to the non-uniform diamond thickness (perhaps as much as 10 micron variations in thickness over the centimeter square area of the detector), indicating the critical need for uniformity in flip-chipped assemblies. These observations almost certainly eliminate the need for theories that the large dead regions observed in the modules were due to electronics failure, either from electrostatic discharge or from large forces generated during flip-chipping which might damage the electronics die itself.

Finally, we have just received the eight loaded PLL boards (the LBL/Wisconsin-designed VME board used for all lab test work) which we expected before Christmas. They are now being inspected, and testing and burn-in will be carried out during January to allow us to ship the completed boards out by the end of January. These additional boards should satisfy the remaining test needs for all of the active institutes in the pixel collaboration.

1.1.1.3.3 Production
No activity.

1.1.1.4 Pixel Hybrids (R. Boyd))

Milestones	Baseline	Current	Status
*Compl. Assembly of 1st proto.	14-Jan-99	10-Nov-98	Complete
*1st prototype design review	18-Feb-99	18-Feb-99	On schedule
*Compl. Tests of 1st protos.	15-Apr-99	15-Apr-99	On schedule
*Select hybrid type	15-Apr-99	1-Mar-99	Ahead
*2nd proto design review	28-Apr-99	28-Apr-99	On schedule
*Compl. 2nd proto design	25-May-99	25-May-99	On schedule

Oklahoma
1.1.1.4.1 Design

A footprint sketch for the version 1.1 prototypes has been completed for review and comment by LBNL and Genova. This version corrects some (nonfatal) omissions from the first version and implements several improvements by taking advantage of all the substrate area for routing.

1.1.1.4.2 Development
Activity is reported in 1.1.1.5

1.1.1.4.3 Production
No activity.

1.1.1.5 Pixel Modules (R. Boyd, K. Einsweiler, M. Gilchriese)

Milestones	Baseline	Current	Status
*Compl. 1st proto. Design	29-Oct-98	30-Jan-99	Delayed
*1st proto. Design review	18-Feb-99	18-Feb-99	On schedule
*Compl. Tests of 1st protos.	18-Mar-99	18-Mar-99	On schedule
*Select module type	18-Mar-99	1-Mar-99	Ahead
*2nd proto. Design review	17-Sep-99	17-Sep-99	On schedule

1.1.1.5.1 Design/Engineering.

Oklahoma
Steve Timm and Saj Alam of SUNY, Albany traveled to Oklahoma for on site training in the setup and use of the pixel module test system. It is anticipated that they will be receiving a test system by the end of January.

1.1.1.5.2 Development and Prototypes

LBNL
Last month it was reported that X-ray inspection of flip chip assemblies had been implemented successfully at a company(X-Tek) in Santa Clara. The ultimate resolution of the X-ray system from this vendor can be as good as about 2 microns, if the sample can be brought very close to the X-ray source(less than 1 mm). Defects in bump deposition(missing bumps) and in flip-chip assembly(bridged bumps) were easily observed on dummy mechanical modules.

In December, active devices were X-rayed. These included single chip/detector assemblies mounted on PC cards, one 16-chip module mounted on an aluminum heat spreader and two diamond single chip assemblies. Neighboring channels in the single chip assemblies had been observed to have one dead channel and one channel with twice the occupancy(in photon source tests). The X-ray scans confirmed in all of these cases that the cause was bridging between neighboring bumps. This was observed in both solder bumps and indium bumps. The 16-chip module had about 50% of the chips with significant dead regions. Although the resolution is just adequate in the presence of the 1/8 inch aluminum plate, it was confirmed that these regions were correlated with areas of merged or bridged

bumps(indium bumps). From these first studies, it's clear that X-ray inspection with this firm can be a powerful diagnostic and QA tool. A blanket order is in place with X-Tek.

Oklahoma
Although internal charge injection is working on the single chip modules, we are still experiencing difficulty with the flex hybrid module. We are in the process of identifying the cause. We have also begun the process of finding a solution to the "high current" problem mentioned in previous reports.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

Milestones	Baseline	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	Done
*FDR for 2nd ABC	23-Oct-98	19-Jan-99	Delayed
*Closing date for market survey	26-Oct-98	25-Sep-98	Done
*Submit 2nd CAFÉ-M	30-Oct-98	11-Jan-99	Delayed
*Issue call for tender	9-Nov-98	9-Nov-98	Done
*Submit 2nd ABC	16-Nov-98	31-Jan-99	Delayed
*FDR for 2nd ABCD	11-Dec-98	15-Dec-99	Done
*Closing date for tender	21-Dec-98	22-Jan-99	Delayed
*Submit 2ns ABCD	27-Jan-99	27-Jan-99	On Schedule
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	On Schedule
*Frame contract in place	15-Apr-99	15-Apr-99	On Schedule
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	7-May-99	Delayed
*Compl. Fab of 2nd ABC	19-Apr-99	18-Jun-99	Delayed
*Test systems complete	26-Apr-99	26-Apr-99	OnSchedule
*1st ICs avail. For 2nd proto hybrid	18-May-99	11-Jul-99	Delayed
*Compl. Fab of 2nd ABCD	30-Jun-99	11-Jun-99	OnSchedule

1.1.2.1.1 Design/Engineering

LBNL & UCSC

Two CAFE-M ICs were irradiated at the PSI facility in Switzerland just before the holiday break. This is to compare the resistor changes from these minimum ionizing particles with the proton and Co data we have taken earlier and hopefully sort out what is the correct

expected change at LHC. We will get the parts back at UCSC to measure early in January. As stated in the November report, we are proceeding to finish the CAFE-P for submission assuming the worst case Co data. Some changes have been made to use extrinsic-base resistors which do not suffer change from radiation in certain parts of the design where their larger size and, therefore, larger capacitance do not affect the performance of the circuit. This will partially mitigate the larger changes we measured with Co irradiations. At month end, the design was complete and the final verifications well underway. We decided not to rush the submission before year-end but rather wait for a final review of verification data the first week in January. Submission is expected within a week of returning from holiday break.

Work on the ABC design proceeded at RAL with Gerrit Meddeler in temporary residence there. At the holiday break, all design and layout but the final "auto place and route" of one logic block had been completed and all blocks but that one had been placed into the chip floor plan. Interconnects between the blocks were also nearly complete. Top level simulations were started at the schematic level. The remaining verification steps will be completed in January. We are trying to schedule the Final Design Review for 19-Jan. Brig Williams is attempting to locate outside reviewers for that date.

The Final Design Review for the ABCD was conducted on 15-Dec. It was well done and generally successful. The remaining verification steps will be completed in the first few weeks of January with submission likely by the end of January. A few days before the review, a problem surfaced in testing existing ABCDs with detectors. See discussion below. This may delay submission if the problem cannot be resolved soon.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

Testing of ABCDs from the second fabrication (original design) has continued. It has been found that the chips perform must better when the backside of the wafers are metalized before the chips are diced. Several chips working on a hybrid at LBNL and at CERN were found to work stably. The issue of large channel-to-channel variations remains and must be addressed in the new design. Some of these chips were irradiated with protons and x-rays. The chips continue of function after irradiation but some of the digital functions slow sufficiently such that they no longer work at the required 40 MHz. This also is being addressed in the re-design.

The ABCD hybrids were then bonded to detectors. The chips then showed problems of oscillation or instability. There is some evidence that altering the detector bias circuit on the hybrid improves this. However, the work at LBNL shows that connecting single capacitors to the ABCD inputs provokes the oscillations. The data was reviewed in a phone meeting on 17-Dec just prior to the holiday break. The cause was certainly not understood and several possible explanations were proposed. More work is planned. We must determine if this is a hybrid/detector induced problem which can be fixed external to the ABCD or if some element of the ABCD design can be changed to solve the problem.

1.1.2.1.3 Production

No activity.

1.1.2.2 Silicon Strip Hybrids(C. Haber)

Milestones	Baseline	Current	Status
Complete design of 1st prototype	17-Nov-97	17-Nov-97	Complete
Complete fab of 1st prototype	2-Feb-98	23-Mar-98	Complete
Preliminary design review	3-Aug-98	10-Jan-99	Delayed
*Compl. 2nd proto subs. design	29-Oct-98	1-Jan-99	Delayed
*Compl. 2nd proto cable design	29-Oct-98	1-Jan-99	Delayed
*Compl. 2nd proto fanout design	29-Oct-98	1-Jan-99	Delayed
*Compl fab of 2nd proto substrate	11-Mar-99	1-Jun-99	Delayed
*Compl fab of 2nd proto cable	11-Mar-99	1-Jun-99	Delayed
*Compl fab of 2nd proto fanout	11-Mar-99	1-Jun-99	Delayed
*Compl procure of 2nd proto comps	11-Mar-99	1-Jun-99	Delayed
*Compl. 2nd proto assembly	17-May-99	1-Jul-99	Delayed
*1st 2nd proto hybrids available	14-Jun-99	10-Jul-99	Delayed

LBNL

1.1.2.2.1 Design

No activity.

1.1.2.2.2 Development and Prototypes
An attempt was made to mount the kapton hybrid on a ceramic substrate. It was however damaged in the lamination process. A new, more gentle process, was suggested and was tested in Nov. It was seen to result in a non-uniform surface structure on test samples. The process was improved and the lamination of a second hybrid occurred this month.

A second possible vendor for hybrid production was identified. A documentation packet and RFQ were sent to the vendor. A quote was prepared by them but not received yet due to the holiday period.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

Milestones	Baseline	Current	Status
*Preliminary design review	3-Aug-98	1-Apr-99	Delayed
Complete fabrication			

of 1st dummy modules	15-Aug-98	15-Aug-98	Complete
Prototype tooling complete	1-Apr-99	1-Apr-99	On schedule
*Compl. Design of proto assy/test	14-Jun-99	14-Jun-99	On schedule
*Compl. Fab of tooling for proto	14-Jun-99	14-Jun-99	On schedule

LBNL

1.1.2.3.1 Design of Assembly and Test

A new version of the assembly software from Manchester is available and we are still studying the documentation.

1.1.2.3.2 Development and prototypes

Design of a new calibration plate continued with the idea of using precision dicing to eliminate the use of the calibration bar. Discussions were held with a photo-mask vendor concerning the production of this plate. Additional comments were received at the SCT meeting at CERN. These have been added to the design and it was posted on the web for further review and comments from the SCT community in Nov. No further comments were received so we plan to move to fabrication.

Results on module metrology at the Rutherford Lab were received in October and studied. Transverse precision was similar to ours but module thickness variation was outside specifications. Following the discussion in the SCT meeting we undertook a systematic study of the assembly fixtures to try and understand where these non-uniformities might be coming from. They don't appear to originate from the shape of the assembly fixtures.

We have obtained thin electron-microscope "targets" which were suggested as a tool for use in measuring surface shape. We are studying these.

A visit from the Smart Scope representative occurred and the new software was evaluated.

A literature survey and some vendor discussions concerning automated dispensing systems were undertaken in Nov. We visited the Asymtek representative and looked at their benchtop system.

Design continued on a folding fixture for the hybrids.

1.1.2.3.3 Production

No activity.

1.1.3 ReadOut Drivers(A. Lankford/R. Jared)

Milestones	Baseline	Current	Status
*Select PreROD implementation	30-Oct-98	4-Nov-98	Complete

*Requirements review	30-Nov-98	18-Nov-98	Complete
*Compl. System design	28-Dec-98	28-Dec-98	Complete
*System design review	11-Jan-99	11-Jan-99	On schedule
*Compl. PreROD design	29-Jan-99	31-Mar-99	Delayed
*Compl. PreROD layout	15-Feb-99	15-Apr-99	Delayed
*Compl. PreROD procure	1-Mar-99	30-Apr-99	Delayed
*Compl. PreROD PCB fab	16-Mar-99	16-May-99	Delayed
*Compl. PreROD 1st assemble	30-Mar-99	31-May-99	Delayed
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	On schedule
*Compl. Test stand essential mod.	12-May-99	12-May-99	On schedule
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	On schedule
*Compl. PreROD assembly	9-Jul-99	15-Jul-99	Delayed
*PreRODs complete	20-Aug-99	20-Aug-99	On schedule
*Test stand design review	21-Sep-99	21-Sep-99	On schedule
*Compl. Design of test stand	28-Sep-99	28-Sep-99	On schedule
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	On schedule
*ROD Common design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD strip design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD pixel design PDR	1-Oct-99	1-Oct-99	On schedule

1.1.3.1.1 Strip Test Beam Support

UC Irvine

Technical support was provided to U.K. groups at Rutherford Lab and at UCL who are incorporating external triggers into their DSP-based readout systems.

1.1.3.1.2 Pixel Test Beam Support

University of Wisconsin

The fabrication of the 8 PLL cards is completed. They will be debugged in January.

1.1.3.2.1 ROD Requirements

UC Irvine and University of Wisconsin

Definition of ROD requirements is largely complete. Although no new requirements were defined in December, the latency for delivery of *L1Accept* signals through the ROD was discussed. Estimates of the overall level 1 latency through the SCT system compiled at UCL yielded a result that does not quite fit within the limits allowed by the level 1 latency buffers on the ABC/D chips. Consequently, budgets for individual contributions to the overall latency, including the ROD latency, are now being considered.

1.1.3.2.2 ROD Essential Model

UC Irvine and University of Wisconsin

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No significant refinements of the essential model were made during December.

1.1.3.2.3 ROD Implementation Model

ROD design effort continued to focus on a combined FPGA/DSP implementation in order to combine the best features of the FPGA-based and DSP-based approaches studied previously. The decoder section of the favored hybrid approach utilizes both an FPGA and a DSP. Progress on understanding optimum division of functionality between decoder FPGA and decoder DSP continued. This work focuses on details of buffering and data transfer between the FPGA at the input and the DSP that follows. The implementation model is now complete at the level of the ROD system design. Completion of implementation model documentation remains. Ongoing detailed design work will validate the implementation model.

UC Irvine

The primary focus of activity at UCI in December was exploring the implications of various schemes for FPGA decoding and data transfer on the decoder DSP in the combined FPGA/DSP decoder section. The central issue is how to decode and transfer in a manner that reduces related tasks in the DSP, in order to make available more DSP processing power for other tasks.

Host DSP issues were further evaluated, and development of software to simulate DSP host software continued. The simulation software models the various tasks of the host DSP without directly interfacing to the decoder DSPs.

Documentation of the old primarily DSP-based implementation was updated and placed on the web at http://positron.ps.uci.edu/~pier/ROD/-UCI_ROD_Guide.html.

University of Wisconsin

The primary focus of the activity at Wisconsin in December was to investigate the impact of various formats of data communication between the FPGA front end and the DSP event builder. To this aim a C simulation of this architecture was written, debugged and studies were performed. The principal problem was to minimize the impact of data transfer on DSP processing. A scheme of data alignment by zero padding of the data was studied. Work continued on the FPGA VHDL code. This effort was aimed at completing the model for 96 channels. Test gather code was also written to complete the

simulation. The event generator was upgraded to include the effects of jets and other correlations.

1.1.3.3.7 Preprototype ROD

UC Irvine and University of Wisconsin

The implementation model for the preprototype ROD is being developed in tandem with the model for the production ROD. Progress on the implementation model is discussed above under WBS 1.1.3.2.3. A modular implementation was suggested for the preprototype ROD in order to facilitate its development. (See http://positron.ps.uci.edu/~pier/ROD/pdf/ModularROD990.pdf)