Pixel Electronics Manpower Estimates

Manpower estimates for remainder of FY02 to FY04

- IC Design for FE-I2, FE-I3 chips
- Board design for test system

Perform bottoms-up estimate based on detailed task lists

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On-detector Electronics Deliverables:

US Responsibilities include:

- FE chip design, testing and production (LBL): Contribute roughly 20% towards the common procurement of the series production. Test roughly 50% of FE ICs.
- Opto-link chip design, testing and production (OSU): Contribute approximately 50% towards the common procurement of the series production.
- Design and provide hardware/software for lab/testbeam single chip and module testing, production FE wafer probing, production module testing/burn-in (LBL).

LBL engineering personnel estimate:

Person	Remaining in FY02	Months in FY03	Months in FY04
Laurent B	5	12	12
Peter D	0.5	1	1
Emanuele M	2	2	2
Gerrit M	1	3	2
Ivan P (Guest Engineer)	2	0	0
Bryan H	1	1	1
John J	2	1	1
Chinh V	1	2	1
Engineer Total	14.5	22	20
George Z	1	2	2
Helen C	0.5	1	1
Technician Total	1.5	3	3

- IC tasks include FE-I2, and FE-I3 (production chip). Continuing manpower is concentrated on front-end issues, assuming that other parts of the design are basically very close to production quality.
- Board tasks include completion of TPLL/PICT/TPCC plus SimpleBOC in FY02, and completion of production burn-in system in FY03.
- Continue to assume that all chip testing and most board testing is performed by physicists, with use of engineering manpower only has needed for technical problems.

Detailed breakdown of tasks for FE-I2

Specific front-end work:

- Front-end work includes characterization of FE-I1 Analog Test Chip, plus design of next generation Analog Test Chip for submission to TSMC. Work on present front-end design needs information from single-chip and full-module assemblies, as well as from irradiated assemblies. Any major surprises in these areas will delay the test chip schedule, and most likely the FE-I2 run.
- This effort is expected to lead to a new Analog Test Chip submission to MOSIS in a May-July 02 timescale (typical cost for our test chip in 0.25μ is about 15K$).
- This work also includes some R&D for the longer term, as zero-crossing design is likely to be too aggressive for FE-I2.

Problem list:

- Modify IF mirrors to increase current by about a factor 2 (Ivan/Laurent).
- Modify mirror sizing for VCal I to V conversion to eliminate non-linearity (Ivan/Laurent).
- Improve diode design for overvoltage blocks to achieve correct thresholds. Also optimize resistor layout for electromigration and turn-on slope. Slope should be steeper for shunt regulator (Ivan/Peter).

- Modify Linear Regulator band-gap reference to achieve output voltage of 1.60-1.65V (Laurent).
- Improve sizing of compensation transistors in pixel calibration chopper circuit to reduce wrong-sign pulse observed for small VStep. Presumably this will also improve the offset observed between internal and external injection (Ivan/ Laurent).
- Pixel control design with mixed VDD/VDDA logic shows many power sequencing problems. Consider improved design in which control is essentially all VDD, with proper interfaces to VDDA when needed. Also re-examine readback design and consider an SEU-latch reset for pixel configuration latches. Concern is that improvements in this area could require considerable layout work (Peter/Ivan/ Laurent).
- Re-examine buffering and distribution of control signals. In particular, should signals like Shift be buffered per column pair ? Also re-size traces like DigitalStrobe and Strobe to reduce present top-bottom skew of about 4ns. Further systematic characterization of assemblies is required first (Laurent).
- Fix RCU bug with early generation of Empty by adding XCK-clocked DFF to delay Empty by 25ns (Gerrit).
- Re-examine timing of Pixel Register, where 2-phase non-overlapping clock is generated with the wrong phase. Looks like the PixClk state machine should run on CCKbar instead of CCK, and then the phase will be correct (Gerrit).

- Study how to improve sense amp and column pair design to increase the operating margin when the CEU clock is operated at the maximum frequency of 40MHz. Also examine TOT processor timing for this case in more detail to make sure the issues are really in the sense amps (Emanuele).
- Improve threshold control, and in particular the design of the TDACs. Present design shows significant non-uniformity (threshold with TDACs on is systematically lower at small row number), most likely related to ITrimTh distribution problem. Possibly use “bipolar” TDAC which tunes both ITH1 and ITH2. In any case, make TDACs more uniform and monotonic (Ivan/Laurent/Peter).
- Examine optimization of the LVDS receiver current versus speed tradeoff. Present receiver uses about 1mA of standing current, which is somewhat high (Laurent).
- Examine possible mods to the present front-end design in order to considerably reduce the threshold dispersion. Possibilities include still higher gain, improved second stage design, and AC-coupling of preamp and second stage. This work requires understanding of whether timewalk and series/parallel noise in complete assemblies are significant problems as well (Laurent, Kevin).
- Turning off the CEU clock still produces data in the given column pair, and it can also cause increased, rather than reduced, current consumption (Emanuele).
- Improve DOMUX diagnostic output, possibly including PixClk1 and PixClk2 (Gerrit, Kevin).

Schedule and Manpower:

- Key question is when does work on FE-I2 start seriously ? Testbeam and irradiation work should be largely complete by the time of the CPPM meeting. Plan to have a first discussion on schedules and workplan at that meeting. Critical path will then be FE Analog Test Chip, but its role in the FE-I2 design is not yet completely clear. If submitted in May, results would be available by early Sept. If submitted in July, the results would arrive very late for FE-I2.
- Laurent is already working, Ivan would probably start in July. Emanuele could start in August, and Gerrit in Sept. This would lead us to an FDR before the Oct pixel week, and then to an engineering run submission about Nov 1.
- The major uncertainty on this schedule is how long it will take to reach some resolution of our problems with yield for chips in the FE-I1 run.
- Hope to bring Ivan back to LBL for 1-2 months. Assume at most 3 months of Emanuele (including additional work on high-level timing simulations) and 2 months of Gerrit are required for FE-I2. Expect that Gerrit would once again assemble the reticle and do all final verifications (DRC and LVS).
- Expect upgrades to MCC-I as well, for example to implement SEU-tolerant configuration registers. In that case the engineering run would most likely contain 2 FE chips and one MCC chip. Opto-chips and others could also be included, depending on how ongoing development work has progressed. Once MCC is included, there is significant additional space in the reticle for other chips.

FE-I3 and beyond estimates:

- For FE-I3, assume further 1 month of Emanuele and 2 months of Gerrit. Depending on the remaining issue list, this may be somewhat conservative. Assume that all of this work will have been completed in FY03. If an FE-I2 run takes place in Nov 02, and no major issues arise from the FE-I2 design, this should be realistic. This model assumes that FE-I3 is a 400μ geometry pixel chip, similar to FE-I1, and it is used to instrument the complete initial pixel detector. Smaller pixels would be an upgrade path (see below).
- Work in FY04 is a combination of limited work in support of production ("documentation and maintenance") plus work in support of on-going R&D effort in smaller feature size processes and higher performance pixel arrays. We expect to begin having access to 0.13μ generation CMOS in FY03 already, but we would not immediately ramp up an effort to use this technology generation until the FE-I3 production was launched.
- The upgrade R&D effort as presently imagined would be entirely IC design, and includes process evaluation and front-end studies (Laurent), standard cell development and design kit issues (Gerrit), and readout optimization studies (Emanuele).
- Depending on personnel availability and funding, the latter two topics could be handled by one engineer. The R&D work would not lead to any significant submissions (beyond test chips) until at least FY05.

Detailed Task List for Board-level Work

TPLL VHDL Work (John):

- Implement DTO/DTO2 and 40/80Mbit/s decoding algorithms.
- Implement support of self-trigger operation.
- Implement support of Hitbus-based threshold scans of single pixels.
- Implement improved self-test features.

TPLL Hardware (John):

- Commission remaining 5 boards from initial production of 7.
- Load and commission remaining boards (15 more boards for a total of 22 ?)

Simple BOC (Sriram and John):

- Detailed proposal made, including block diagram and all parts specified.
- Schematic in progress, expect layout and boards to be ready during June.
- Sriram is doing most of the work, so cost should be low.

PICT Work (Chinh):

- Still have not finished commissioning the pin driver portion of the board.
- Then need to commission remaining 2 loaded boards, gain more experience, and then complete the production quantity of boards (roughly 6 total ?)

TPCC Work (Chinh):

- Complete VHDL and commission first 3 cards.
- After initial evaluation of 3 cards, proceed with any minor modifications before production, order production parts, fabricate and load boards, and commission and deliver them.

Burn-in System (Chinh):

- Presently not well-defined, but likely to look like an extended TPCC.
- Specifications should be complete by early 2003 (?), with design and fabrication by the end of FY03.

Beyond FY03:

- No obvious major tasks, but expect some amount of continuing maintenance and possible extensions of functionality through additional VHDL. Also may need some board layout in support of the R&D program (traditionally, this work has been done by George not Bryan). Estimates are probably very conservative.
- Present test system components should continue to serve well even for “beyond DSM” chips, as the LVDS interface standard we use should continue to function adequately for 0.13μ processes (most likely VDD=1.0-1.2V).