Background

New double-sided stave geometry is under consideration, one with 10 electronics chips across a 10cm wide module. The chips are mounted on a 1.5cm wide hybrid, in the same fashion as on the 6 chip double-sided stave geometry.

Before jumping into a full-blown stave layout, investigative thermal solutions for this configuration were made. The principal objective is to establish whether the simple U-Tube cooling channel design could be retained, as judged by chip and silicon module temperature. An alternative option included in this assessment is to use Triple U-Tube geometry, but still retaining the inlet and exit at one end. For this investigation, it was convenient to presume a 2.8mm outside diameter cooling tube, supplied with CO_2 coolant. The design can be re-visited using C_3F_8 coolant, but one is faced with a considerable heat load for a 1m stave length.

Three models were constructed using the same chip size used in the earlier models, 6.6mm by 8.46mm. As a matter of interest one model was limited to the 8.46mm chip length. This solution precludes thermal heat spreading along the stave Z-axis, via the BeO hybrid, silicon module, and the stave composite face. Admittedly, the result is academic, but it does reveal how powerful the thermal spreading is limiting chip temperature.

It is convenient to use symmetry features afforded by the double-sided stave feature. Referring to Figure 1, the model is split at the upper/lower mid-plane of the stave and at the mid-plane between chip arrays (every 2.5cm).

Figure 1(a), which does not allow heat spreading in Z, illustrates a model limited to one chip length. Figure 1(b) is a complete model 2.5cm long that simulates the single U-Tube cooling geometry. As shown in Figure 2(c), another tube was added to simulate the Triple U-Tube concept.

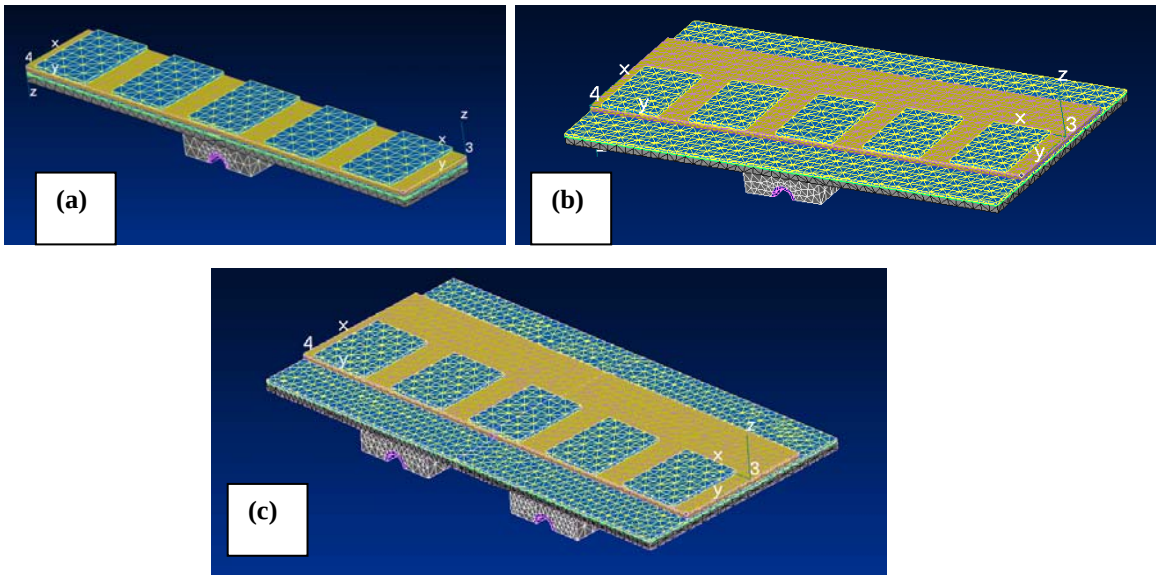

Figure 1: Three FE models to describe the thermal solution for the 10cm wide, 10 chip module.

In all three models the material thermal and material thickness properties are identical[1]. Another common thread in all three models is the POCO Foam body, which attaches the cooling tube to the composite facing. This transition piece is 8mm wide by 4.6mm high (controls facing separation). Each POCO Foam transition piece contributes .048% radiation length for 10cm wide stave. For the single U-Tube this is equivalent to 0.096%. And for the Triple U-Tube the effect is double this value, or ~0.19%. It is possible that the cross-section can be trimmed a bit, but it is suggested that the width in contact with the composite facing remain approximately the same.

Figure 2 depicts the simple solution for 2D heat flow, restricted to transfer from the chips directly to the cooling tube. The load is 0.5W per chip, total 2.5W. The RHS of Figure 2 is annotated to illustrate the high thermal gradients which occur in the cable and the composite facing.

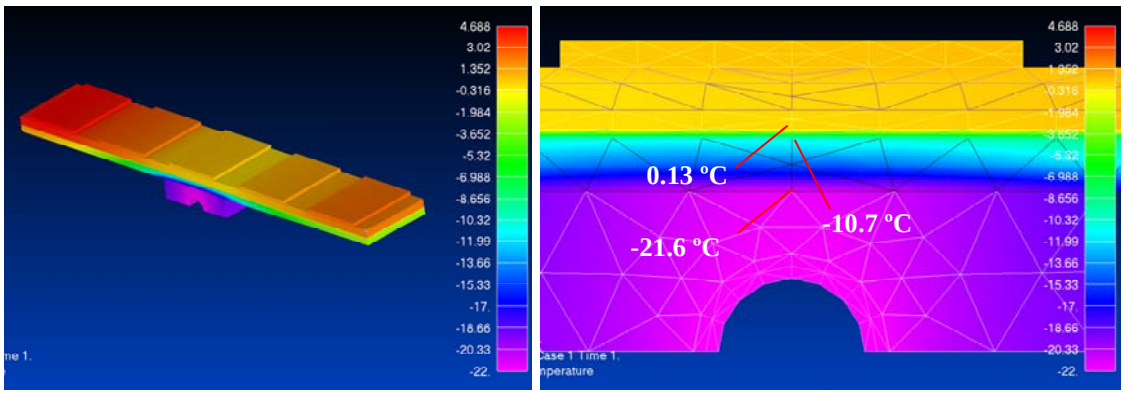

Figure 2: FEA of no heat spreading in the stave axial direction. Chip peak temperature is 4.7ºC. Gradient directly above the cooling tube through the composite facing is ~10.9 ºC. Temperature drop through cable for this same region is ~10.8ºC.

By adding the third dimension to the model heat spreads throughout the hybrid and silicon module, reducing the heat flux through the cable and the composite facing. Referring to Figure 3, one sees the beneficial effect of heat spreading. The chip temperature has dropped dramatically. The gradient through the composite facing directly above the cooling tube is ~3ºC and through the cable ~2.6ºC. One should be notice that the cable is 1/6 the thickness of the cable, yet contributes comparable resistance.

The warmest point on the silicon strip detector is -14.5ºC for the reference cooling temperature of -22ºC. It is important to realize that this temperature does not include thermal resistance terms for the adhesives. This effect we have been adding after settling on geometry.

Forming a simple ratio of 5W to 3W (i.e. 6 chips versus 10 chips) and multiply the chip temperature to coolant drop of 6ºC (NASTRAN solution Feb LBL meeting,

[1] Material thickness: Chip=0.38mm (148W/mK), Dielectric hybrid=0.28mm (5W/mK), BeO=0.38mm (210W/mK), Silicon module=0.28mm (148W/mK), Kapton cable=0.125mm (0.12W/mK), Composite facing=0.76mm (axial=360W/mK, thickness=1.44W/mK), Al tube=0.014in wall (204W/mK), POCO Foam=2.3mm (50W/mK in-plane, 150W/mK thickness)

results in an estimated overall temperature gradient of 10 ºC. With reference to Figure 3, the corresponding temperature gradient is 8.7 ºC. The previous solution was for a semi-flat tube, whereas this solution is for wider contact with POCO Foam. The increased thermal contact in this model contributed to this decrease (15%).

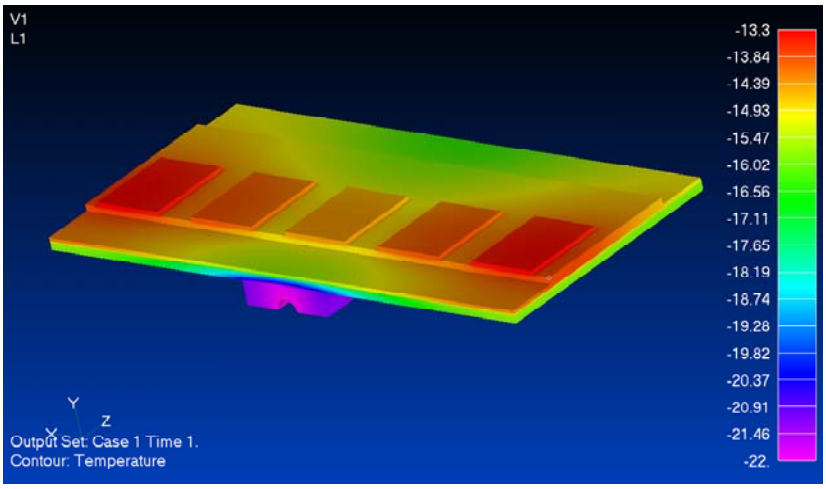

Figure 3: 3D FE thermal solution accounting for heat spreading along the axis of the stave. Peak chip temperature has dropped by 18ºC to -13.3 ºC.

By changing from a simple U-Tube to a Triple U-Tube the peak temperature drops by nominally 3 ºC on the chips. Equally important, the silicon module temperature drops to a range of -16.7 ºC to -17.1 ºC for an assumed cooling inlet temperature of -25ºC. The gradient through the composite facing and the cable become 1.8 ºC and 2.3 ºC respectively.

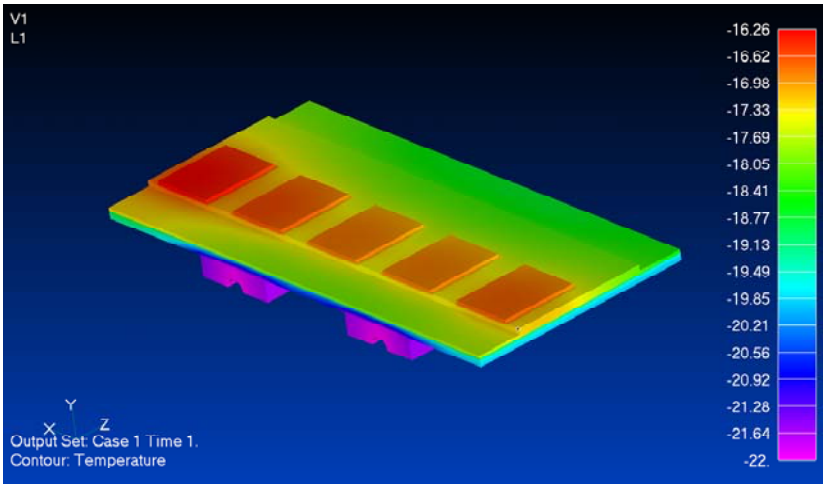

Figure 4: Thermal solution for 10cm wide stave with Triple U-Tube cooling system.