

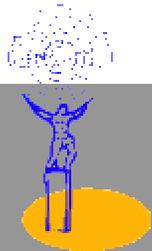


# Progress and Status of ATLAS SCT Construction in the US.

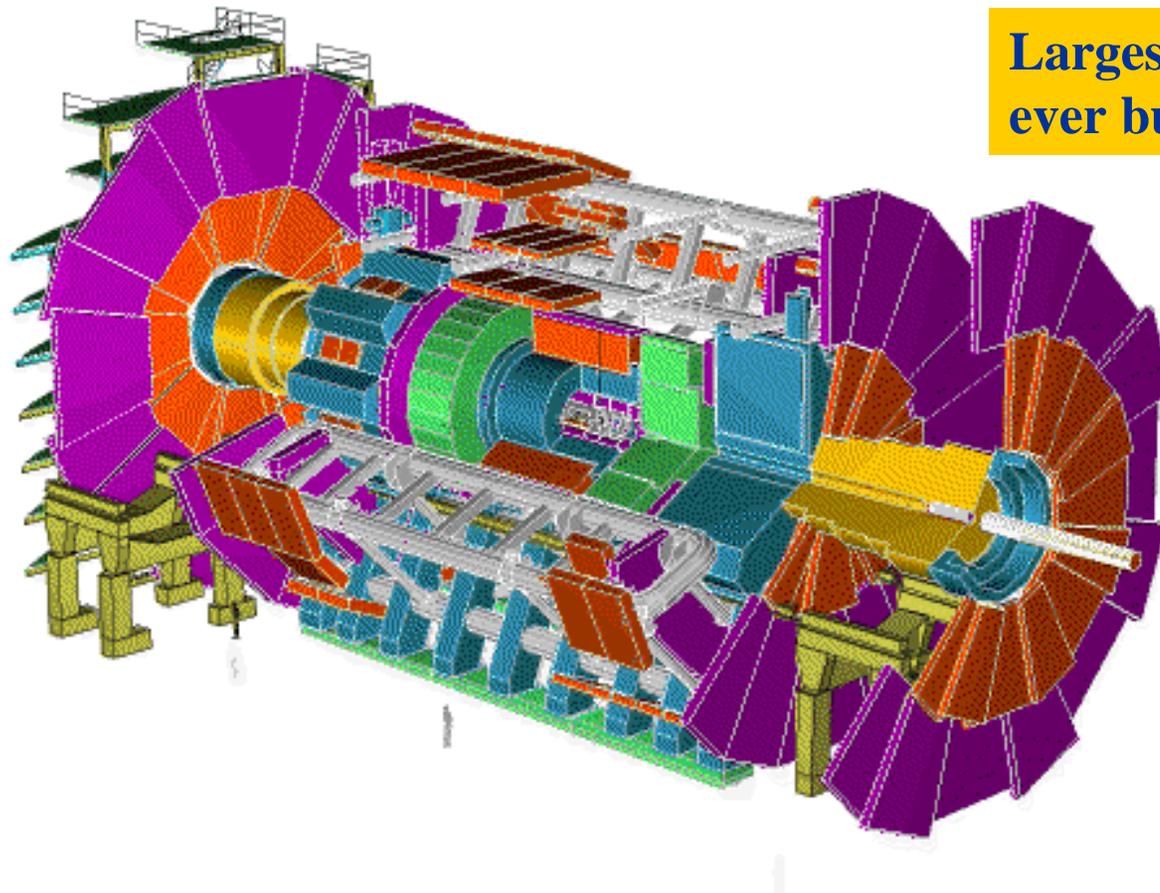


A. Ciocio, V. Fadeyev, M. Gilchriese, F. Goozen,  
C. Haber, B. Jayatilaka, T. Johnson, F. McCormack,  
C. Vu, T. Weber, R. Witharm, L. Zimmerman  
*Lawrence Berkeley National Laboratory, Berkeley,  
California, USA*

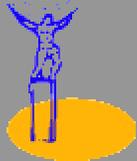
M. Anderson, A. A. Grillo, A. Seiden, F. Rosenbaum,  
W. Rowe, M. Wilder  
*SCIPP, University of California Santa Cruz, USA*



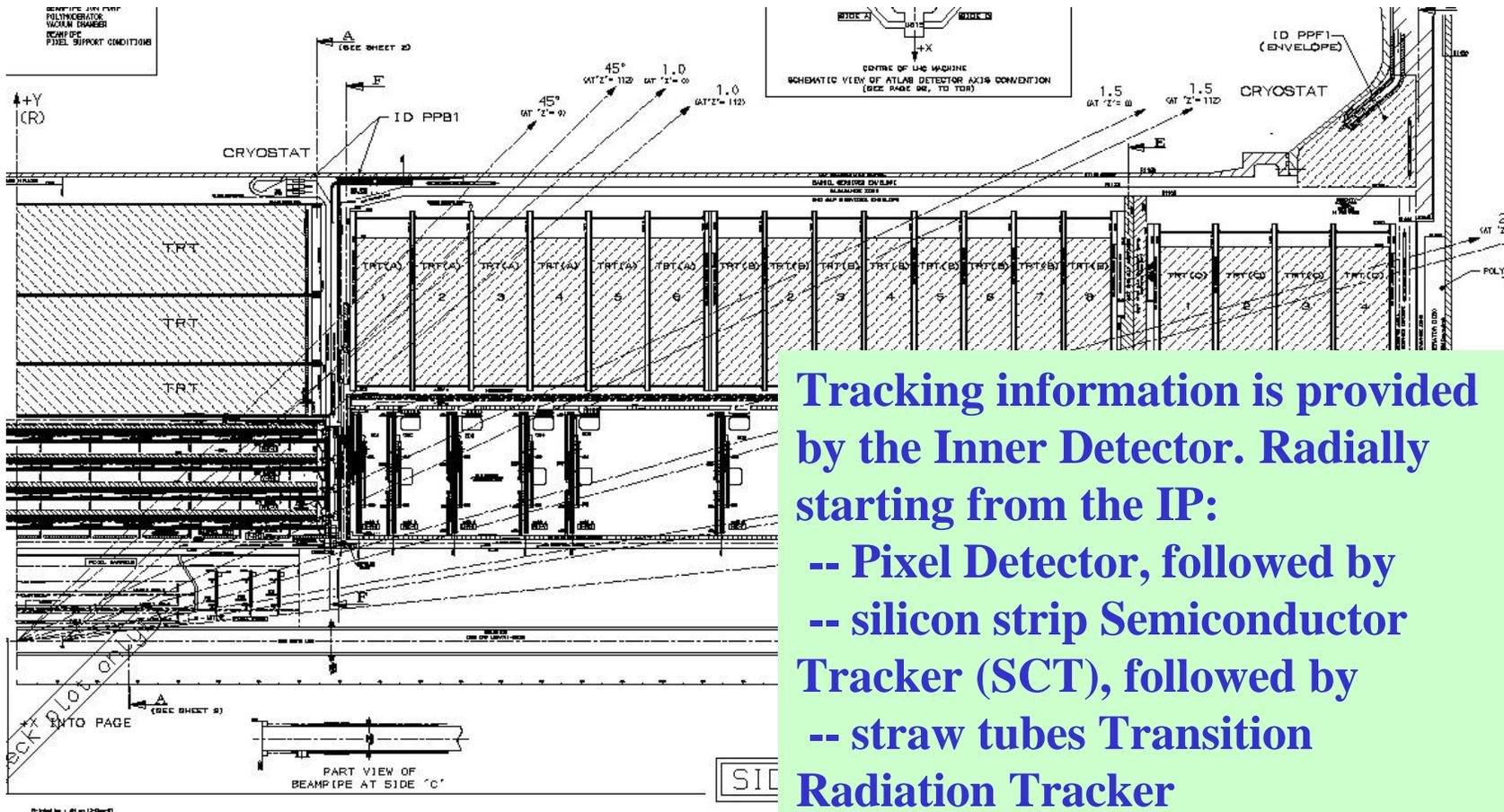
# ATLAS Detector



**Largest HEP Apparatus  
ever built**

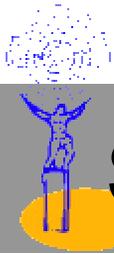


# SCT Geometry



Tracking information is provided by the Inner Detector. Radially starting from the IP:

- Pixel Detector, followed by
- silicon strip Semiconductor Tracker (SCT), followed by
- straw tubes Transition Radiation Tracker



# SCT Features and Requirements

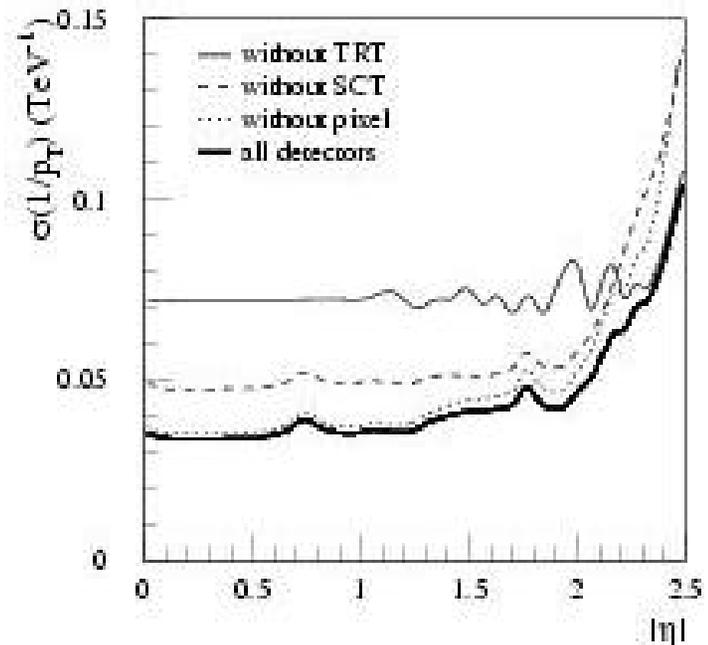


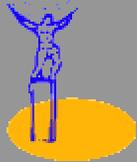
## Features:

- 4 barrel layers, at 300, 373, 447, and 520 mm radii.
- 9 forward disks
- 60 m<sup>2</sup> of silicon strip sensors with 60,000,000 readout channels
- 4,000 modules and 50,000 front-end ASICs
- 16  $\mu$ m (R $\phi$ ) and 580  $\mu$ m (z) spatial resolution

## Unique Requirements:

- Rad-Hard up to 10 MRad
- 25 ns bunch-crossing time
- Large-scale distributed project

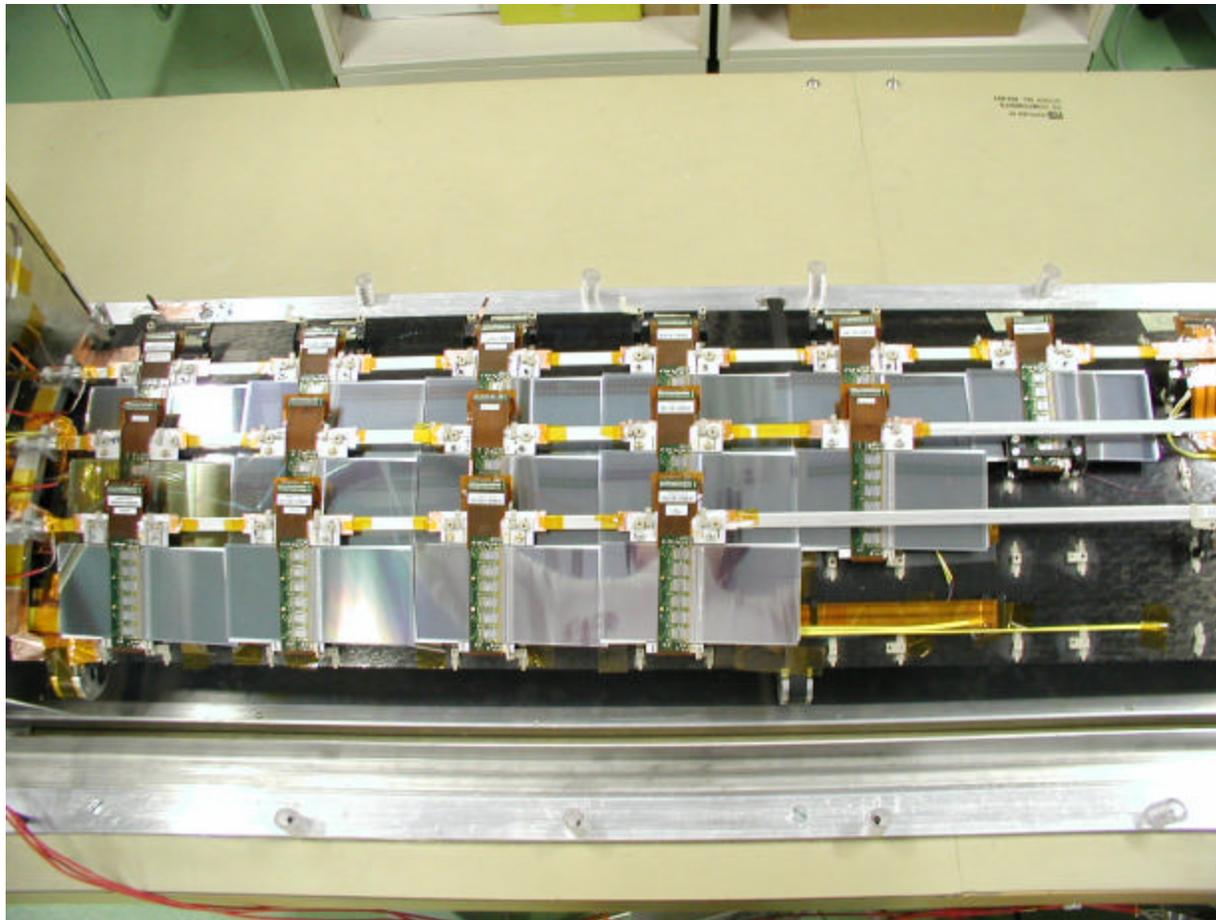




# SCT System Test View



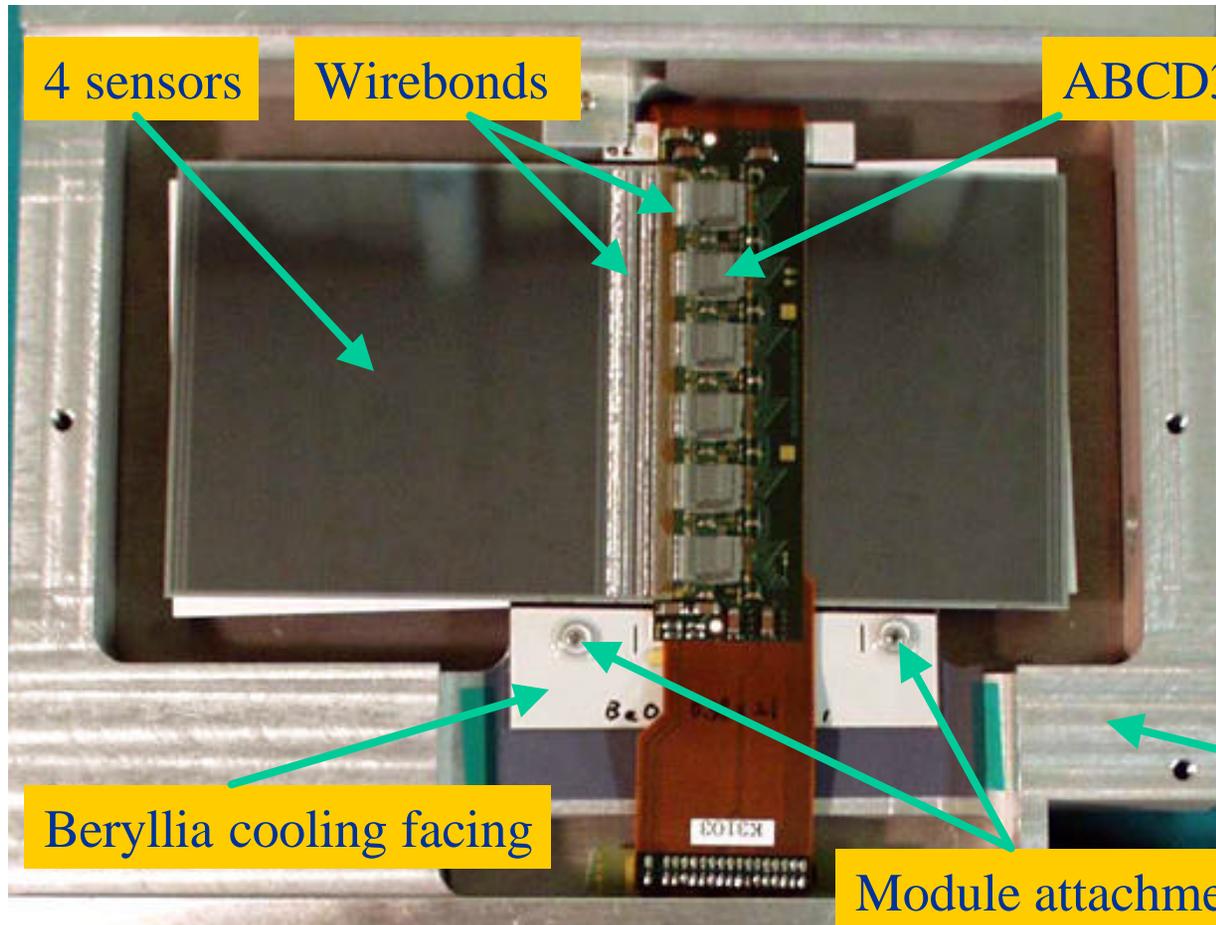
SCIPP BERKELEY LAB



SCT System Test  
with 15 modules  
mounted on a barrel  
sector at CERN.



# SCT Barrel Module

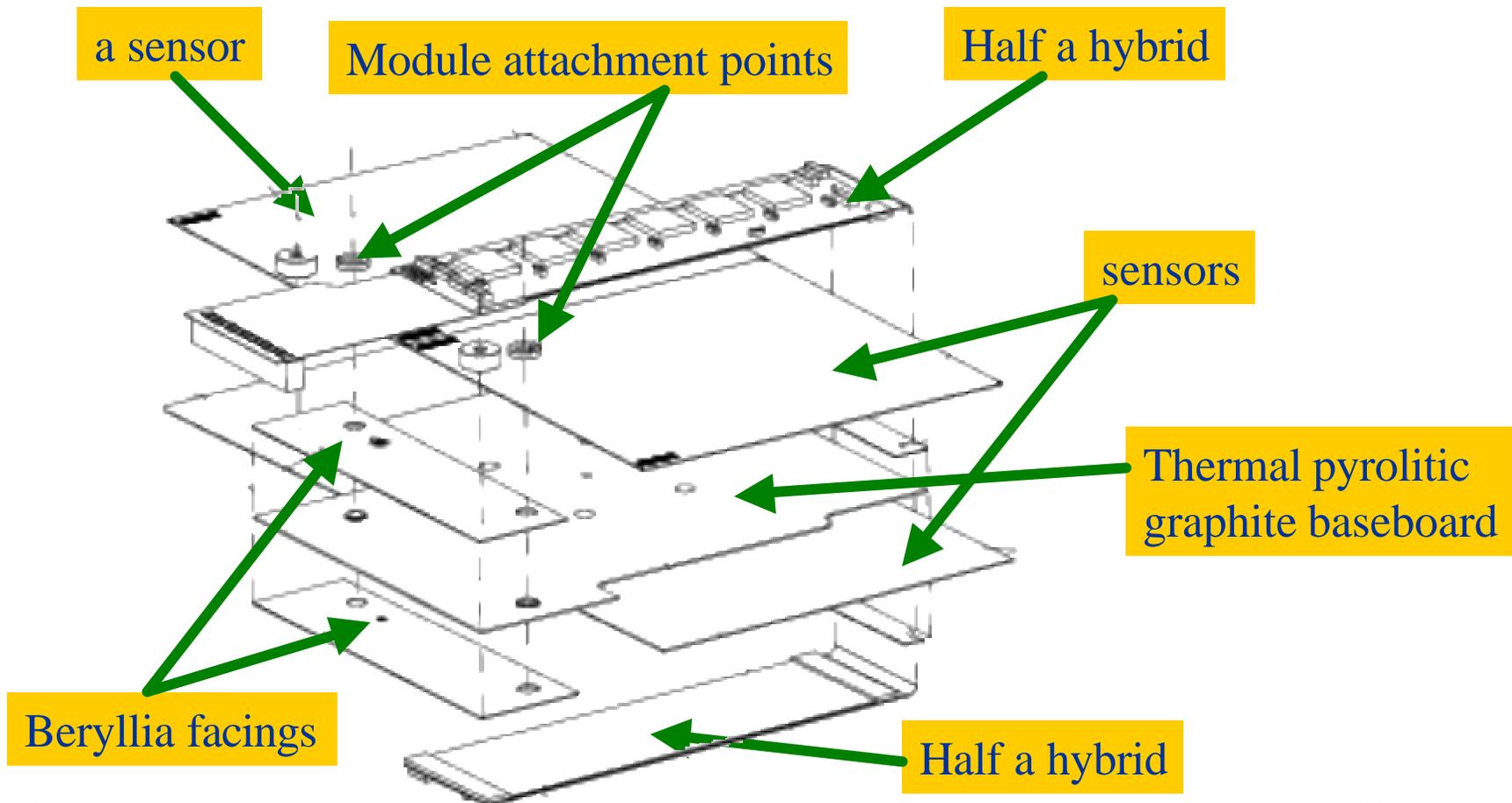


## Features:

- 4 single-sided sensors at 40 mrad crossing angle
- 1536 strips with 80  $\mu$ m pitch
- Multi-Chip Unit
- Large dimensions (12 cm x 6 cm x 1.1 mm)

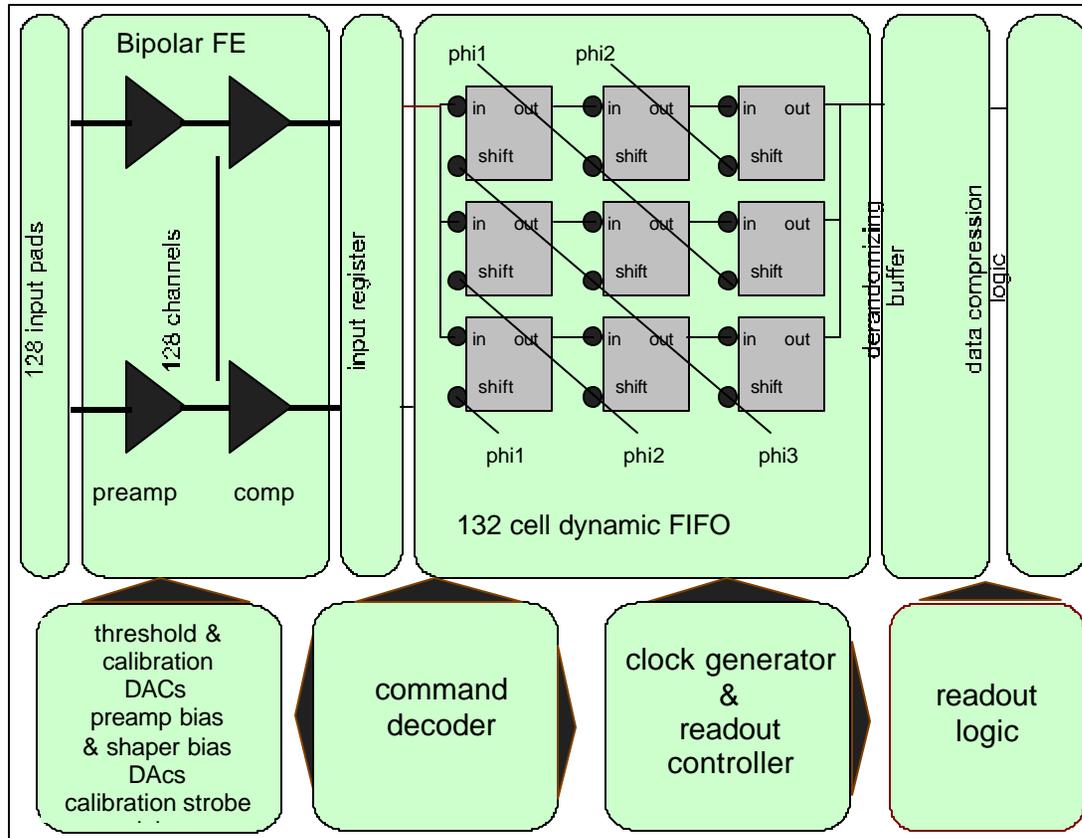


# SCT Barrel Module





# ASIC



## ABCD3T:

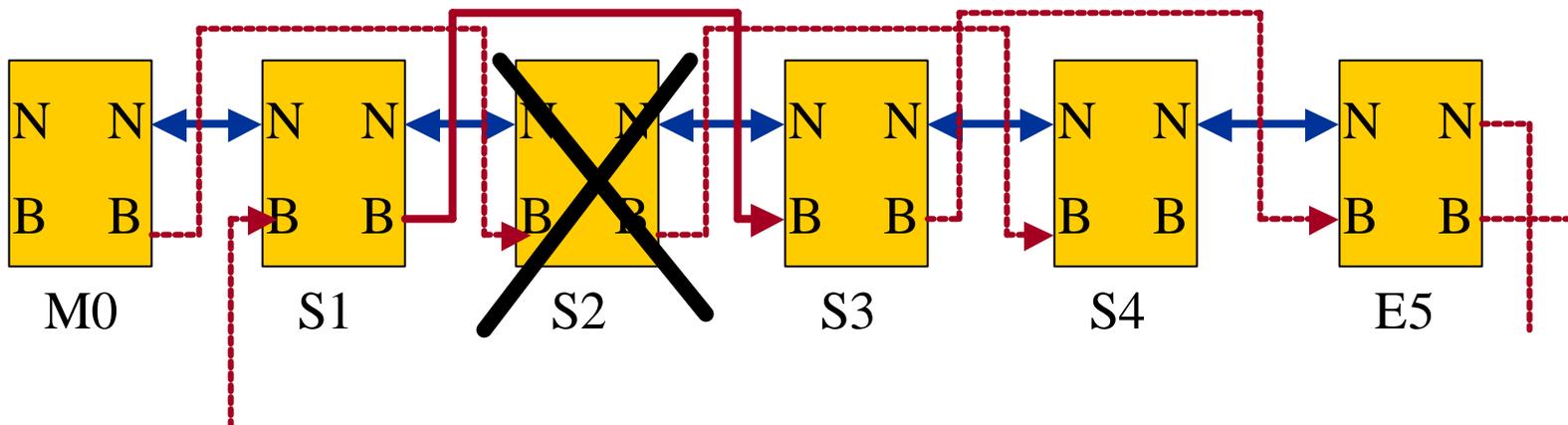
- ✍ 128 readout channels
- ✍ 40 MHz clock
- ✍ analog front-end with amplifiers and comparators
- ✍ binary readout
- ✍ 132-deep digital pipeline and communication circuitry
- ✍ rad-hard DMILL technology
- ✍ 3-bit trim DACs for each channel (channel matching after irradiation)
- ✍ edge or level sensing mode
- ✍ sparsification

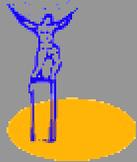


# ASIC Communication and Redundancy



- The data transfer on hybrid is serialized, thereby avoiding extra intelligence.
- Cases of a chip failure are mitigated by redundant data routes, bypassing the failed chip.



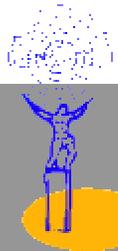


## LBNL Asic Tester (“LAST”)

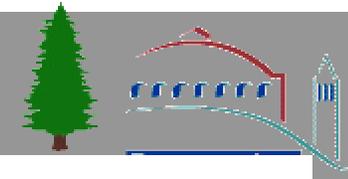


Large number of specialized chips => developed a customized Tester. At the wafer level, we verify:

- ➡ Analog front-end performance
- ➡ Digital functions (control register, addressing, communication, pipeline, output buffer)
- ➡ Power Consumption
- ➡ Internal DACs linearities
- ➡ I/O Signals Properties (timing, amplitudes, duty cycles)

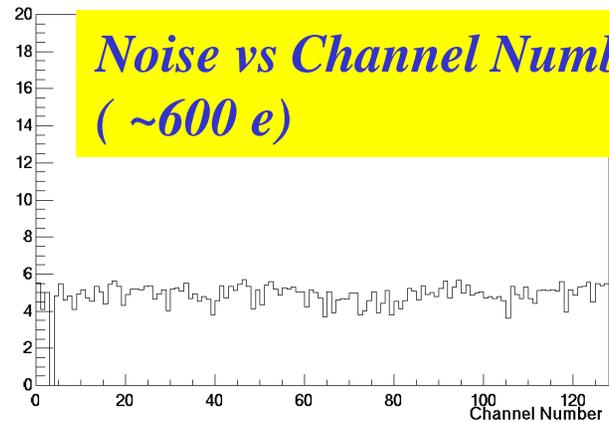


# LBNL Asic Tester ("LAST")

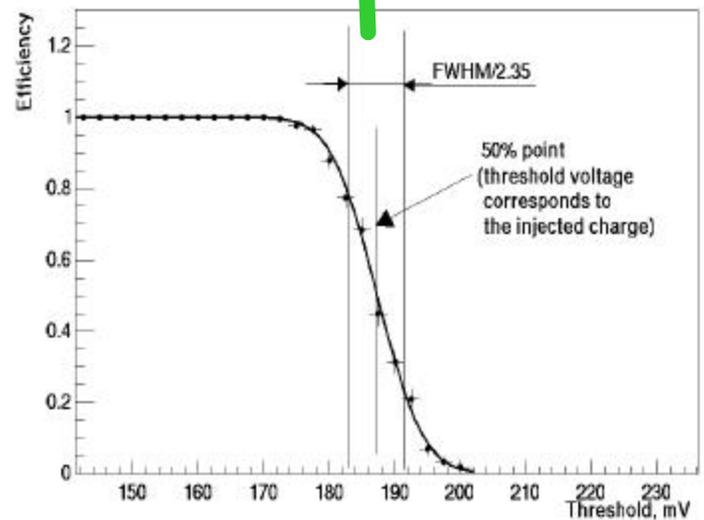


Test the analog front-end via charge injection. Take 400,000 histograms per wafer.

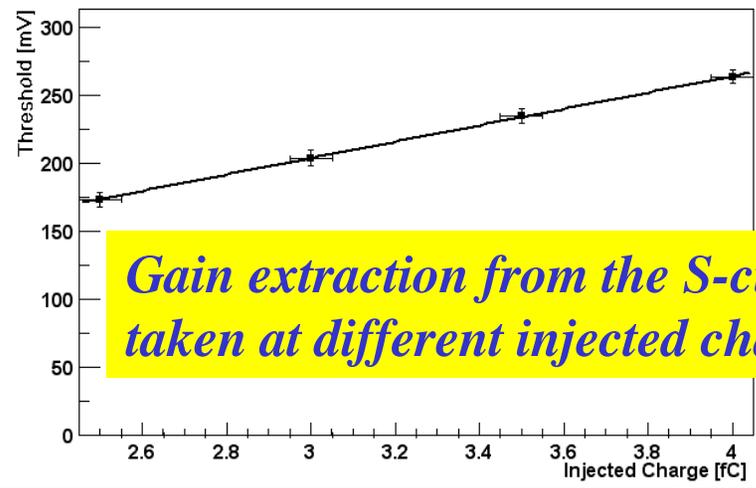
Noise, in mV



S-curve fit



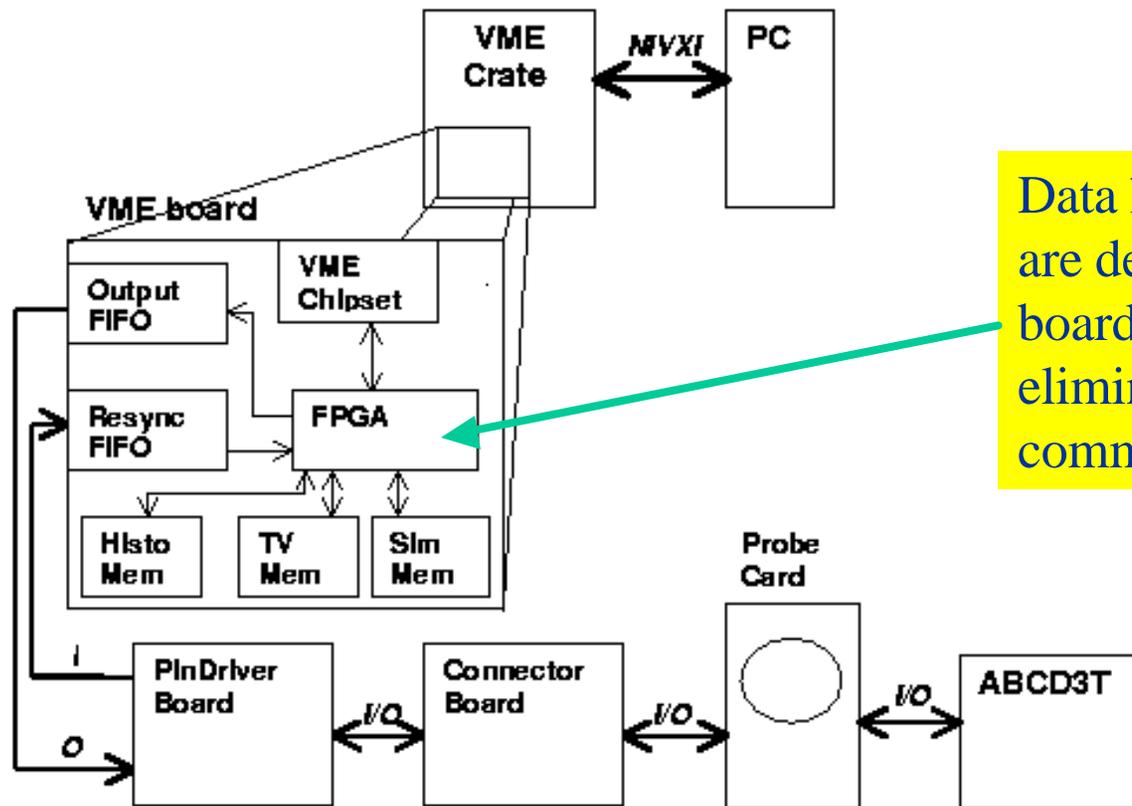
*Threshold scan*



*Gain extraction from the S-curves taken at different injected charges.*



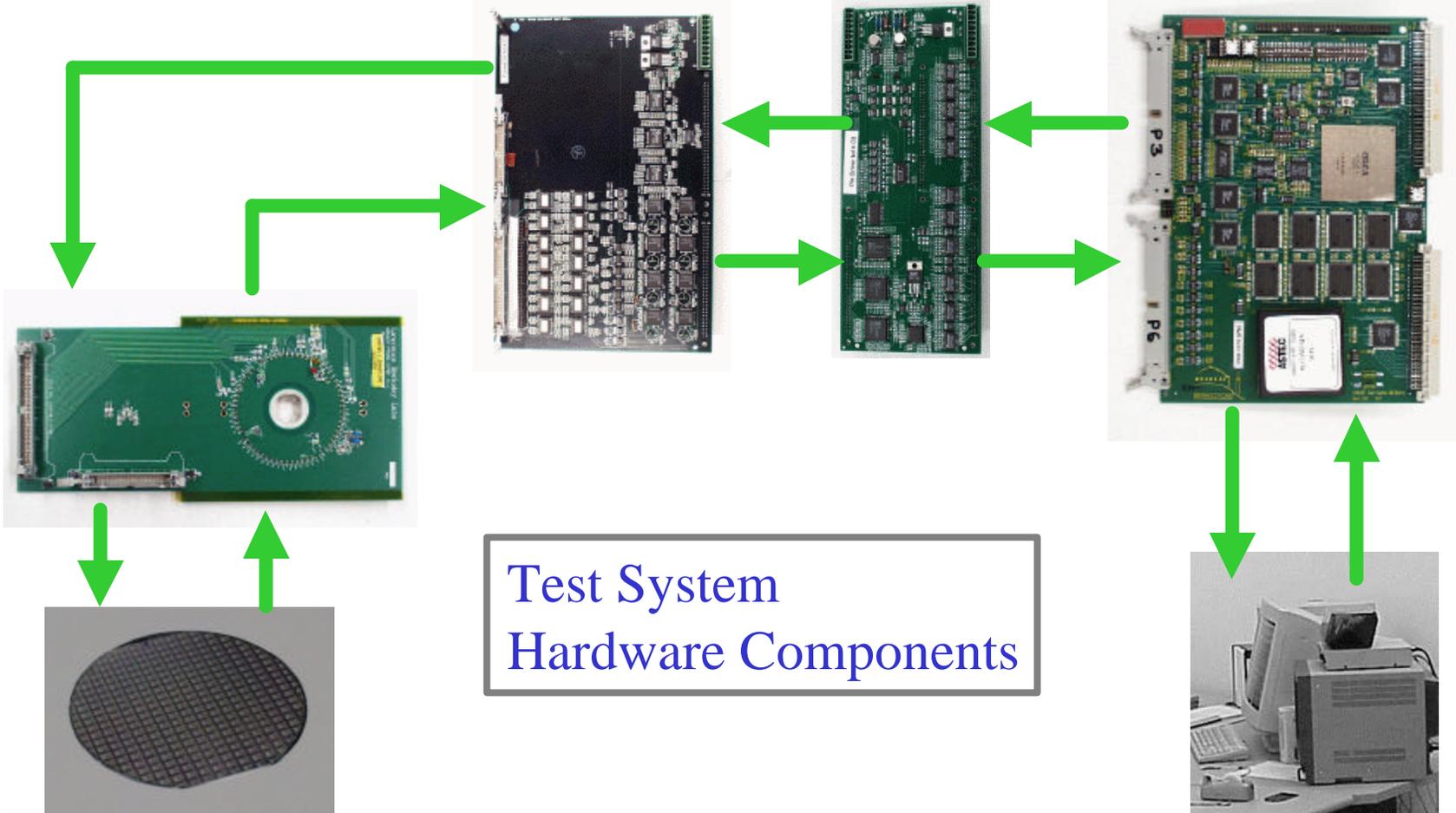
# LBNL Asic Tester ("LAST")



Data handling algorithms are delegated to the VME board FPGA thereby eliminating the PC communication bottleneck.



# “LAST” Components





# “LAST” at RAL



Test setup at  
Rutherford  
Appleton  
Laboratory, UK

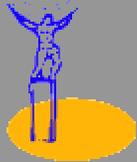




# Chip Production and Testing



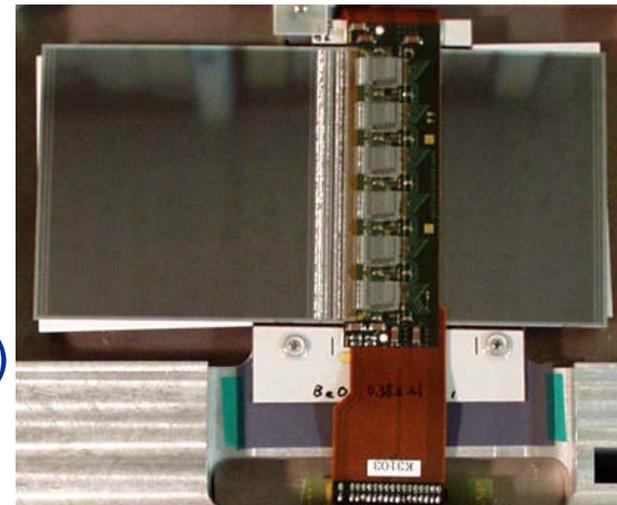
- Test time was optimized to be ~1 min/chip ( $\Rightarrow$  5 h/wafer).
  - Limited by the communication with chips under test.
  - Commissioned 4 test systems to shoulder the test load:
    - SCIPP (2),
    - RAL,
    - CERN
- (built, debugged, calibrated 8 systems)
- The chip yield is consistent across the test sites within 2%
  - Chip production is well advanced, > 30% of chips are tested
  - The yield is close to the 26%, the minimum value specified in the contract with the manufacturer.



# Module Builders

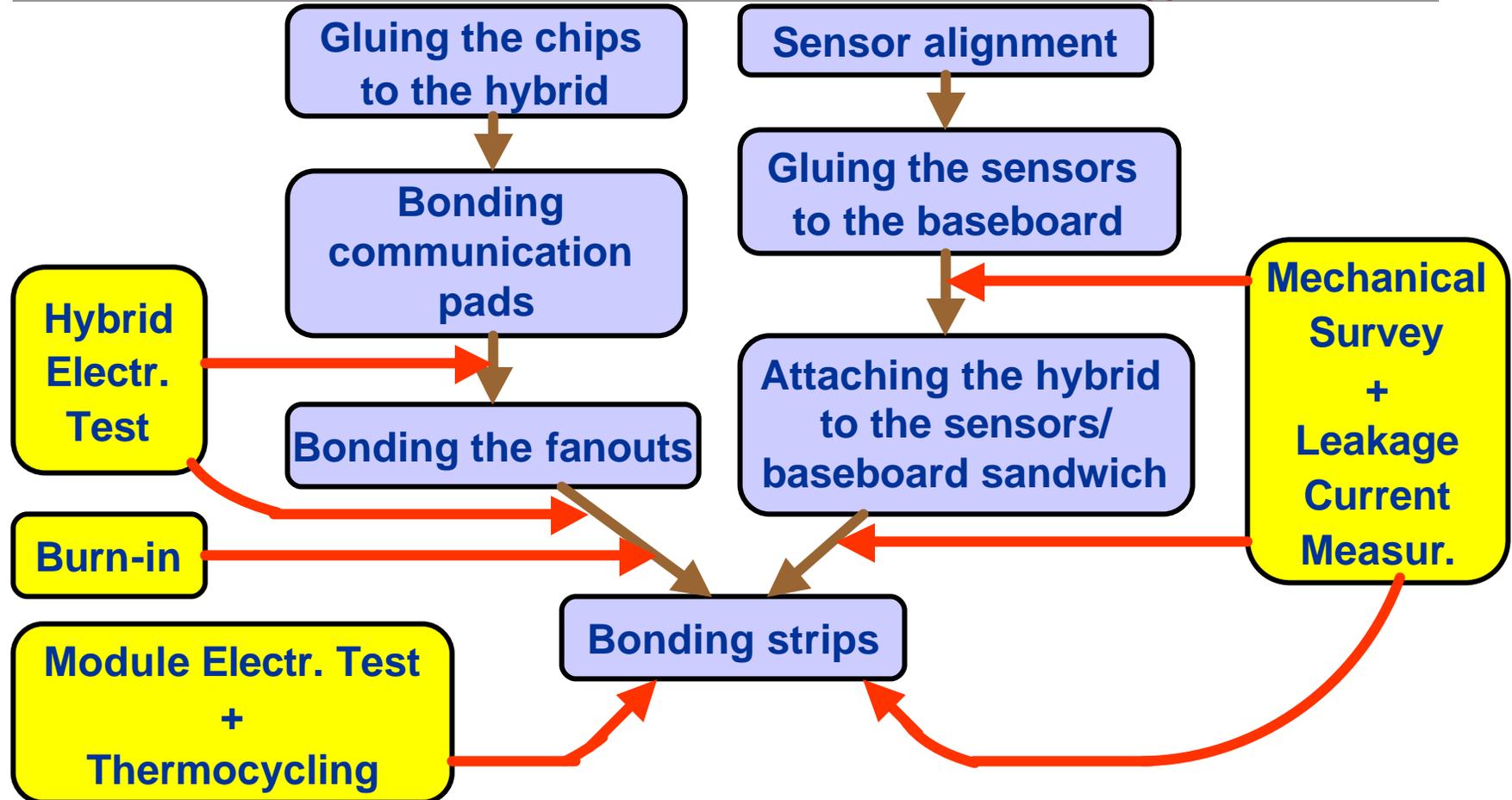


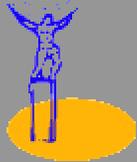
- Barrel SCT modules are built at 4 different sites:
  - Japan (KEK), UK, Scandinavia, and US (LBNL/SCIPP)
- US to build 700 modules (~1,000,000 channels, more than CDF silicon system)
- Plan on the steady production of 3 modules/day
- Have to demonstrate the ability to build modules reliably to the community => build 5 modules to qualify for the production





# Building a Module



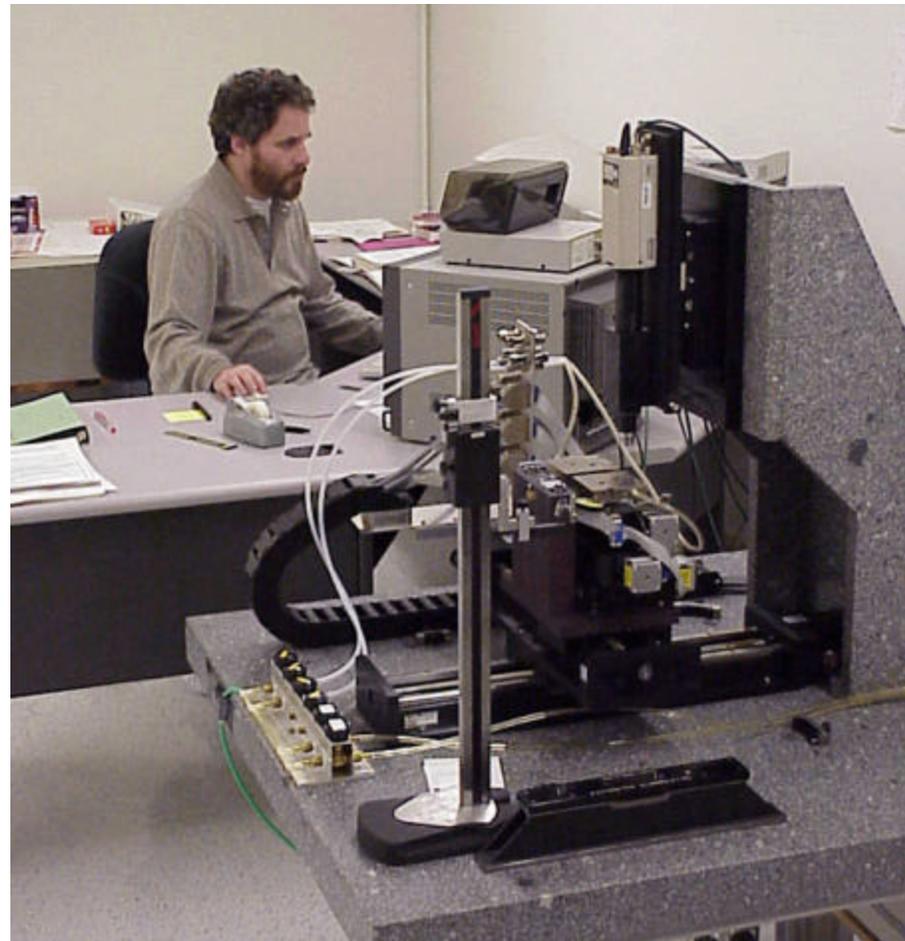


# Sensor Alignment



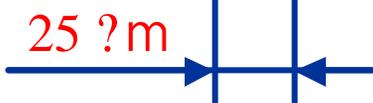
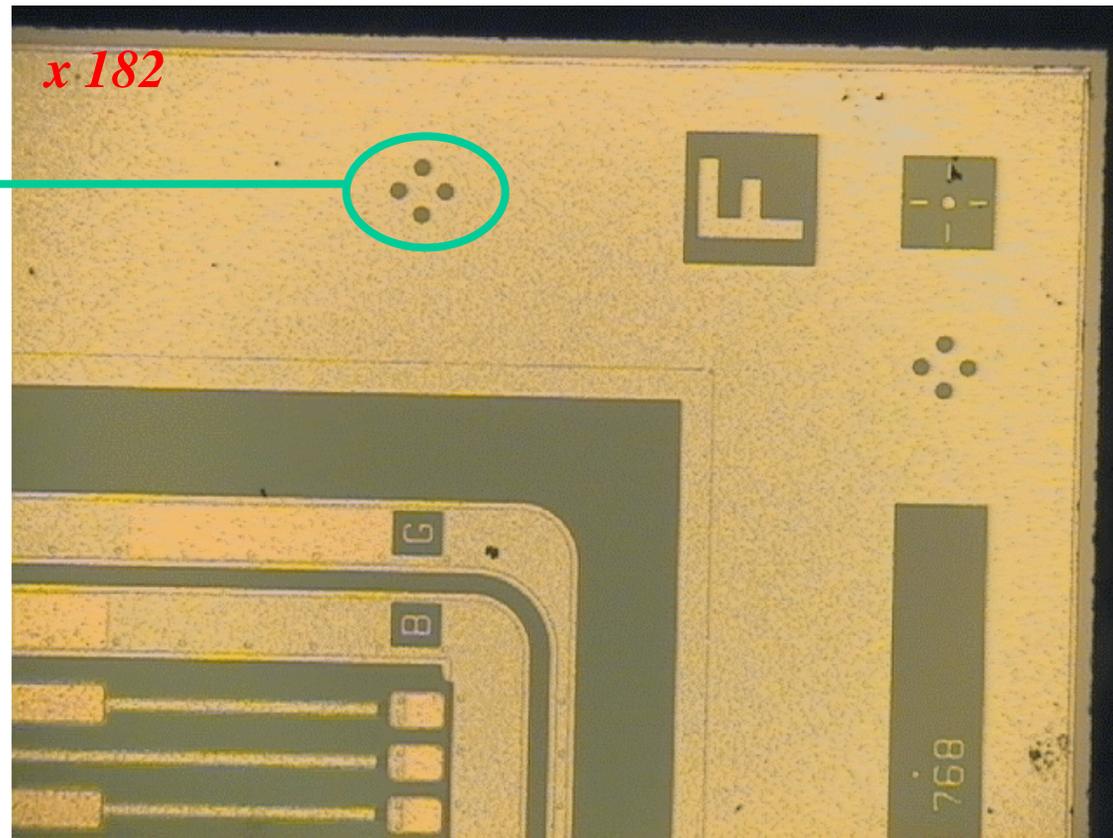
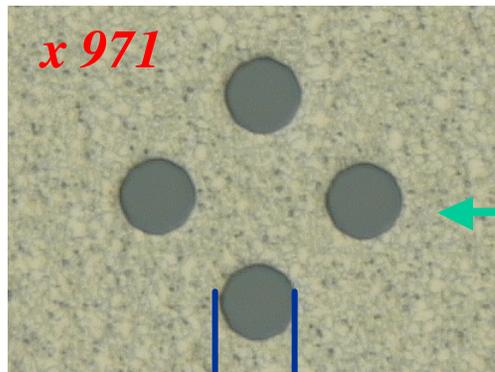
Relative alignment of a pair of sensors using their fiducial marks

Motion stages with video camera under LabView control





# Sensor's Fiducial Marks

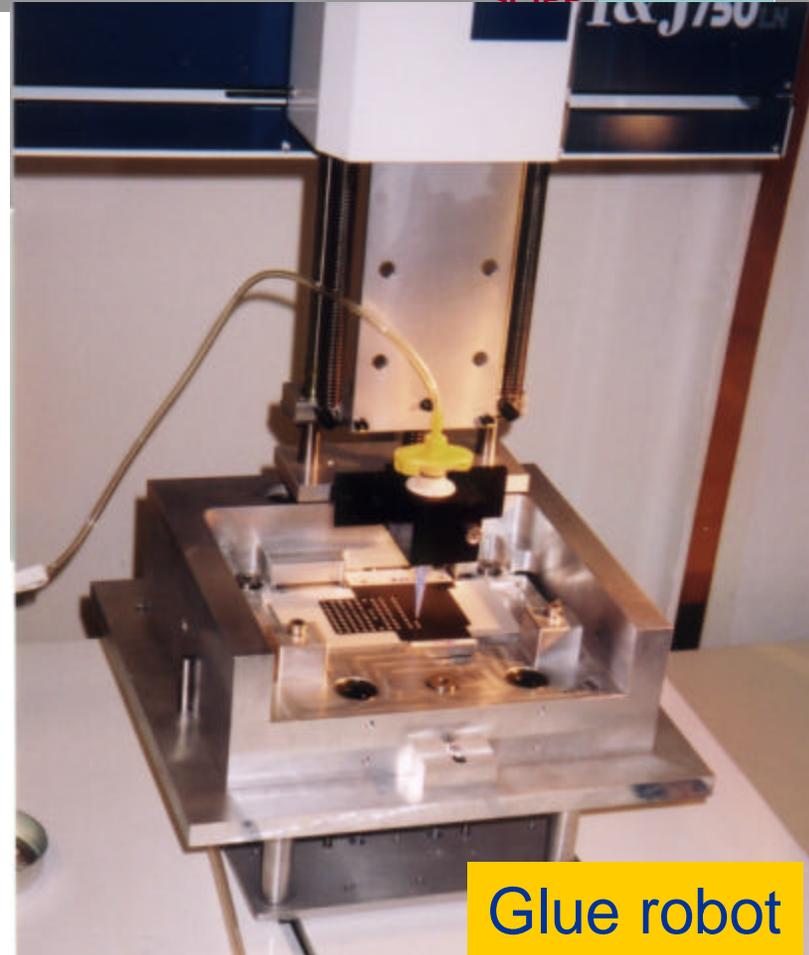




## Gluing sensors to the baseboard



Precision glue dispensing  
(affecting the module  
thickness)



Glue robot



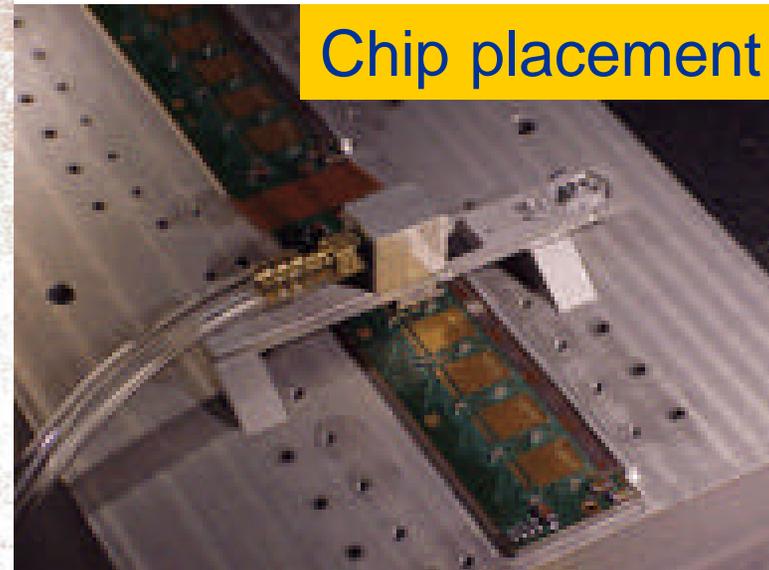
## Gluing ASICs to the hybrid

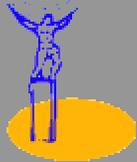


- Conductive glue to ensure good ground for ASICs operating at 40 MHz
- Special jigs to ensure complete uniform glue coverage underneath a chip



Glue deposition test on glass





# Bonding



Over 3,000,000  
bonds to do

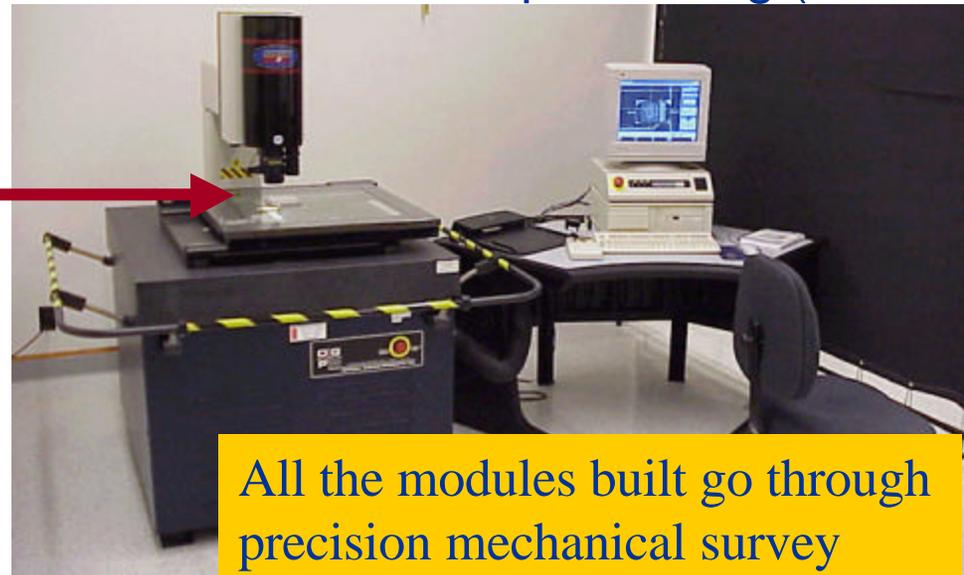
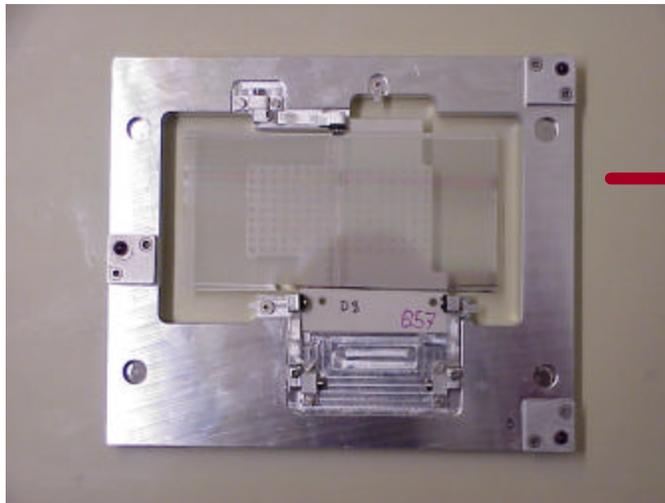




# Mechanical Survey



- No other stand-alone tracker helping in calibration
- => must have excellent initial approximation
- => tight mechanical tolerances on the shape and orientation of the 4 sensors and the baseboard
- Especially tight specs on the front-to-back relative positioning (5-10 ?m)



All the modules built go through precision mechanical survey



# Leakage current



**Sensitive to the sensor quality, surface contamination (mishandling etc)**



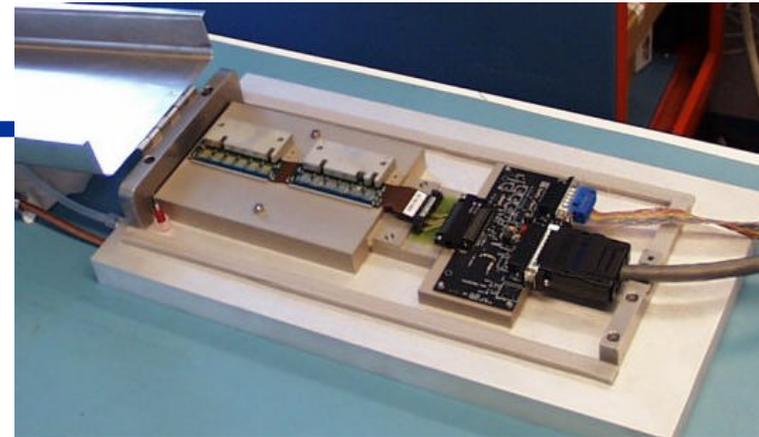


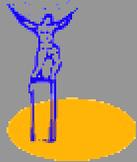
# Electrical Tests



Extensive electrical tests of hybrids and modules, coupled with

- burn-in and
- thermocycling.

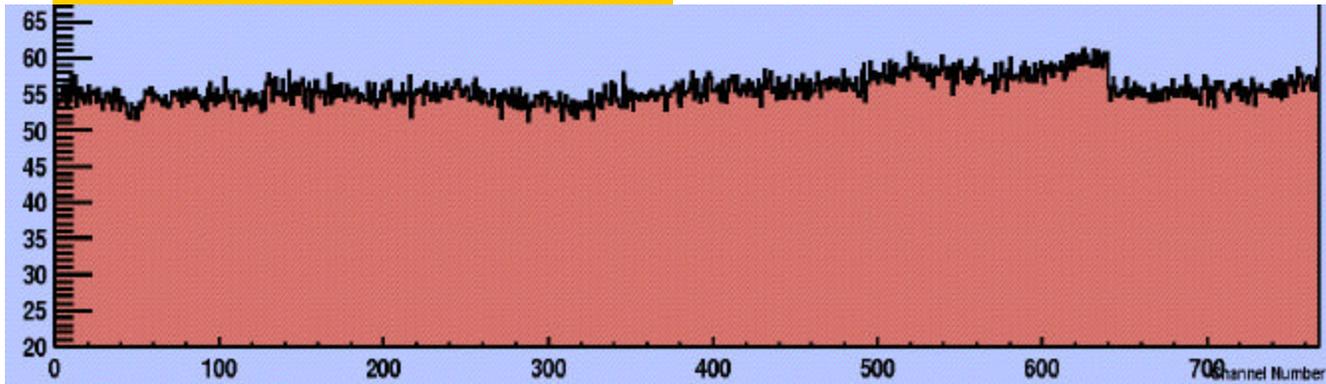




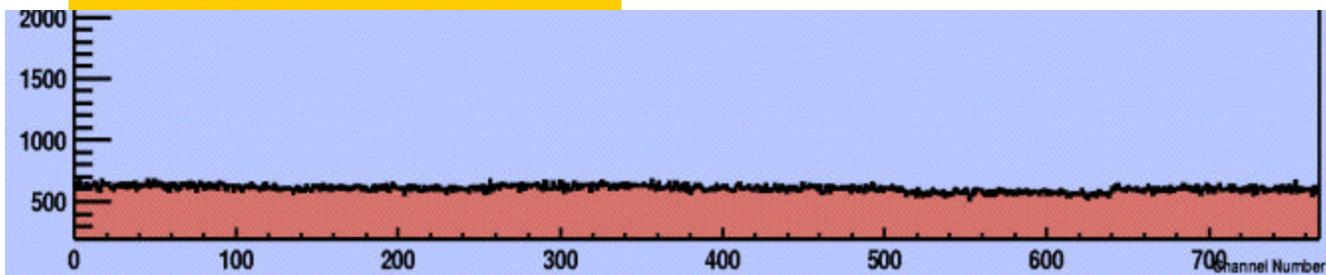
# Electrical Tests



Gain [mV/fC] vs. channel number

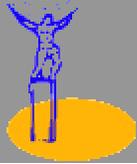


Noise [e] vs. channel number



Tests similar to the ones for the wafer screening:

- Analog
- Digital
- Power
- Consumption
- IV Scan



## Status



- Component production is well advanced
- KEK module building site is in production; US and other sites are in the process of qualification
- Gained experience with a dozen mechanical dummies
- 4 electrical modules have been built and met the specs
- Plan to begin the production in June-July with the steady-state rate of 3 modules/day by the end of 2002