

Pixel Detectors for Hadron Colliders

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Overview of Goals and Requirements:

- High luminosity colliders present unique requirements of radiation hardness, high occupancy, and precise timing
- Hybrid technology is presently the only feasible approach

Major technical challenges (ATLAS, BTeV, CMS):

- Sensors
- Electronics
- Interconnections, mechanics and cooling

Future directions:

- Improvements in electronics
- Improvements in interconnection technology

Use ATLAS Pixel Detector as source of many examples...

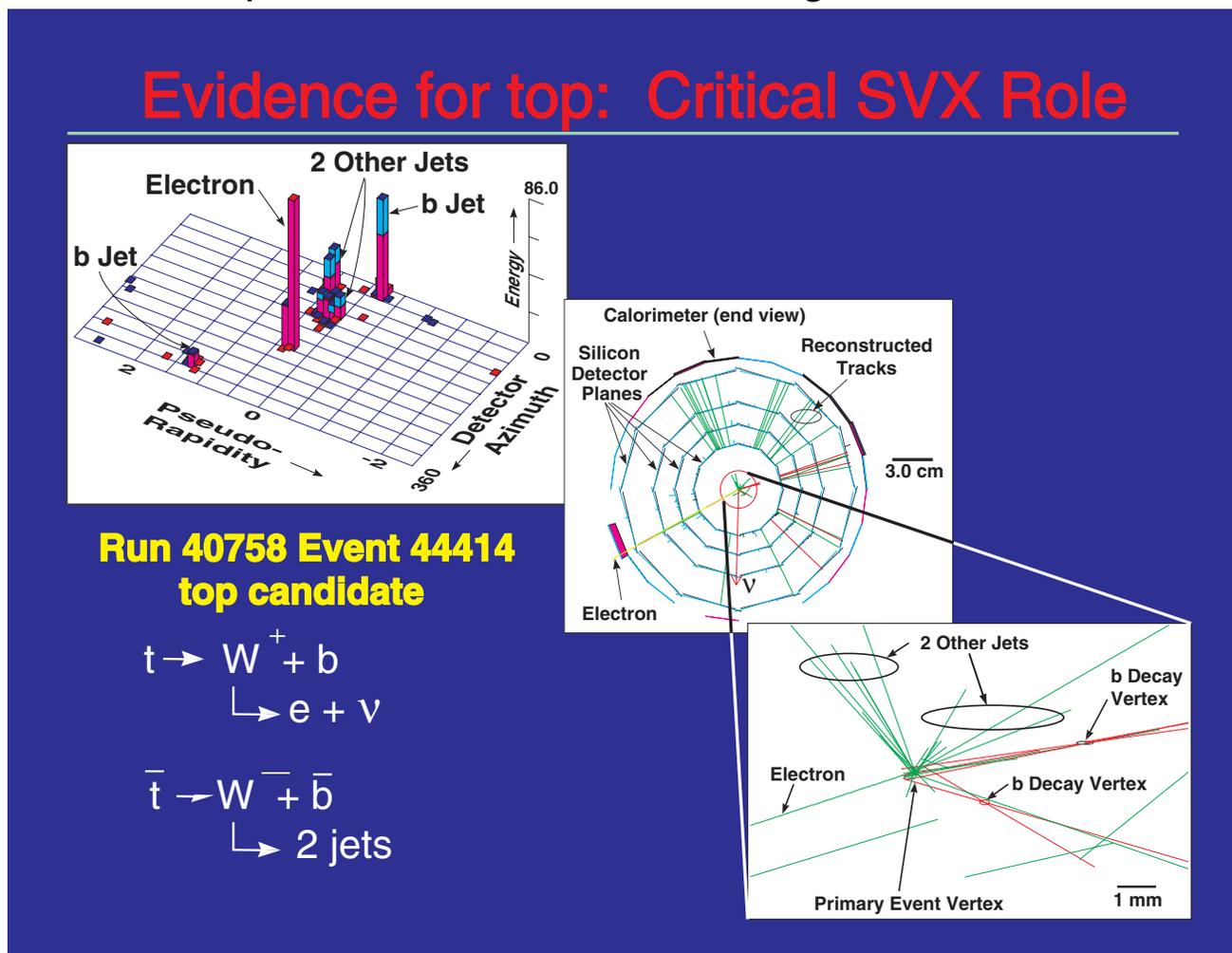
Hadron Colliders and Pixel Detectors

Tracking issues in hadron collider experiments:

- Most high P_T particles produced in hadron colliders are associated with jets, leading to challenging track finding problems (high local particle densities).
- Much of the interesting physics benefits greatly from the reconstruction of heavy quark and lepton decays (especially B's, $c\tau \approx 500\mu$ for B-hadrons), so tracking goals include excellent impact parameter resolution.
- Tracking in solenoidal field implies fitting helices with 5 track parameters: curvature, phi, and dip angle, plus distance of closest approach in r and z.
- Low material budgets (1-2% X_0 per measurement layer) are required to reduce multiple scattering in critical few GeV region.
- More ambitious goals include use of precise silicon tracking information in low-level triggers (e.g. CDF Run 2 impact parameter trigger, proposed BTeV trigger).
- Modern collider experiments all use Silicon Trackers to address these goals. Presently installed systems rely on fine-pitched strips (50-100 μ), and achieve point resolutions of 10-15 μ per measurement plane in one coordinate.
- First example of precision vertexing in a hadron collider was SVX detector installed in CDF in 1992. This provided the first vertex-based b-quark tagging in a hadron collider, leading to evidence for top quark in 1994, and discovery in 1995.

First Evidence for t-quark in Tevatron Run 1a (CDF, 1994)

- With significant input from SVX b-tagging capability, CDF showed $\approx 3\sigma$ effect consistent with t-quark mass of 175 GeV using initial Run 1a data:



- Clear observation of detached vertices in small number of events was compelling.
- Discovery of t-quark followed with greater statistics in Run 1b (CDF + D0, 1995).

High Luminosity:

- The physics potential of hadron collider experiments is often limited by the collision rates that the detectors can reconstruct.
- In the search for rare decays or weak processes such as Higgs production, the maximum tolerable luminosity is critical.

High Occupancy and Precise Timing:

- Hadronic total cross-sections are always large ($\sigma(\text{tot})$ at LHC is $\approx 100\text{mb}$), so high luminosity means very high particle rates (LHC at 10^{34} has 23 interactions per crossing, with roughly 1000 charged particles within tracking coverage).
- Operating at the highest possible luminosity requires resolving the very fine beam time structure (LHC uses 25ns bunch crossing interval).

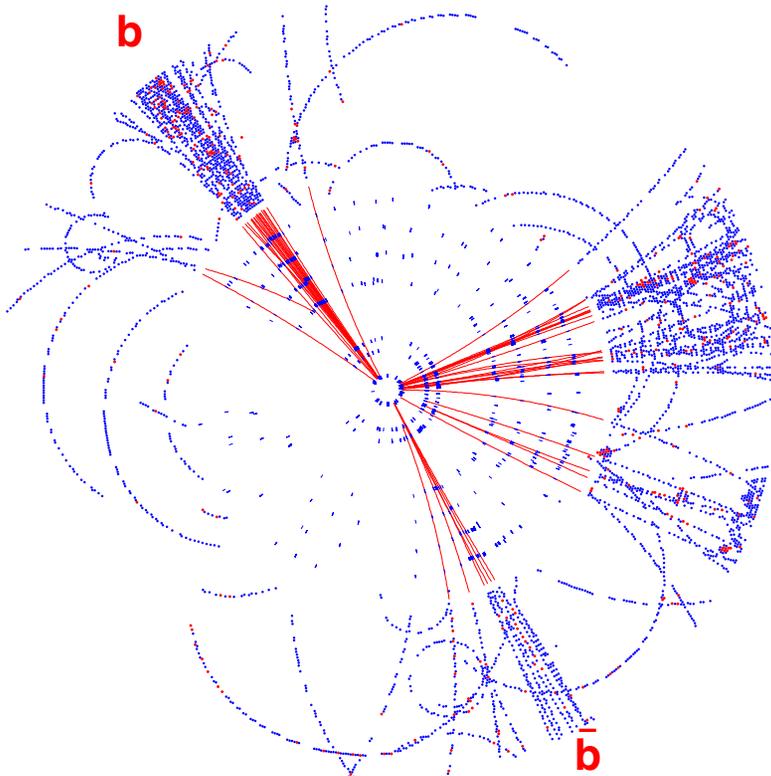
Radiation Hardness:

- High particle fluences in hadron colliders imply very significant radiation doses to electronics and sensors (LHC innermost layer sees more than 10MRad/year).
- Measuring heavy quarks with high precision and largest possible statistics (hadronic B-factories) requires placing vertexing extremely close to the collision region in the forward direction, and also requires extreme radiation hardness (inner edge of BTeV pixel planes also sees about 10MRad/year).

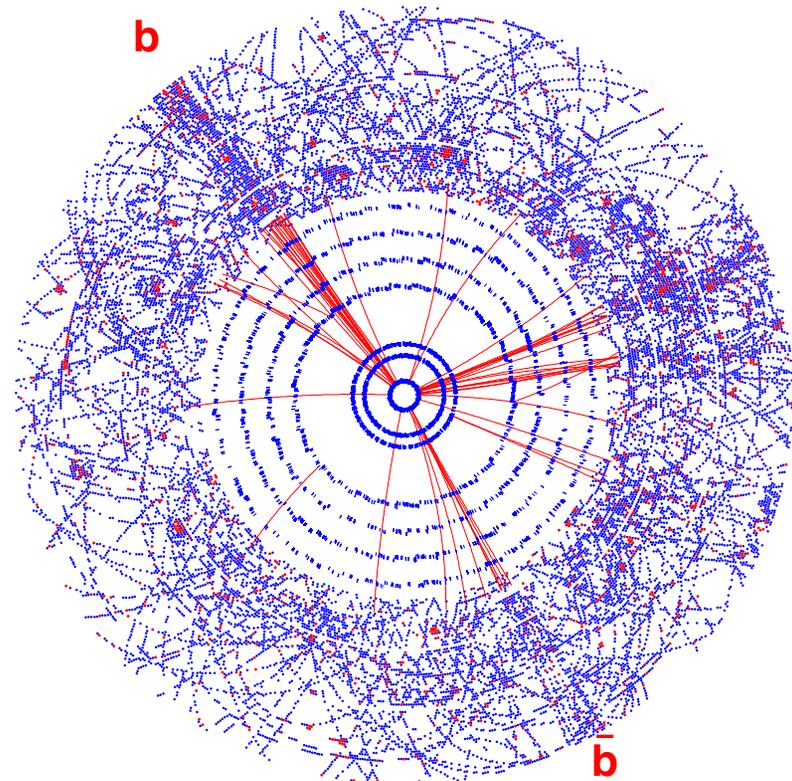
Pattern Recognition and Triggering:

- Pixels provide individual space point measurements with high precision for on-line triggering and offline pattern recognition.
- $H \rightarrow b\bar{b}$ event in ATLAS at zero luminosity and at design luminosity:
(Precision hits shown for $0 < \eta < 0.7$ only, TRT hits for $z > 0$ barrel only)

ATLAS Barrel Inner Detector
 $H \rightarrow b\bar{b}$



ATLAS Barrel Inner Detector
 $H \rightarrow b\bar{b}$



What do Pixel Detectors for Hadron Colliders look like ?

Many approaches to building pixelated particle detectors:

- Charge Coupled Devices (CCDs), either using commercial or custom devices. These are read out serially with no internal zero suppression, and do not provide continuous sensitivity and high readout rate required for hadron colliders.
- Monolithic pixel detectors that detect charge created in the electronics chips. Original approach used custom electronics on high resistivity silicon, but was very limited in circuitry which could be used. More recently, groups have used charge deposited in thin epitaxial layer present in modern deep-submicron processes. This signal arrives relatively slowly (100's of ns?) and is very small.
- Hybrid pixel detectors, in which a separately optimized silicon sensor and commercial electronics chips are connected using flip-chip technology. This allows the design of a high-quality silicon sensor using appropriate base material (oxygenated, high resistivity silicon), and the use of commercial deep-submicron CMOS electronics to implement complex, high-speed circuitry.
- In this talk, focus purely on the hybrid solution and give examples of how this is being used in three major hadron collider pixel detectors now approaching construction (ATLAS, BTeV, and CMS).

Basic building block of a hybrid pixel detector is the module

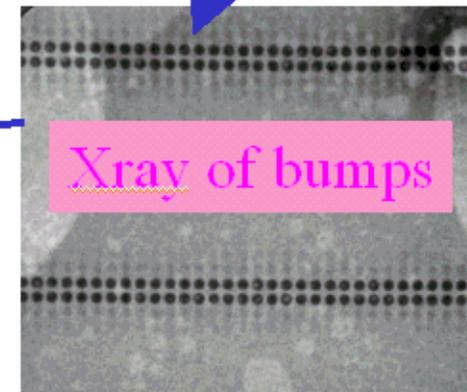
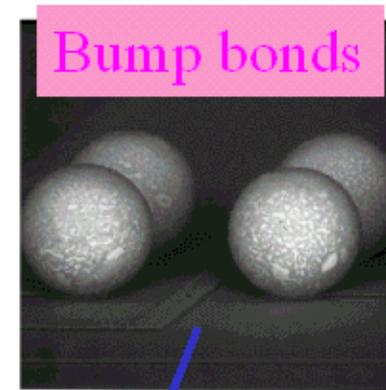
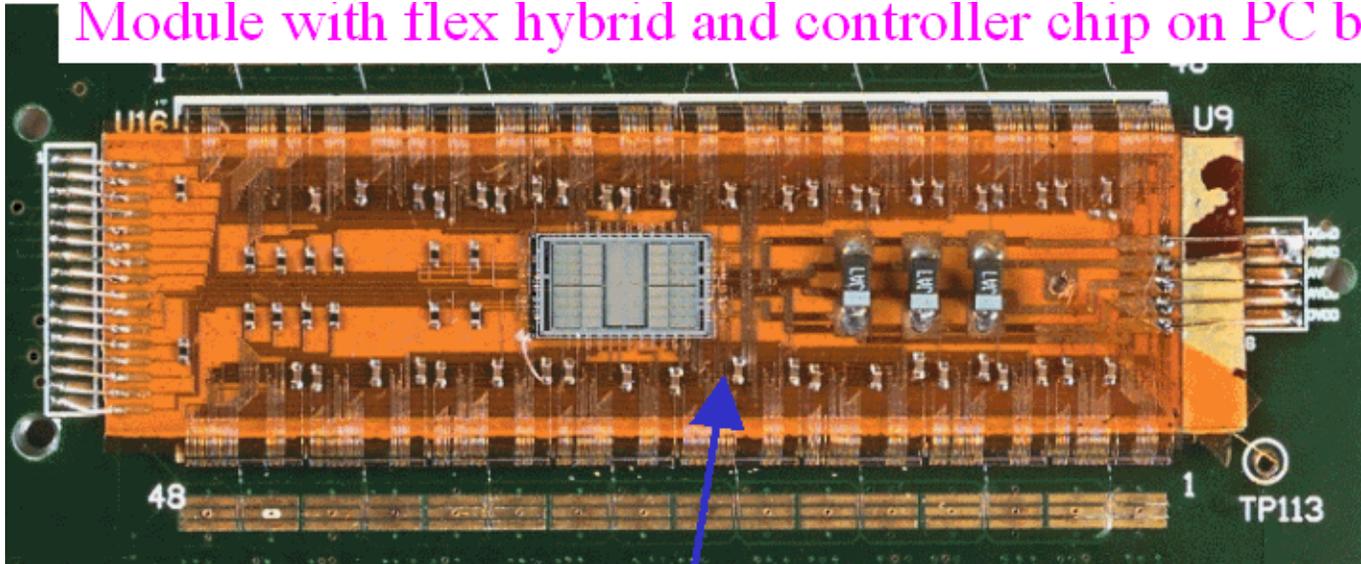
Ingredients of a hybrid pixel module:

Hybrid pixel detector module is a multi-chip assembly:

- Substrate consists of a carefully optimized rad-hard sensor. Preferred technology for pixels is to use n+ on n-bulk. This requires double-sided processing to implement the biasing and guard-ring on the back-side, but after type inversion, it can be operated partially depleted.
- Anywhere from 5-16 front-end chips are attached with fine pitch bump-bonding to the sensor. Typically, this requires 50-100 μ pitches and 20 μ bumps, well below current commercial standards (IBM C4) of 100 μ bumps on 250 μ pitch.
- Front-end chips are connected together using a high density interconnect, typically a Kapton Flex circuit. An additional readout controller chip of some kind is normally used to coordinate the control and readout functions for all of the FE chips.
- Fast serial links are then used to transfer clock, control, and data on and off the module.
- The result is an object that provides active coverage over a 5-10 cm² area, is subdivided into roughly 50K detector elements, consumes several watts of power, and weighs only about 3 grams.

Example of early ATLAS prototype Pixel Module:

Module with flex hybrid and controller chip on PC board



Sensor

ICs

- Active area is 10cm^2 , 46K channels, 16 FE on sensor substrate, and MCC chip.

Radiation effects on silicon sensors and micro-electronics

Sensors:

- Standard silicon sensors are made from high-resistivity silicon material (few $K\Omega\text{-cm}$), which can be depleted with moderate bias voltages to rapidly collect the charge deposited by ionizing tracks. Typical depletion voltages for 300μ silicon are about 100V, and collection times for n^+ implants (electrons) are about 10ns.
- Under irradiation, defects are created in the silicon lattice. These defects are not related to ionizing dose, but to displacement damage where atoms are moved around in the lattice. Displacement damage (also known as NIEL, non-ionizing energy loss) is tabulated in 1MeV neutron equivalents, using “hardness factors” to correct for other particle types and energies.
- These defects create leakage current at a rate which is now very well-understood. Leakage current has strong temperature dependence (a factor 2 for every 8C).
- Additional p-type defects affect the depletion behavior, causing type inversion (n-bulk becomes p-bulk), and increasing the depletion voltage. The behavior of these latter defects as a function of time and temperature after irradiation is complex, with initial beneficial annealing (time constant of about 1 week at room temperature), followed by so-called reverse annealing (time constant of months at room temperature).
- Heavily irradiated sensors are operated cold to reduce leakage current and to suppress reverse annealing, typically range of -10C to 0C is optimal.

Microelectronics:

- CMOS electronics devices operate by controlling carriers flowing in very thin (nm) channels, using gates separated by very thin oxide layers (5-15nm). The only significant source of radiation damage is ionization damage to the various oxide (SiO₂) layers used to isolate gates and to isolated transistors from each other.
- Bipolar devices are more complex, and suffer from both ionization damage to oxide layers and from displacement damage to the transistors themselves.
- Some strip applications use bipolar transistors in the front-end design (e.g. ATLAS strip readout) to achieve optimal noise and speed performance, but almost all silicon readout is done using pure CMOS processes.
- The traditional approach to rad-hard CMOS design involved working with specialized foundries with “hardened” processes developed primarily for military applications. These processes have been 1.2 μ or 0.8 μ , with 2-3 metal layers. Equivalent commercial processes, even with special layout techniques, could not tolerate radiation doses much beyond about 100KRad.
- However, it has been realized for some time that once the gate oxide becomes thin enough (much less than 10nm thick), virtually all of the damage created by ionizing radiation will “anneal” extremely rapidly due to quantum tunneling effects, leading to intrinsically radiation-hard gate oxides. The 0.25 μ CMOS processes were the first commercially available which operated completely in this regime, providing a new approach to radiation-hard electronics.

The ATLAS Inner Detector (2T Solenoid):

Outermost system uses gas-filled 4mm straws

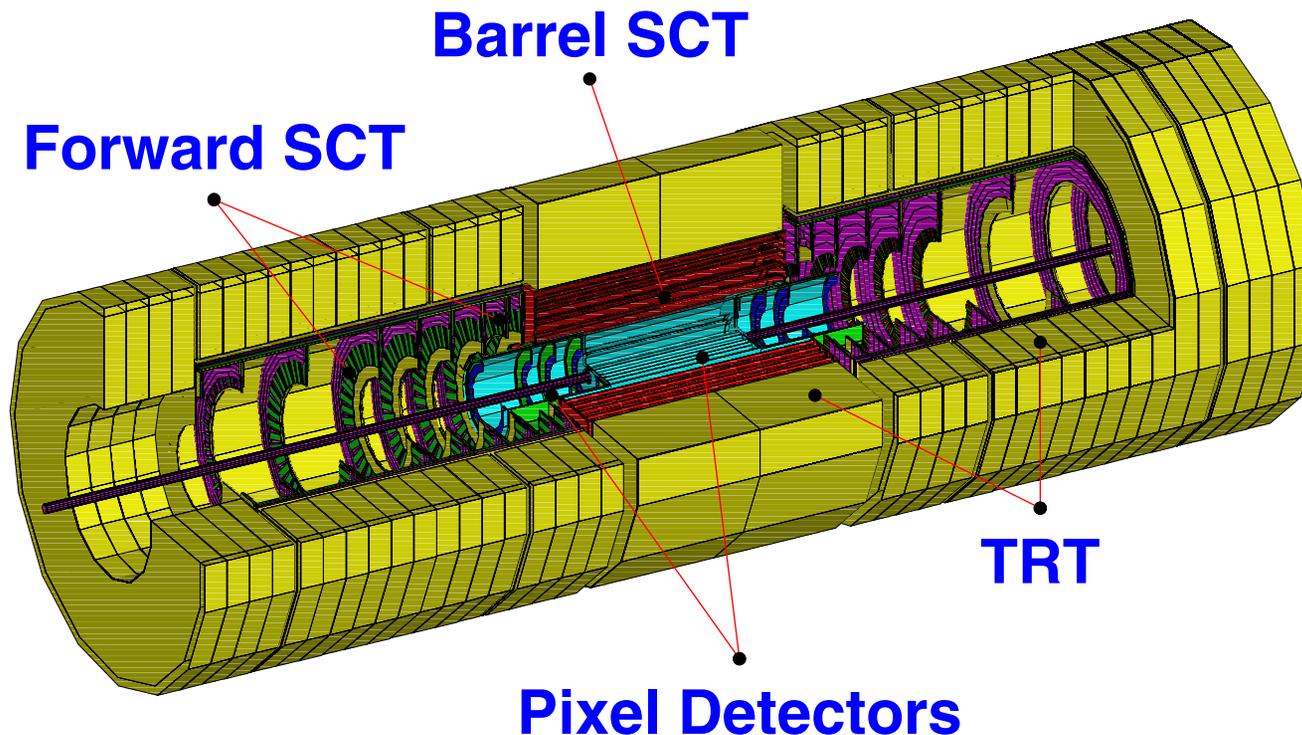
- There are 420K electronics channels, and a TR radiator supplies particle ID.

Intermediate radii contain a silicon strip tracker

- Four barrel layers and 9 disk layers contain 61 m^2 of silicon with 6.2M channels

Innermost system is pixel tracker

- Three barrel layers and 3 disk layers contain 1.8 m^2 of silicon and 85M channels



Pixels address many vital tracking issues at LHC:

Radiation Damage:

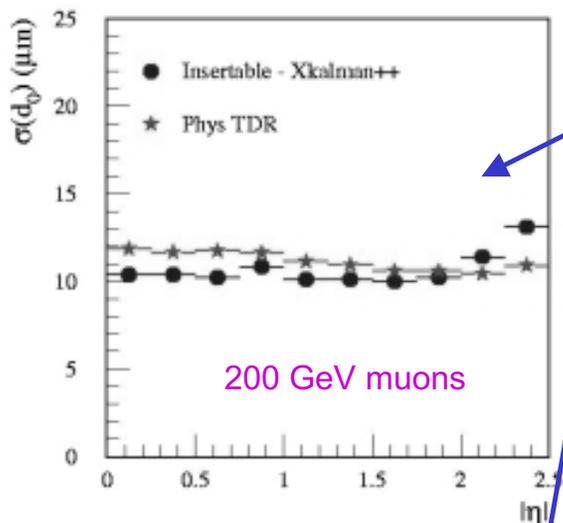
- LHC radiation levels prohibit operation of silicon strip detectors below radii of about 25cm. Limits arise from parallel noise from sensor leakage current, as well as signal loss from charge trapping and partial depletion of sensor.
- Pixels reduce leakage and improve signal/noise ratio per channel relative to strip systems by their high segmentation. In ATLAS, expect 10Ke signal at the end of lifetime. Leakage is expected to be about 30nA/pixel, and noise should be less than 400e, for a lifetime dose accumulated by electronics of 30-50MRad, and by sensors of 10^{15} 1MeV neutron equivalent.

Occupancy and Timing:

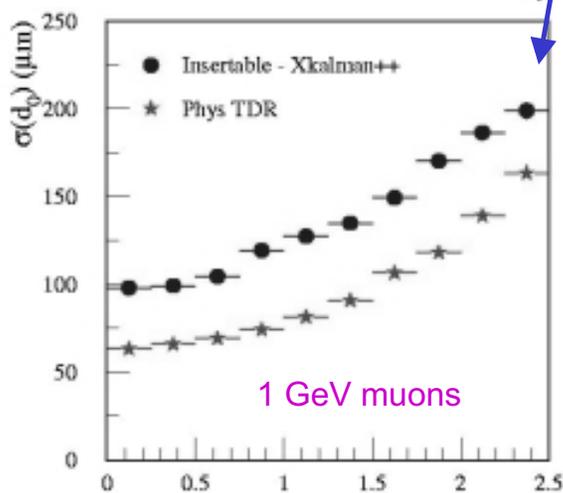
- Small cell size ($50\mu \times 300\mu - 400\mu$) of pixel detector yields low occupancy of no more than 5×10^{-4} per pixel per crossing at 4-5cm radius. A strip system would have an occupancy at least 100 times larger.
- Timing is very challenging, and pixels have no advantage here. Dominant effect is timewalk in the front-end (preamp and discriminator), where charges near threshold have additional delays due to the finite preamp risetime and discriminator speed. Reaching values of 20ns for charges in the range of 4Ke - 100Ke with a current budget of only about $20\mu\text{A}$ per pixel is proving to be very difficult, despite the relatively small detector capacitance.

Performance (examples from ATLAS):

- Based on prototypes, simulations predict $\sigma(r\phi) \approx 10\mu$ and $\sigma(z) = \approx 50-100\mu$
- This leads to the following simulated impact parameter performance (GEANT):



200 GeV muons



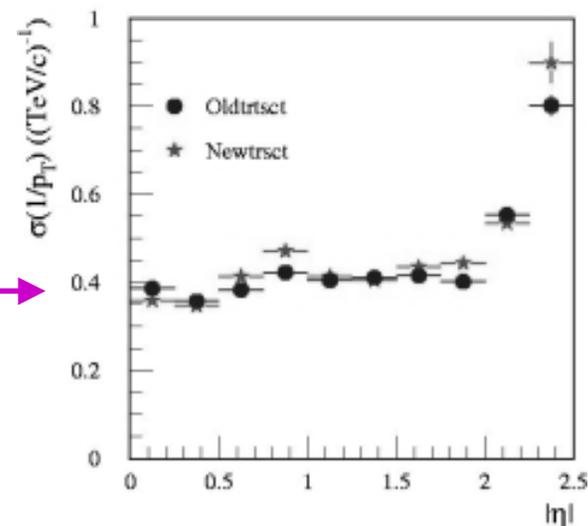
1 GeV muons

Transverse impact parameter resolution for muons with $p_T = 1$ and 200 GeV: now

$$\sigma(p_T) \approx 10 \oplus \frac{98}{p_T \sqrt{\sin \vartheta}}$$

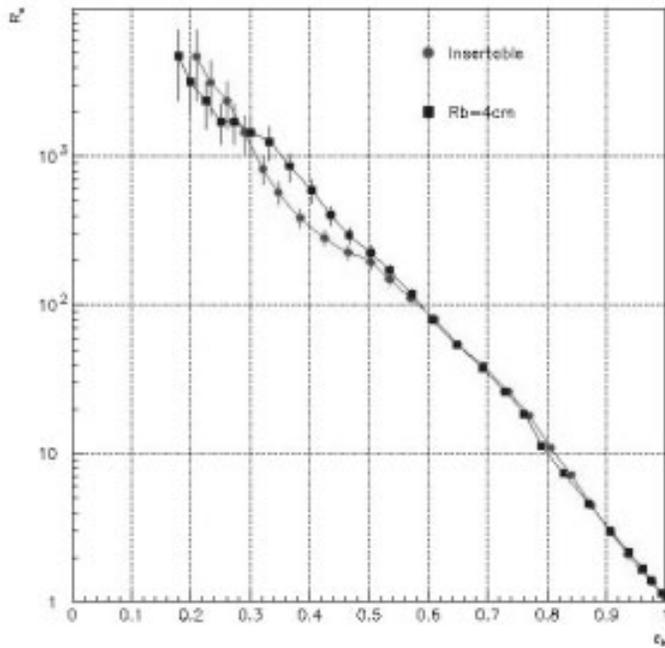
Main difference due to increase of beam pipe and B-layer radius: B-layer moved from 4 to 5 cm.

Dependence of the p_T resolution on SCT and TRT geometries for muons with $p_T = 200$ GeV

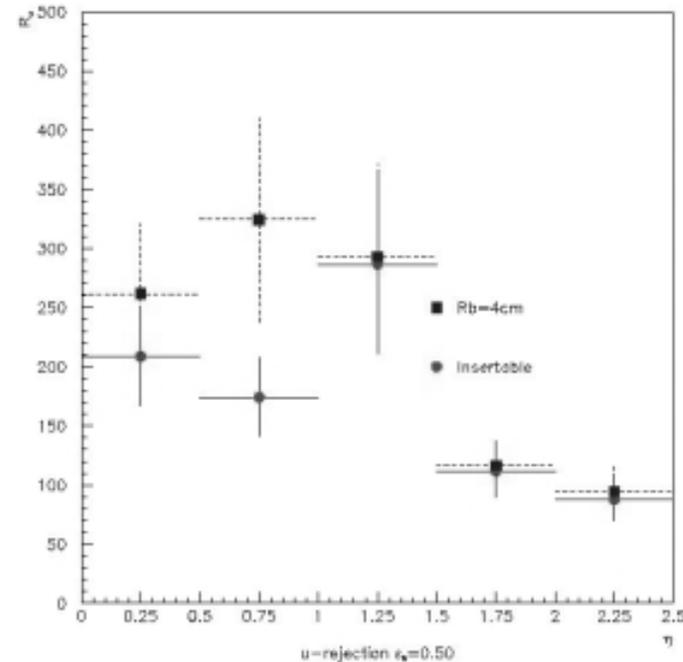


- Significant loss in resolution at low P_T is due to material (about 7% X_0 at $\eta=0$).

- And to the following simulated b-tagging performance (GEANT):



Rejection for u-jets vs efficiency for b-jets



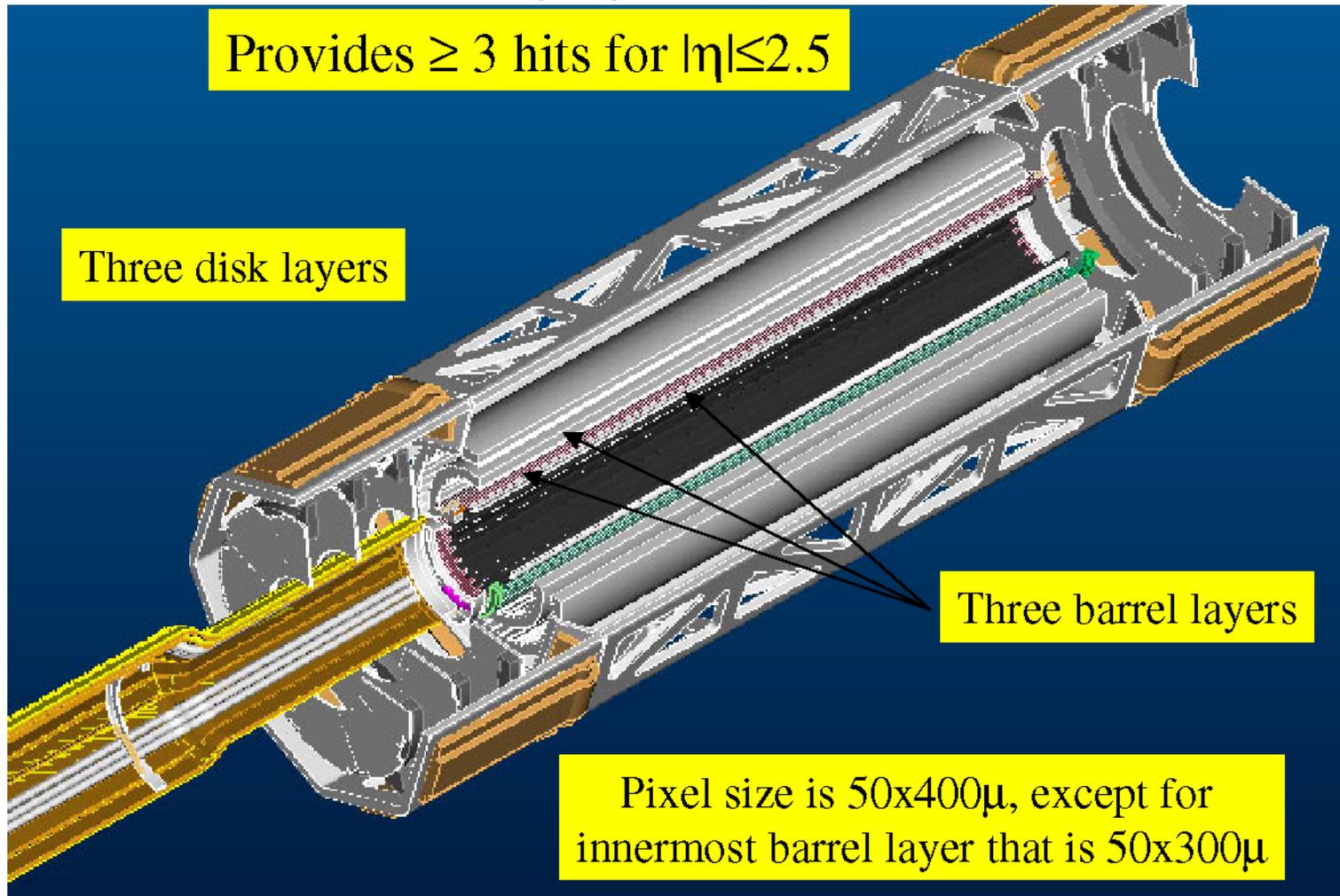
R_u for $\epsilon_b = 50\%$ vs $|\eta|$

Layout	R_u for $\epsilon_b = 50\%$	R_u for $\epsilon_b = 60\%$
Insertable	190 ± 20	89 ± 6
B-layer R = 4.13 cm	230 ± 25	88 ± 6

- B-tagging performance is evaluated for 400GeV Higgs decaying to b-quarks and non-b-quarks without pile-up. Studies done with full 10^{34} pileup indicate that rejection of u-jets deteriorates by about a factor of 2 for $P_T(\text{jet}) < 100$ GeV, and stays the same for higher P_T jets.

ATLAS Pixel Detector

- System is based on three barrel layers and three disk layers, providing 3 pixel hits over the inner detector tracking region of $|\eta| < 2.5$.

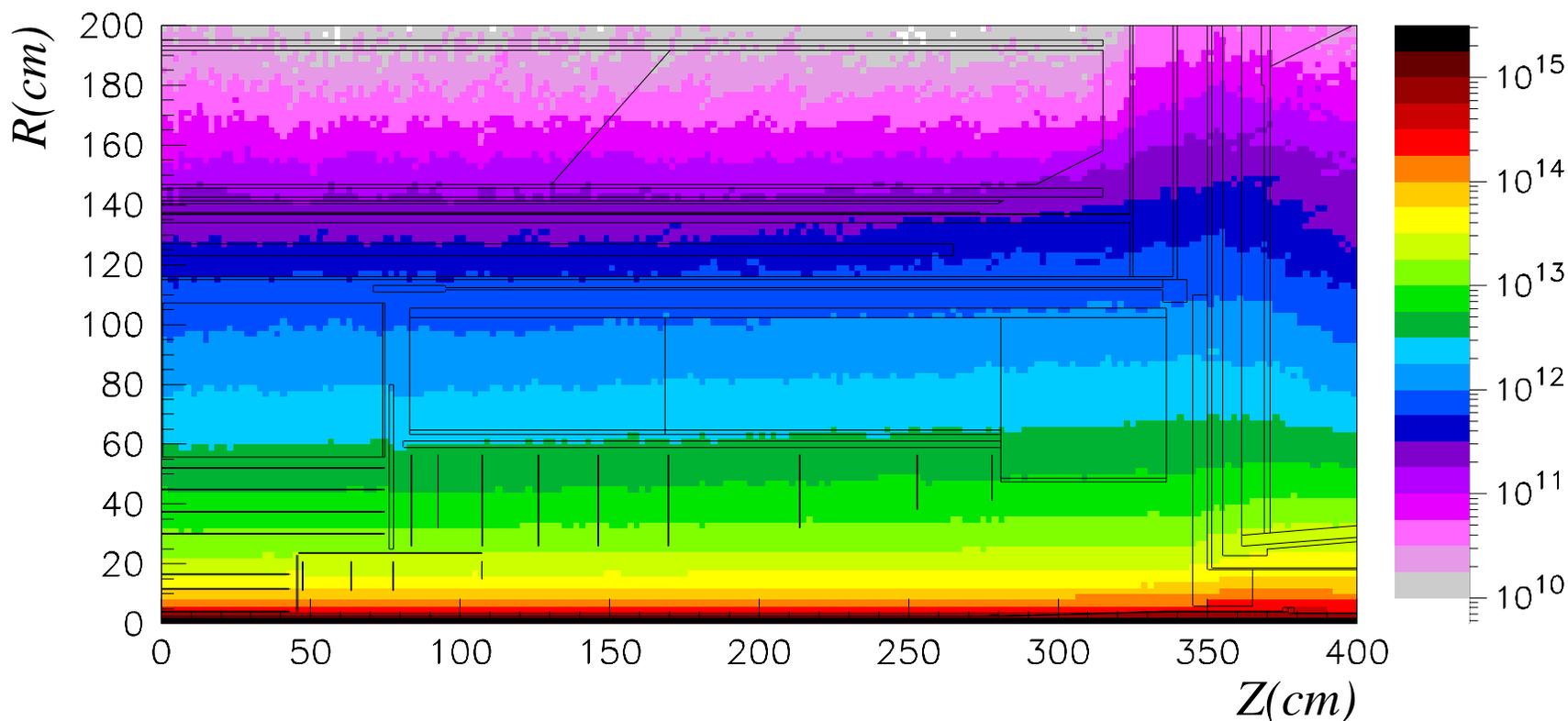


- Physical size of system is roughly 1.6m long, with 0.2m radius. Innermost layer is at 5cm radius, and worst-case power consumption is about 4000A at 2V.

Radiation in ATLAS Inner Detector

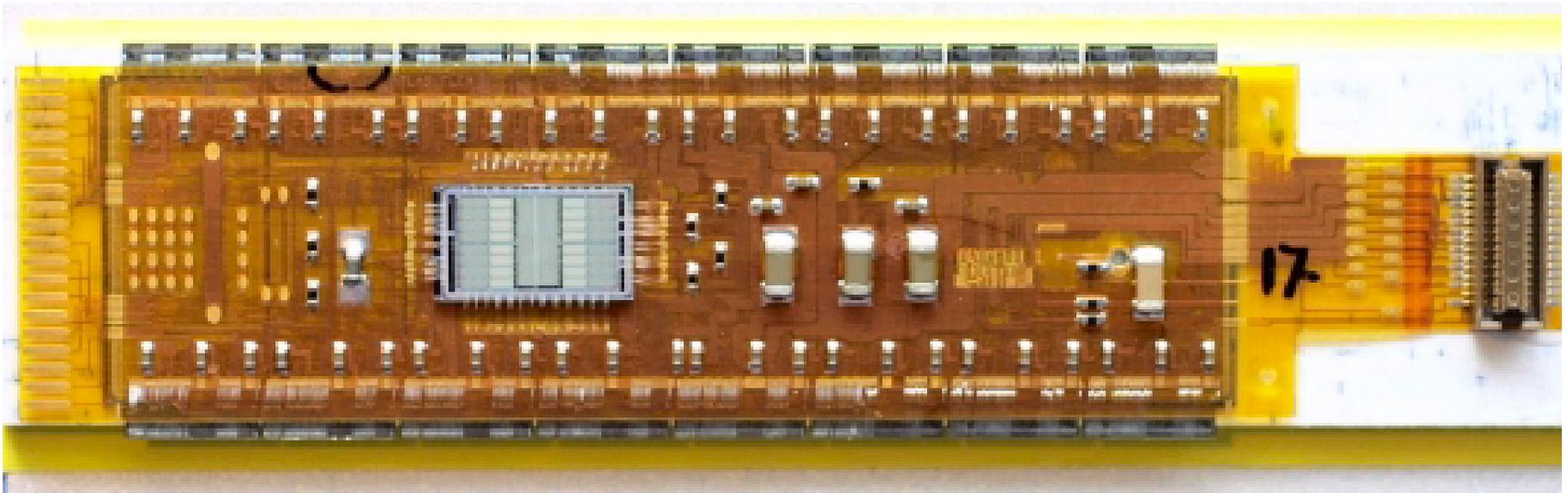
At small radii, where the pixel tracker lives, the total radiation dose is dominated by charged hadrons from the underlying events (true for all silicon layers in ATLAS)

- Fluence of charged hadrons through the ATLAS Inner Detector per cm^2 per year at design luminosity. Outer layers see $\approx 10^{14}/\text{yr}$, inner layer sees $\approx 4 \times 10^{14}/\text{yr}$



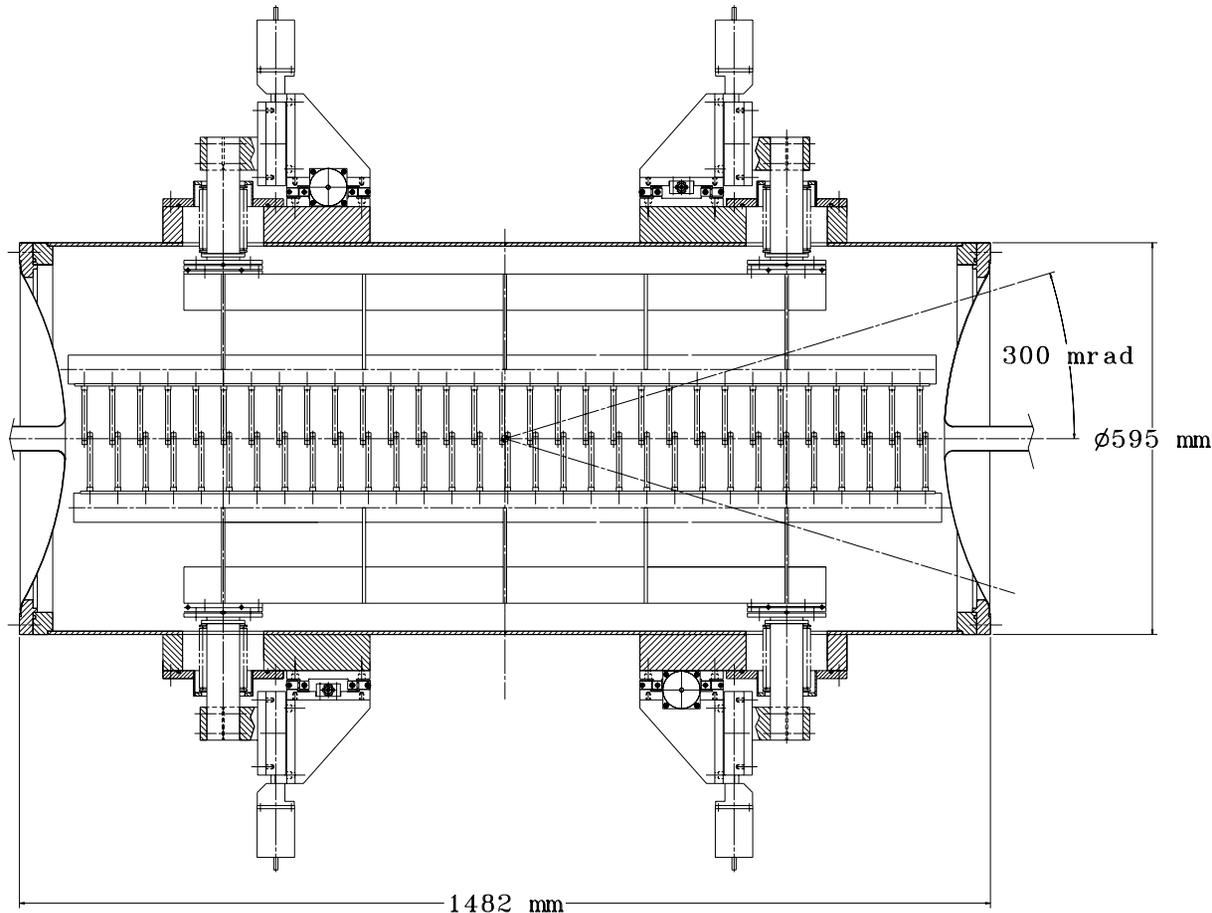
Module and electronics design:

- Electronics is based on a $50\mu \times 400\mu$ pixel, arranged into 18 columns of 160 pixels each.
- Front-end chip contains DACs needed to adjust biasing, digital timewalk correction, internal decoupling, and measurement circuit for critical capacitors.
- Charge information is provided by using a preamplifier with linear Time-over-Threshold (TOT), and measuring the discriminator pulse length using the 40MHz beam clock.
- A Module Controller Chip provides event building, and command and control functions for the module.
- Prototype module shown here includes temporary test connector:



The BTeV Pixel Detector (1.6T Dipole)

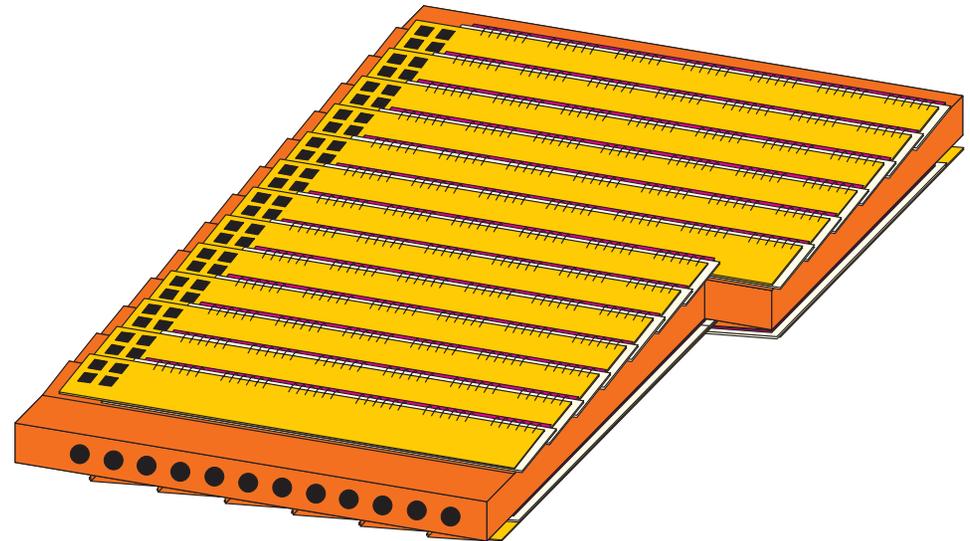
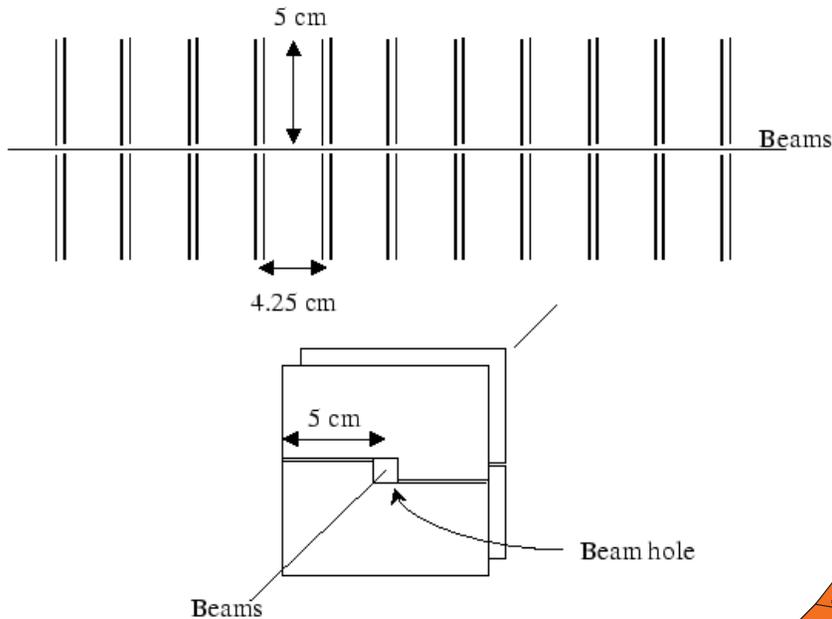
- Detector is placed very close to interaction point, and consists of 31 planes of pixel modules, 0.6 m^2 , for a total of roughly 30M pixel channels, with very small ($\pm 6 \text{ mm}$) cut-outs for the beam to pass through.



Entire pixel system is placed inside the machine vacuum, in a large vacuum tank, in order to minimize material and distance to interaction point.

- Special features include goal of performing complete first level trigger based on secondary vertex reconstruction for every 132ns crossing (heavily pipelined).

- The trigger requirement implies moving all zero-suppressed data off of the detector (roughly 1 TB/sec data rate !)
- Many individual modules are supported on an L-shaped support, which also provides cooling. Two plates make up a plane that surrounds the beam region:



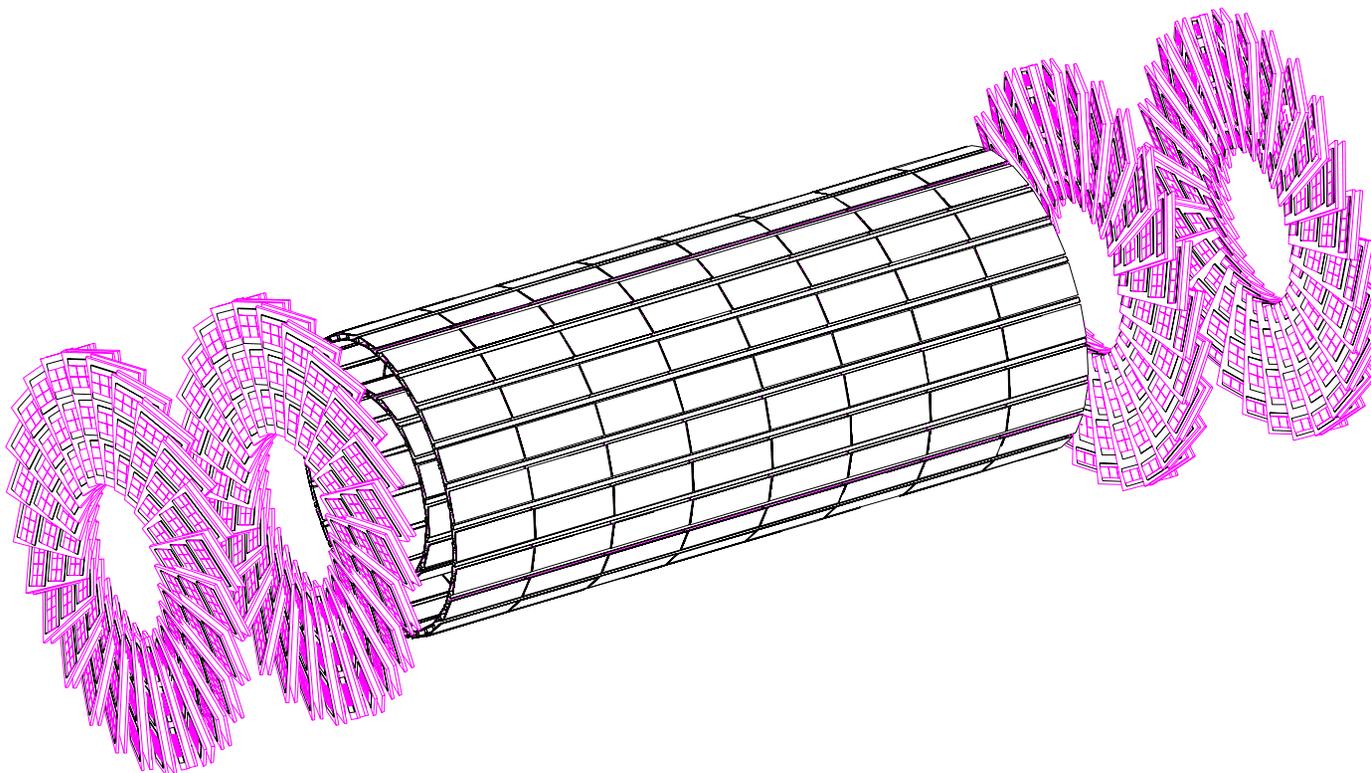
- Individual modules are mounted on two sides of a carbon-based cooling structure, and consist of roughly 5 readout chips on a common 5 cm² substrate.

Module and electronics design:

- Electronics based around a similar pixel to ATLAS ($50\mu \times 400\mu$) to ease prototyping of sensors.
- Design uses 3-bit ADC to digitize charge information directly in each pixel. Presently, all 8 thresholds are individually programmable to allow non-linear definition of the ADC values.
- Since this detector forms the basis for the first level trigger, all hit data must be transmitted off-chip. The plan is to use LVDS and wires to transmit the data a small distance into a lower radiation area, and then to transmit using fast optical links.
- Modules are made up of a single row of 5-7 FE chips connected by a high density interconnect, built from Kapton. Readout controller chips are used at the end to send high-speed data streams off detector.

The CMS Pixel Detector (4T Solenoid)

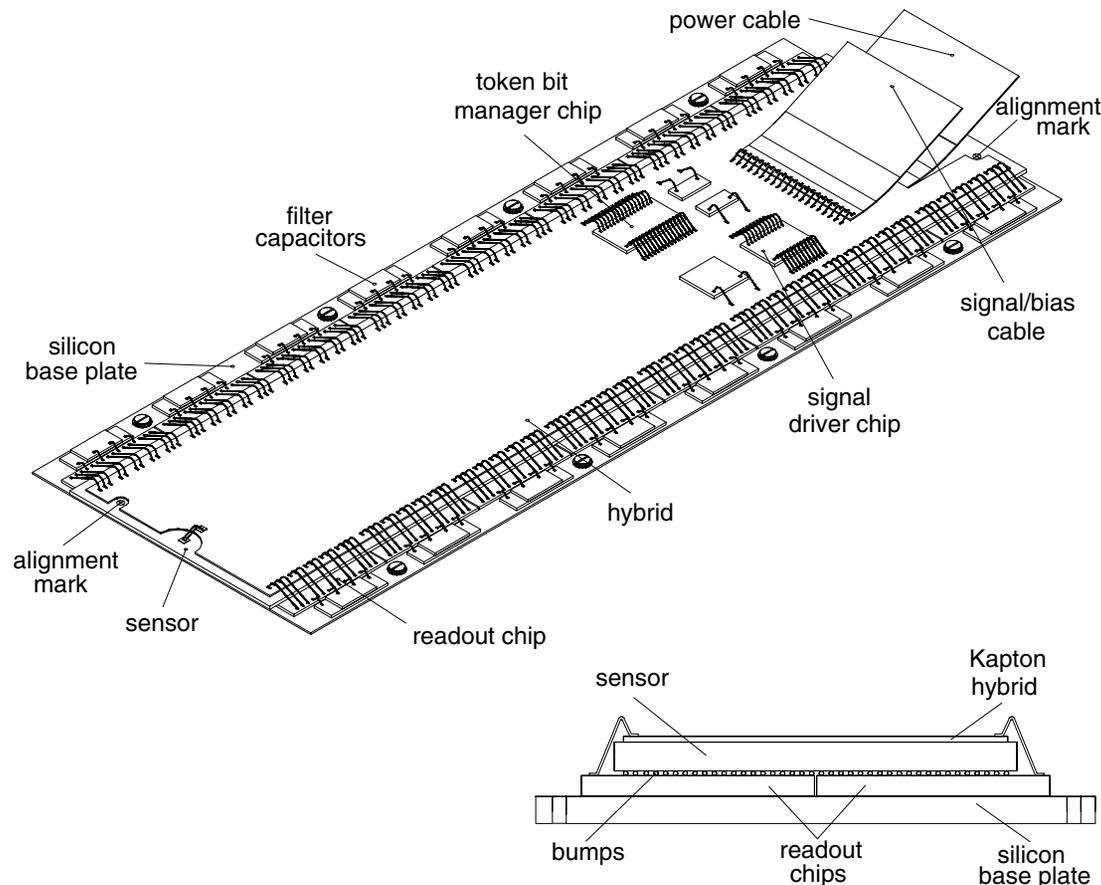
- The CMS pixel detector is a two layer system, with two barrels at 4.3 and 7.2 cm radius, and two disks at each end.
- A third layer would be added later at a larger radius of 11cm
- There are about 45M pixels in the two layer system:



- The system operates in a 4T magnetic field (initial Lorentz angle of 30 degrees in barrel, turbined layout in the disks). It relies on $150\mu \times 150\mu$ square pixels with significant charge sharing to provide good resolution in both directions.

Module and electronics design:

- The front-end produces an analog signal representing the input charge. This signal is stored in the chip periphery and transmitted over an analog optical link for digitization in the off-detector electronics.
- Each Readout Chip (ROC) contains 52 rows of 53 pixels each. A module is constructed by bump-bonding 16 ROCs to the sensor substrate. Information is transmitted off the module using two control and driver chips:



Pixel Module is roughly 66mm long by 18mm wide, with an active area of 10cm²

Major Technical Challenges

Sensors: critical issue is radiation hardness.

- Use n+ in n-bulk design to allow partially depleted operation after type inversion. The n+ implants require isolation to avoid shorting by electron accumulation layer. Standard designs use high-dose p+ stop implants to isolate pixels. They produce high-field regions after significant irradiation, leading to breakdown.
- ATLAS and BTeV use p-spray approach (uniform low-dose p implantation step, which is overcompensated by n+ pixel implants). This eliminates breakdown even after irradiation to 10^{15} fluences.

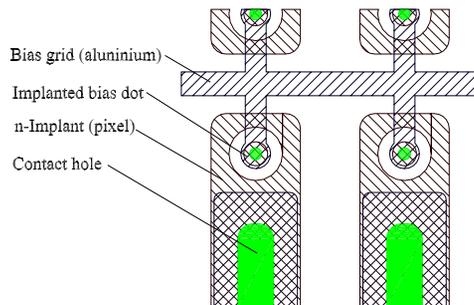
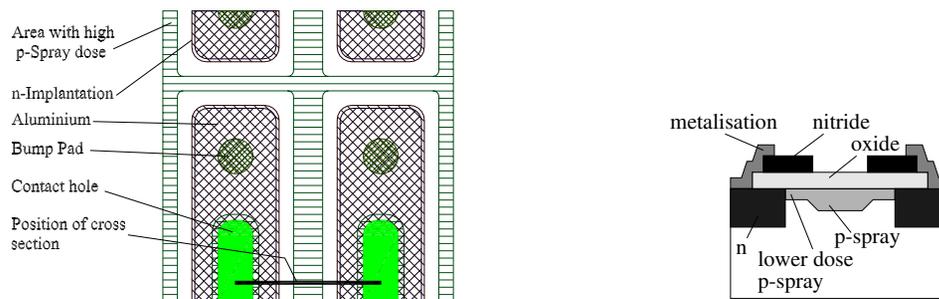


Fig. 10. Design detail of the bias grid in the second sensor prototype.



P-spray approach also allows implementation of punch-through bias net which allows holding implants at a fixed potential.

This permits I/V checks during wafer-testing and also prevents implants from floating to bias potential in case of bump-bonding defects.

- In order to maximize the signal after irradiation, detectors must be operated at highest possible bias voltage to deplete as much silicon as possible and to minimize trapping effects. ATLAS uses 600V, which then produces almost 1W of power dissipation in sensors due to leakage current at end of lifetime.

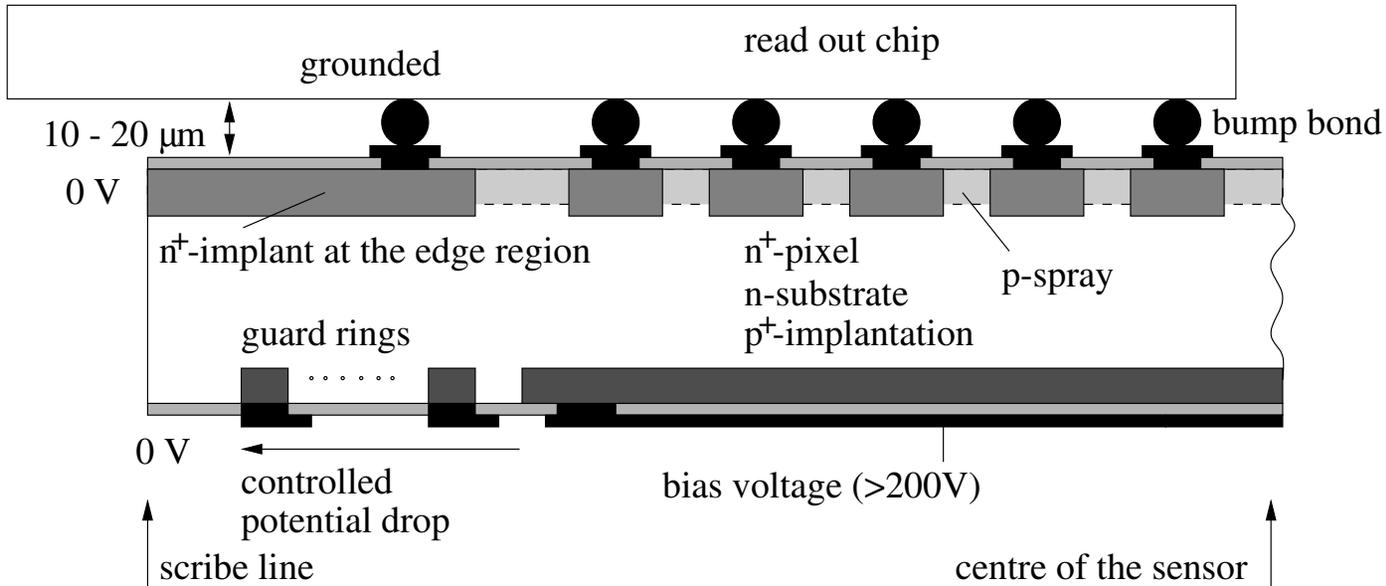


Diagram showing guard geometry near edges of module, designed to operate safely with bias voltages of beyond 700V.

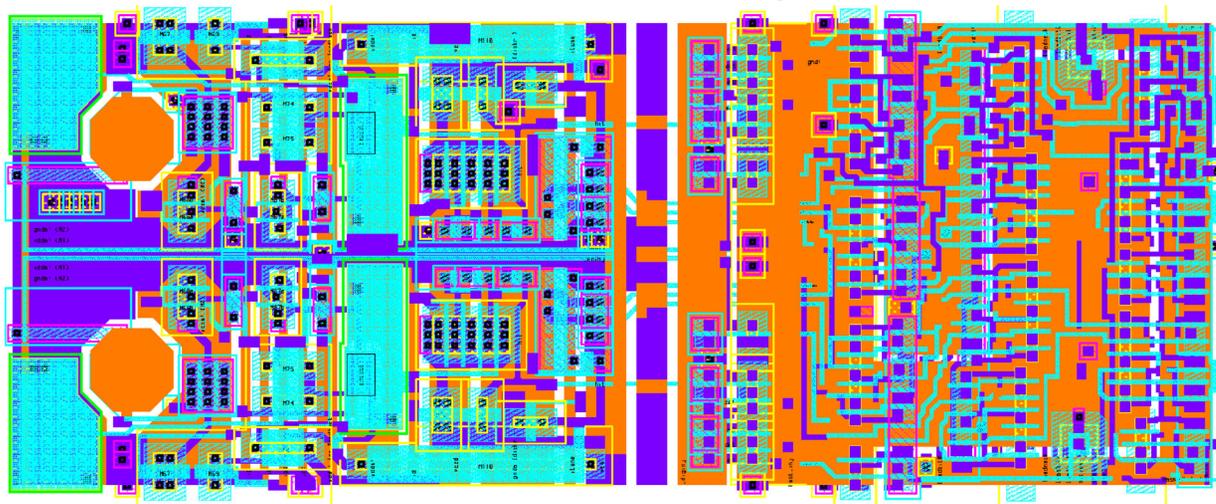
- The sensors must be kept cold to control leakage currents and reverse annealing, requiring optimization of mechanical structure for low temperature operation.
- Coverage of regions between electronics chips on module requires some special attention. In simple hybrid case, ATLAS chose to extend pixels in long direction, and to create additional “ganged” pixels above the top of the readout chips. This provides coverage at cost of additional noise and occupancy in edge pixels.

Electronics:

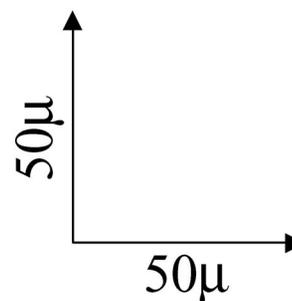
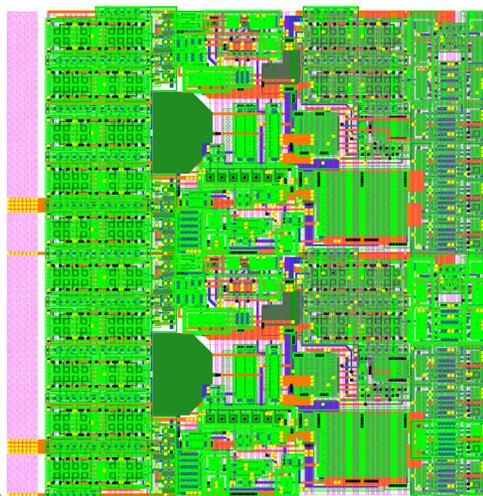
- Radiation hardness has proven to be difficult to achieve. Initial path pursued by ATLAS and CMS was to use traditional rad-hard vendors (Honeywell SOI and ATMEL/DMILL). Both were 0.8μ rad-hard SOI processes. However, the density of these processes is rather low . In addition, they represent a small specialty market, so the processes are expensive, poorly controlled, and slowly evolving due to the limited market size.
- BTeV switched to the alternative deep-submicron path about two years ago, ATLAS has switched this year, and CMS is likely to switch next year.
- The advent of accessible (available to small-scale customers for multi-project and engineering runs) 0.25μ CMOS processes has changed everything. These processes, with a gate oxide thickness of 5-6nm, show the very tiny threshold shifts expected when quantum effects allow almost all of the trapped charge created in the MOS gate oxide by irradiation to tunnel out very rapidly. VT shifts of order 50mV are observed after doses of 30MRad, far lower than those seen in the traditional rad-hard processes.
- To reap the benefits of the rad-hard gate oxide in 0.25μ processes, it is necessary to follow some special layout rules, in particular to make only annular NMOS (to prevent any leakage path between drain and source), and to guard-ring different NMOS from each other. These rules do affect the designs, forcing the use of larger NMOS than usually needed (increased power consumption and current spikes), and preventing the use of small W/L NMOS in analog designs.

- These processes are very high-volume commercial products, and as such are cheap and highly stable and reproducible. The smaller feature size also leads to much more compact designs, even using the rad-tolerant layout techniques.
- Comparison of recent ATLAS front-end+control designs in DMILL and 0.25 μ :

Two pixels
(analog)
in *DMILL*



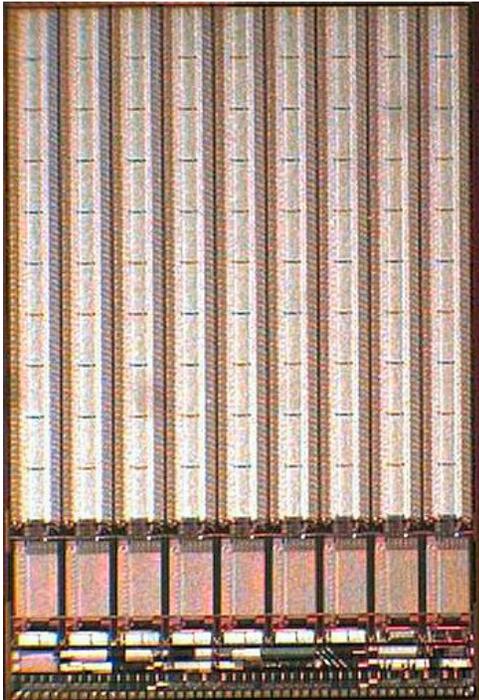
Two pixels
in 0.25 μ



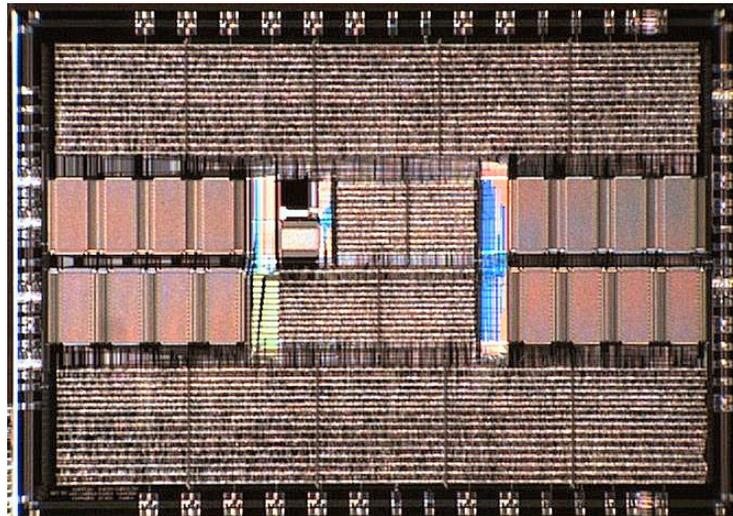
- Small 25 μ x50 μ region on the left contains 10 SEU-tolerant latches for trim DACs.

- Greatest design challenges are in front-end. To operate effectively at the end of sensor lifetime, need 3-4Ke thresholds. For these thresholds, hits should already be associated with the correct beam crossing, which requires about 20ns maximum timewalk for LHC. The noise and threshold dispersion must also be low enough to allow operation with low noise occupancy at these thresholds. In ATLAS, the requirement is for the combined noise and dispersion to be less than 400e. The total current budget for the analog front-end is typically around 10-25 μ A per pixel, and achieving a 20-30ns peaking time with roughly 400fF load and low bias current is very challenging. In deep-submicron processes, low power designs require operating essentially all transistors in the sub-threshold region, where they are exponentially sensitive to V_T shifts and to V_T matching.
- Significant issues arise in trying to prevent coupling between fast digital readout in the back-end of each pixel and the preamplifier in the front-end of each pixel. Depending on the bump-bonding technology, the sensor has a conductive pixel implant that sits 8-20 μ away from the electronics which traverses from the pixel digital back-end to the pixel analog front-end. Present chips do their best to shield the sensor from any digital pick-up by carefully covering all active digital circuitry with as much metal as possible. Although deep-submicron processes have many more metal layers, and provide stacked vias, they also have maximum fill fractions in any given layer, so a complete shield requires two metal layers to implement.

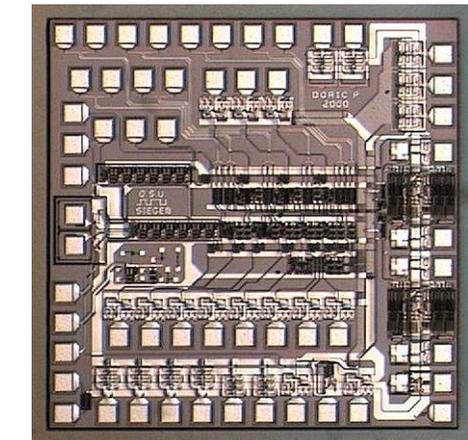
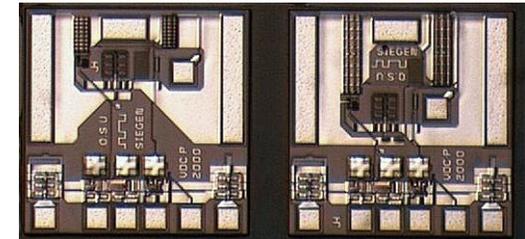
- To construct complete modules requires a whole chipset. For example, in ATLAS there is the front-end chip (16 per module), there is the module controller chip (one per module), and there are two chips to support the opto-link operation (one DORIC, one or two VDC per module). This requires significant engineering resources.
- Chips from a recent ATLAS DMILL engineering run are shown here:



FE-D2



MCC-D2



DORIC and VDC

- Distance to nearest elements in power supply system (e.g. regulators) can be large (10m in ATLAS), requiring careful power management, using smart decoupling and transient clamping inside chips, high-density ceramics on hybrid.

Interconnections:

- In hybrid pixels, major interconnection problem is bump-bonding. Present detector designs rely on 50μ pitch, which is very demanding. Very few vendors are willing to do this, and they are not large, commercial firms (with the exception of Seiko who provided excellent prototypes before the service was discontinued).
- Connecting chips within a module, including power distribution and signal bussing, is challenging. Present designs use Kapton hybrids, typically $25\text{-}50\mu$ base material with 25μ cover layers, and about $15\text{-}20\mu$ of Copper in traces to cope with 1A current distribution with modest (50-100mV) voltage drops.
- Achieving full coverage in each pixel layer, despite large dead area of each pixel chip which is allocated to buffering and housekeeping functions, is challenging. It requires large overlaps and very tight mechanical tolerances. ATLAS modules are mounted with 1mm clearances, and module envelopes that forbid even 0402 components in many regions of Flex Hybrid. The large overlaps also increase the material budget significantly.
- Bringing large amounts of current into and out of small pixel detector volume without introducing excessive heat or excessive material is challenging. Cables must be made from Aluminum twisted pair, and any optimization gives significant material and power dissipation. In ATLAS, dissipate about 2KW in the last 1-2m of services. Making high quality connections with Aluminum tapes or wires is also challenging. ATLAS is investigating “micro-welding” techniques used for power devices, in which wire-bonding is done with several hundred micron wires.

Mechanics/Cooling

- Complete detector will dissipate 5-10KW in the tracker itself, and many more KW in the services. In ATLAS, dissipate about 10KW in tracker and another 10KW before reaching the first major patchpanels at 10m from detector.
- Pixel modules present an area load, and heat needs to be collected into cooling pipes by material with high thermal conductivity in all directions. This material also must have a low CTE to avoid introducing large stresses in attached modules over roughly 50C operating temperature range (+25C to -25C). ATLAS has chosen carbon-carbon material.
- Pixel modules themselves have materials with varying CTE, and it is essential to avoid attachment procedure introducing shear stress on the fragile bumps.
- Using a pure liquid cooling system requires significant amounts of fluid in cooling pipes, adding to the material budget. ATLAS has chosen evaporative fluorocarbon cooling to provide cooling margin and very low mass (essentially have only fluid film inside cooling pipes, which evaporates and uses latent heat to provide cooling).
- Need extremely low mass mechanical and cooling system, which will place modules to about 10μ , and yet will also support services for 4000A of DC current. Structure must have very low CTE to allow tracking module locations under thermal cycling from 25C assembly temperature down to -25C operating temperature for local supports.

Future Directions

There will be upgrades to detectors discussed here:

- Physics performance for b-tagging dominated by efficiency, material, and resolution in the innermost layer for LHC pixel detectors.
- The relatively small area of this layer (for example, 0.25m^2 in ATLAS) make upgrades feasible, and highly desirable given rate of technological progress. Expect an upgrade of innermost layer within about 3 years of start of running.
- In areas of mechanics and sensors, do not expect major technological advances.
- Exception could be the use of alternate substrates such as CVD diamond. Prototypes have worked to fluences beyond 10^{15} n equivalent (this is where the silicon signal deteriorates to the same value as the best diamond signals seen so far). Major advantage could be lack of leakage current, with elimination of need for sub-zero operation. However, rate of technological progress likely to impose lifetimes of order 10^{15} n equivalent in any case.
- Possibility of LHC machine upgrade to some multiple of 10^{34} and shorter crossing time (10-15ns ?). This might occur in 2012 or so, and would require very significant upgrade of complete tracking systems. Demands on pixel system would be extreme, perhaps increase of 2-3 in occupancy and 5 in radiation damage. Early studies of physics issues underway, and suggest that incremental luminosity only really interesting if detector capabilities stay almost the same.

Electronics:

- Present expectation with electronics built using 0.25μ process is that lifetime is roughly 50-100MRad. This is a good match to the lifetime of oxygenated sensors.
- Expected timing for an upgrade would be installation in 2009-2010. On the timescale relevant for producing this electronics, many commercial applications will be using a 0.13μ 8-metal or 0.10μ 9-metal CMOS process.
- This significant change could allow a factor 4-5 reduction in pixel area, or a significant increase in the functionality of a given pixel. However, there are many technological issues to study, including whether Single Event Gate Rupture will begin to play a role in the lifetime of the electronics.
- Matching and other analog design issues often prevent significant scaling of analog designs with feature size. With increased digital capability, designs will tend to cope with less-than-ideal analog performance using digital algorithms.
- Such processes will have gate oxide thickness of 2-3nm. Below about 3nm, quantum tunneling induces very large leakage currents, which will require new approaches to analog design.
- The supply voltage will be 1.0-1.3V, reducing the dynamic range of signals by a factor of two. The threshold voltage will only decrease from the present 500mV to about 350mV, so the ratio of supply to threshold voltage is dramatically reduced. This affects the speed of digital circuits, and more importantly, the dynamic range of analog circuits.

Interconnections:

- Size of modules, and therefore all mechanics issues, are driven by fundamental FE chip size. As industry moves into 300mm and then 450mm wafer sizes, price per unit area, and yield, of die will continue to improve. It might become possible to build much larger chips, with a more favorable active to total area ratio. This could potentially simplify the mechanics and reduce the overlaps (and material).
- Use of fine pitch bump-bonding is not presently commercial technology. This should improve over the next few years as mainstream industry catches up. It is possible that one could achieve 25-30 μ pitches with non-commercial processes.
- Present approach to module design based on Kapton hybrid and discrete passive components with large numbers of wire-bonds is very labor intensive and leads to highly fragile modules.
- Commercial electronics will soon be driving interconnect technologies to the level where they should be more useful for us. This might allow us to carry out a completely industrial production of pixel modules that are highly integrated.
- Already some experience in this direction due to explorations of MCM-D technology by ATLAS. This uses deposition of thin multi-layer interconnects on sensors using 50 μ pitch via and trace technology based on 7 μ Copper. Technology still too experimental for production use, but this should change.

Summary

- Pixelated silicon detectors based on hybrid designs appear to provide the best technology for tracking in high luminosity hadron colliders.
- This type of detector is in its infancy, with no complete detectors installed in hadron collider experiments yet.
- Such detectors are inherently somewhat massive due to the need to remove large amounts of heat generated over large areas, and the services required to bring power into and out of the detectors.
- The performance of pixel detectors is very strongly driven by the electronics.
- With the advent of rad-tolerant layout for commercial deep-submicron processes, we can build rad-hard electronics which is in the mainstream. This should allow us to follow “Moore’s law” and benefit from these extraordinary technical advances. However, we should not forget that no large scale system using this approach is yet operating in an experiment.