

# Status of Off-Detector Electronics

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**System consists of ROD, TIM, ROD Crate Backplane, and BOC (Back of Crate Optocard).**

- ROD is joint LBL/Wisconsin development (Jared)
- TIM us a UCL Development (Lane)
- Backplane is an Oxford/RAL development (Wastie)
- BOC is a Cambridge development (Goodrick)
- 3-day Review and Workshop at LBL Jul 31-Aug 2.
- First prototypes in fabrication, with plans for system testing in November.
- Emphasis for first tests is on SCT version, but pixel version involves (in principle) only firmware changes.
- Further information on all components:  
<http://www-wisconsin.cern.ch/~atlas/off-detector/off-detector.html>

## Status of ROD Prototype

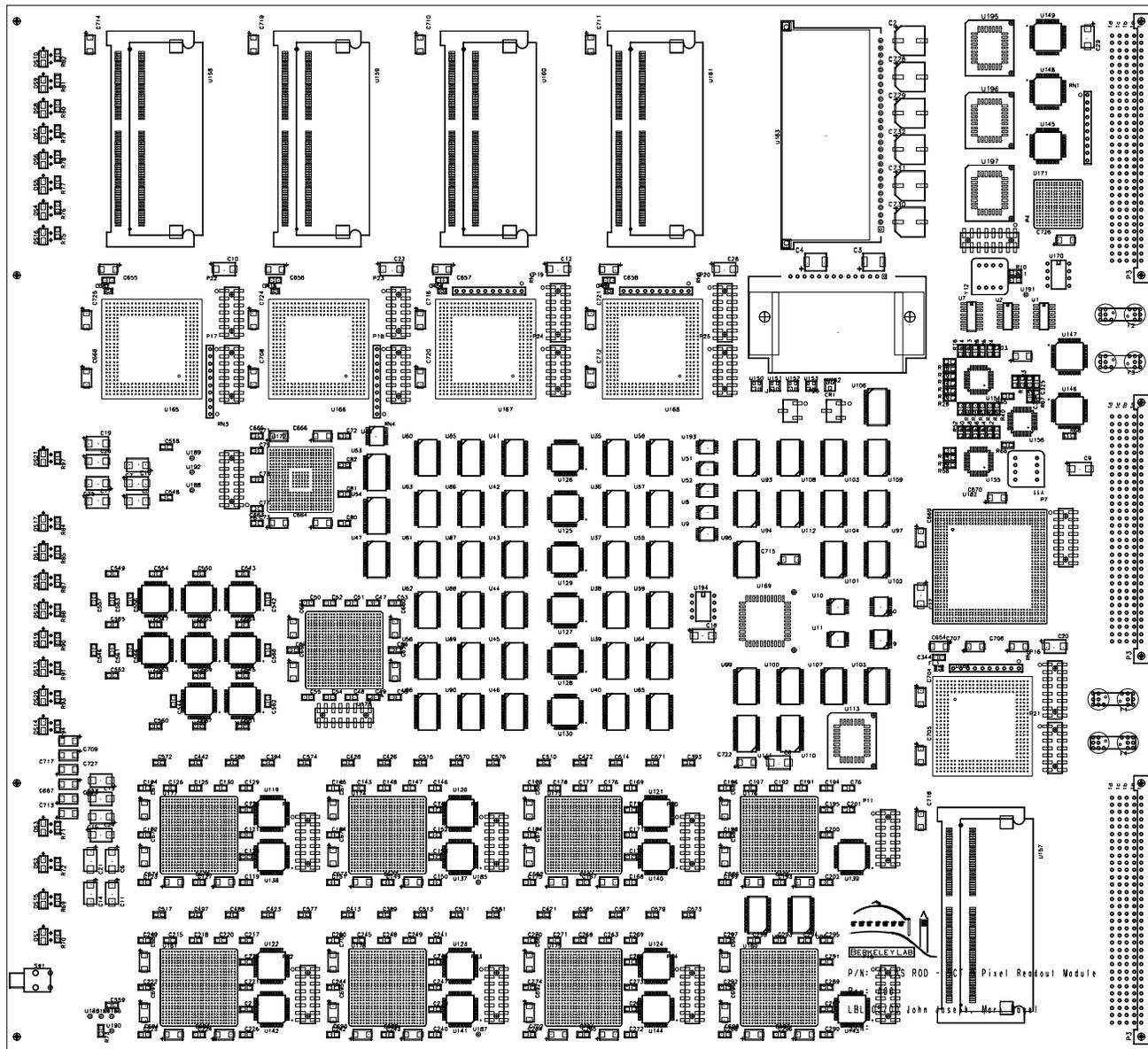
### Program for prototyping:

- Build significant number of prototype cards. Plan is for 12 total.
- Initial debugging and software testing to be done by designers at LBL. Fully tested boards would be delivered to SCT and Pixels.
- Users to perform evaluation of design during the first part of 2001. This should include testing with real modules (many...), as well as operation in the lab and in the test beam.
- Most likely, ROD community will need to design more complex data source for realistic “LHC-like” testing. Believe that something like a 1GByte memory is required to be able to play very long patterns through the ROD and test error recovery protocols, sustained bandwidth, etc. Of course, much of this has been or will soon be checked in simulation...

### Parts orders completed for 12 boards:

- Basic design is for 96-link SCT board, including loading of 2 of 4 slave DSPs. Each DSP has 32MB of memory.

# Layout of 9U VME board was completed in early August:



Board contains eleven FPGA in BGA packages and five DSPs in BGA packages, and has about 16K vias.

Layout is aggressive, including 12 layers with 5mil layer thickness to fit in VME crate rails, as well as microvias and fine pitch to route out of BGA regions.

Fabrication is proving difficult, but now trying a new vendor.

- First vendor delivered only a single board out of expected ten. Vendor seems able to test continuity and nearest neighbor shorts with flying probes, but very concerned about fragility of card under temperature cycling required for BGA mounting. Trying second vendor who has built comparable boards before.
- Hope to have partially loaded card in about 2-3 weeks for debugging.
- Design has now been through significant simulation. Complete data path from input to output simulated (but not using full FPGA routing information).
- Have written special VHDL for testing purposes, and there are also now three different “loopback” cards under construction. These cards plug onto the BOC connector and re-route input and output signals to allow more flexible capture and injection of data.
- Using these cards, expect to be able to perform all functional tests of ROD. However ability to generate and capture test patterns within the ROD itself is somewhat limited (handful of events at any given time).
- Have test environment written in LabWindows running on PC and talking to DSP evaluation board running skeleton of Master DSP software.
- Some delays, but looks possible to have some working boards in November.

## TIM Status:

- First boards fabricated and being debugged at UCL now.

## BOC Status:

- First boards now in fabrication. Difficulty is in obtaining opto-electronics parts (chips and arrays).

## Backplane Status:

- Design completed and in fabrication.

## Plans for Pixel Evaluation:

- Clearly, SCT will lead the way in the evaluation, including initial system testing in Cambridge this year, and operation in system test facility at CERN early in 2001.
- John Richardson will be working with LabWindows test environment created by Lukas at LBL, and adding some of the PixelDAQ functionality. We plan to perform initial evaluations of the card in the lab using existing modules and direct connection to BOC connector (no optical components).
- Basic problem is that there are far too few modules to carry out significant evaluation. In addition, we are still some ways from useful opto-link prototypes that could be included in evaluation.
- More planning required for next steps ! Need to evaluate prototype by mid-2001.