DSM ATLAS Pixel Testchip

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Contents

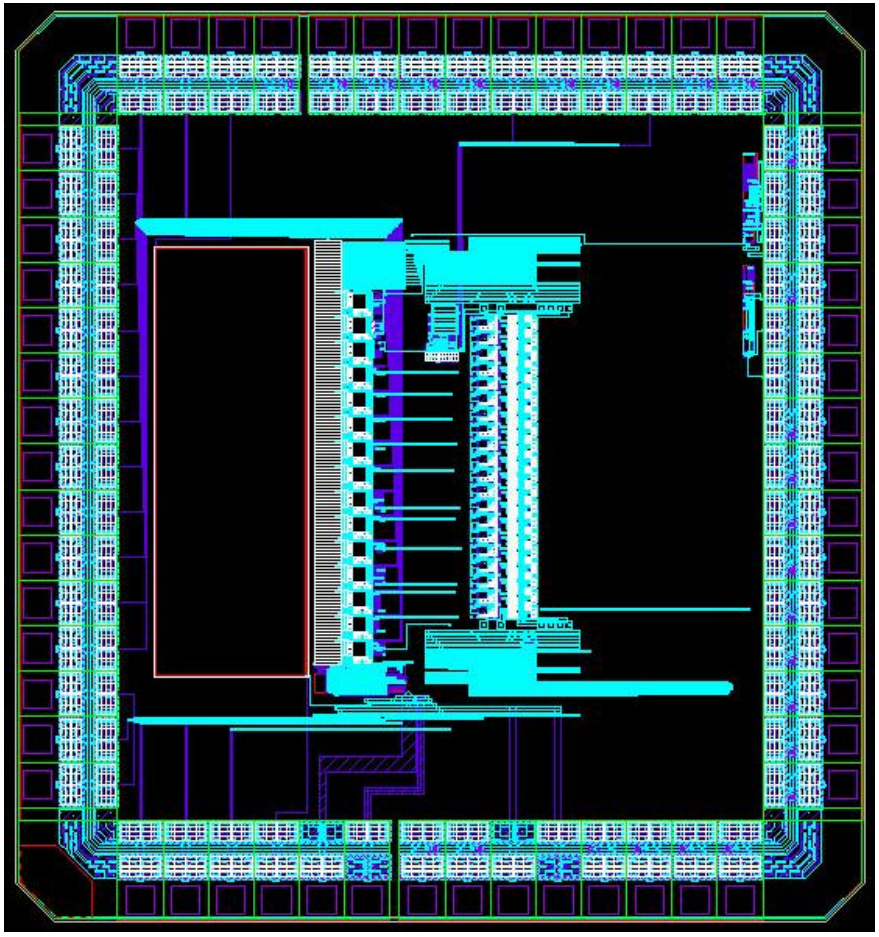
- Overview of circuit blocks on TSMC test chip
- Current reference
  - concept, schematic, layout, measurements
- Current DACs for bias generation
  - concept, schematic, layout, measurements
- Generation of calibration voltage

- Pixel control logic
- SEU flipflops

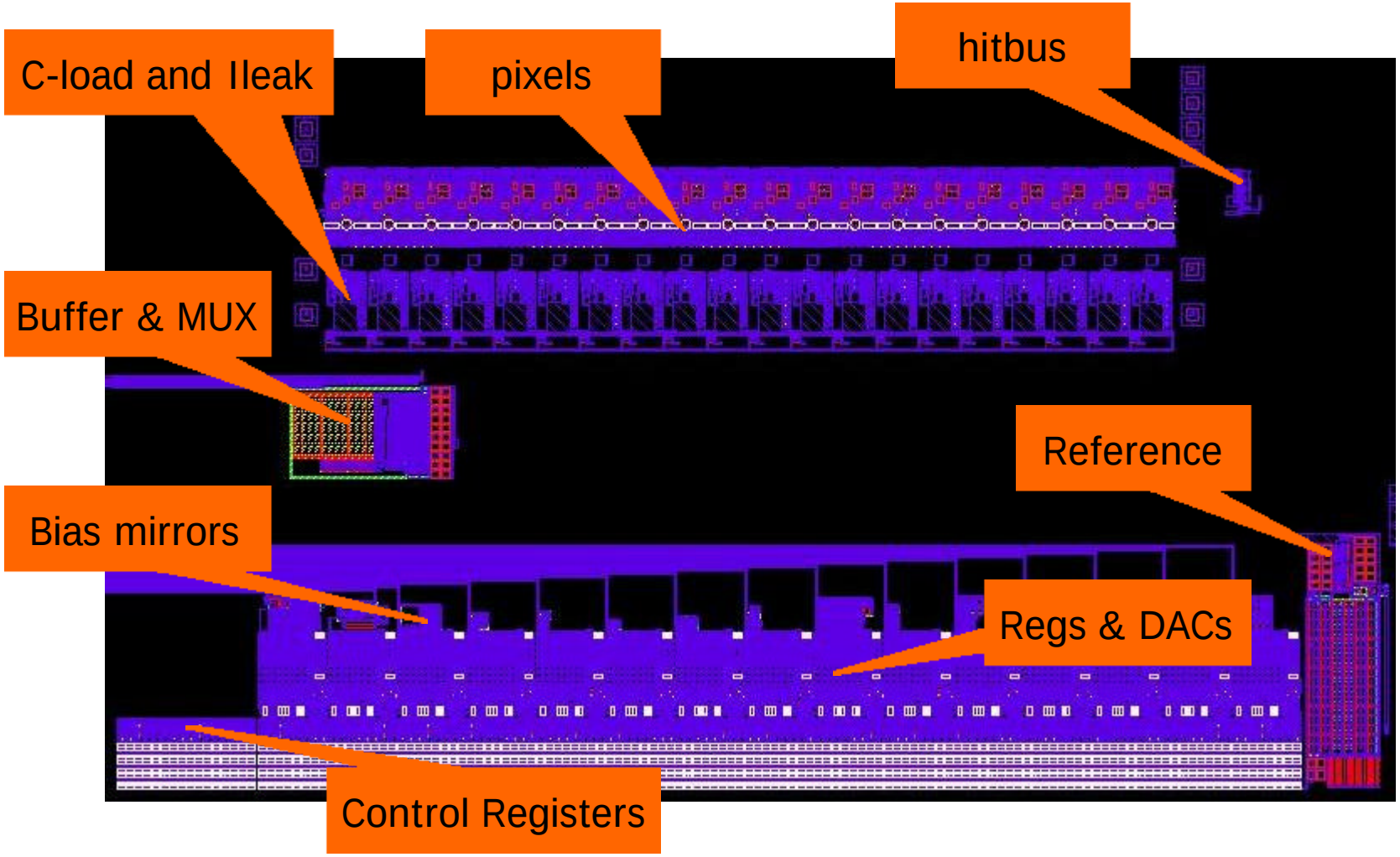
- Analog Pixel part
  - overview of different blocks - schematics and layouts
  - some measurements

TSMC Test Chip

- Chip Size = 2.8mm x 3.0mm , 58 wire bond pads, bonded to PLCC68 package
- Design operating voltages are VDDD = 2.0V, VDDA = 1.6-1.8V
- Chip contains
  - CMOS input / output pads, analog pads (with protections)
  - LVDS input- and output test circuits
  - Low voltage current reference
  - 8 bit current DACs to control all chip biases
  - current mirrors to scale current biasses
  - Generation of 8 bit calibration voltage
  - Analog buffer to monitor pulse shapes (4 ⇒ 1 MUX to select signal)
  - 8 bit 'ADC' to measure leakage current in every pixel
  - All global control bits use SEU tolerant FFs they can be read back any time
  - Large test capacitor array
  - pixel column with 20 pixels
  - Capacitive loads and leakage source on all pixels



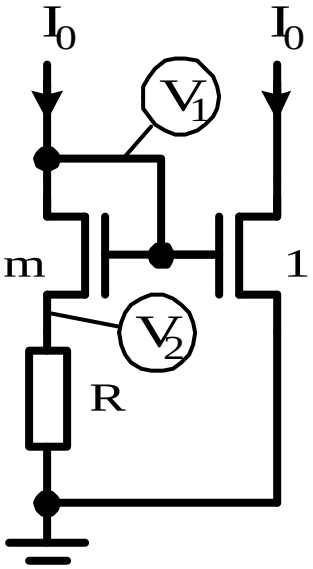
Core Layout


C-load and Ileak
pixels
hitbus
Buffer & MUX
Reference
Bias mirrors
Regs & DACs
Control Registers

Current reference - principle and layout

MOS in weak inversion:

$$I_D = I_{DO} e^{\frac{V_G}{nU_{Th}}} e^{\frac{-V_S}{U_{Th}}}$$



$$I_0 = mI_{DO} e^{\frac{V_1}{nU_{Th}}} e^{\frac{-V_2}{U_{Th}}}$$

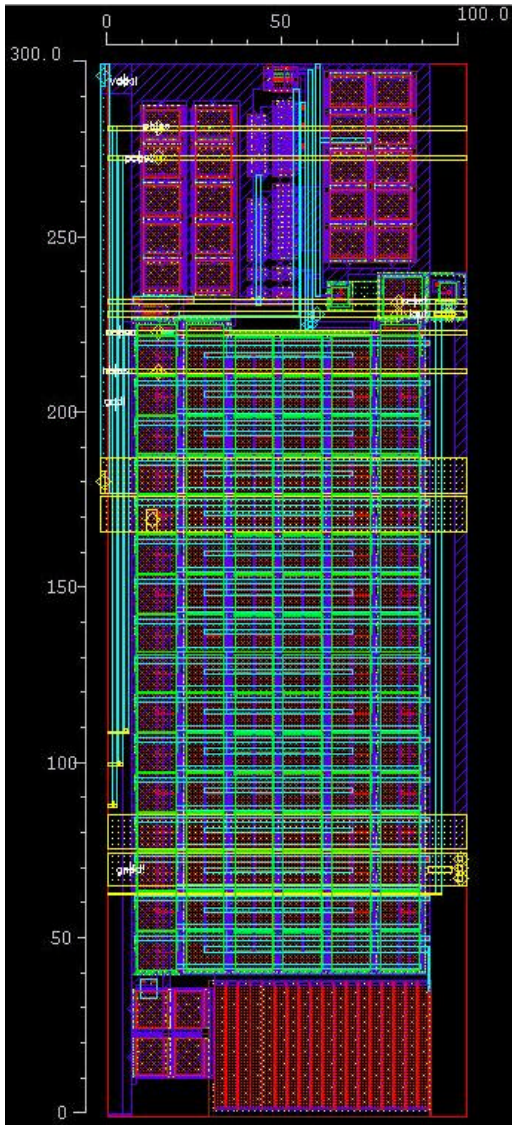
$$I_0 = I_{DO} e^{\frac{V_1}{nU_{Th}}}$$

$$I_0 = V_2 / R$$

$$\Rightarrow I_0 = \frac{kT}{q} \frac{\ln m}{R}$$

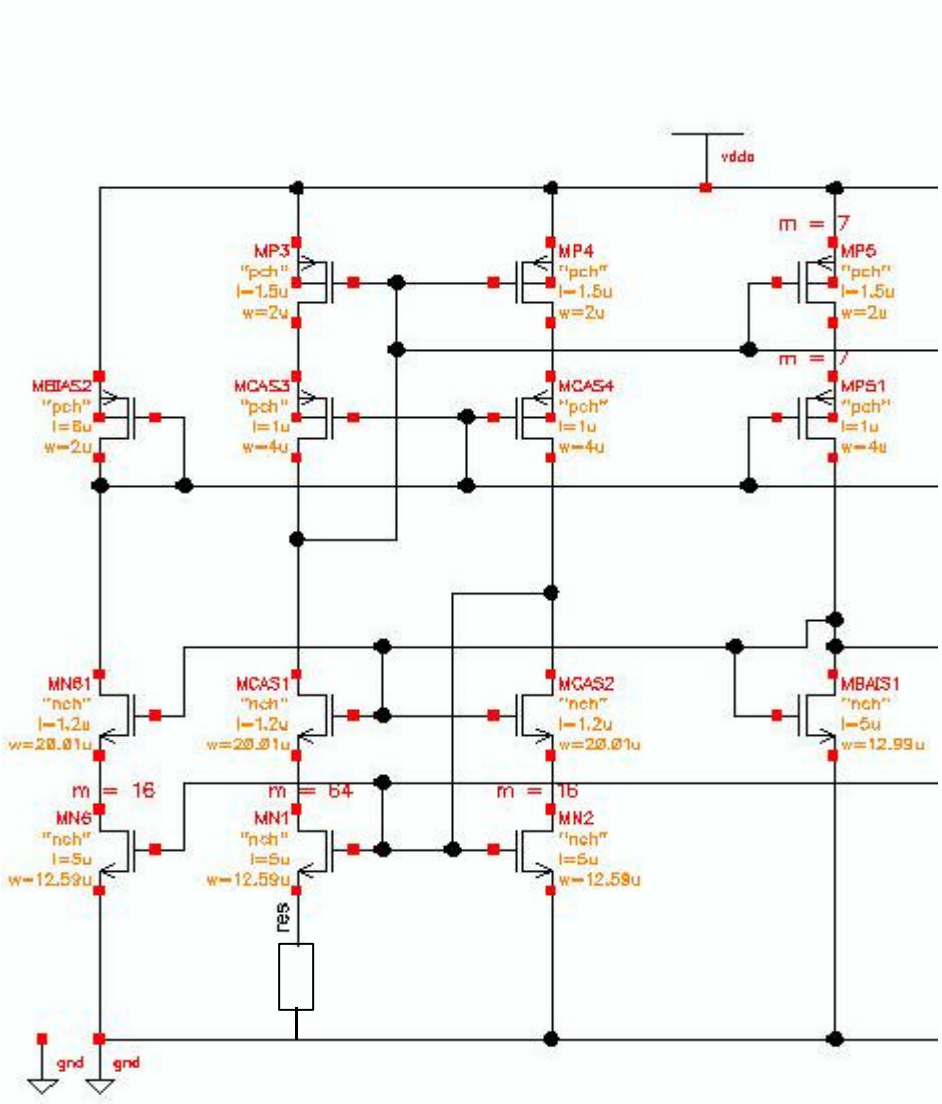
☺

Independent of technology parameters !



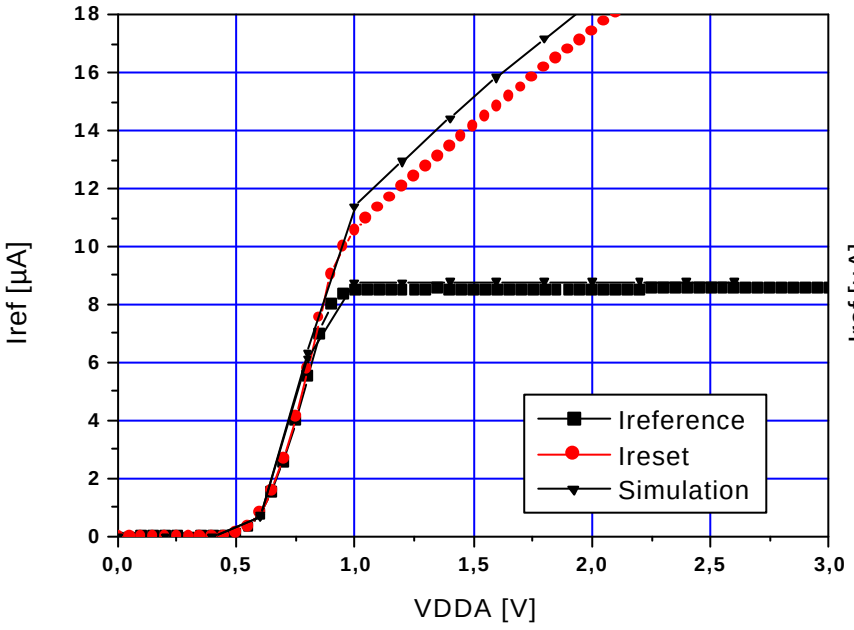
Layout:
300mm x
100µm

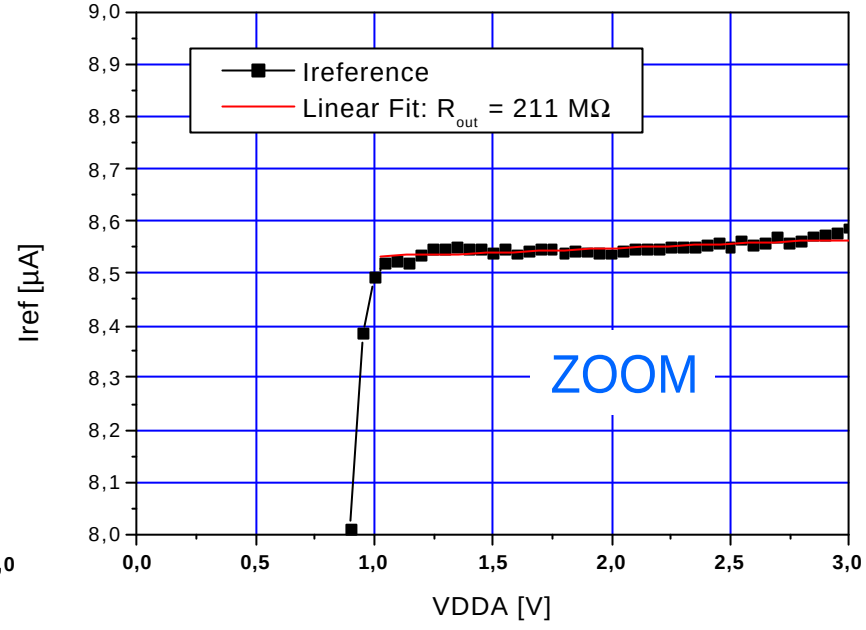
Current reference - detailed schematic



- NMOS in weak inversion
- Resistor is OP P+ poly
- All MOS are cascoded using low voltage cascode circuits
- Cascode biases are also used in other circuit blocks (DACs)
- Reset pin forces current into circuit for guaranteed start

Current reference - measurements

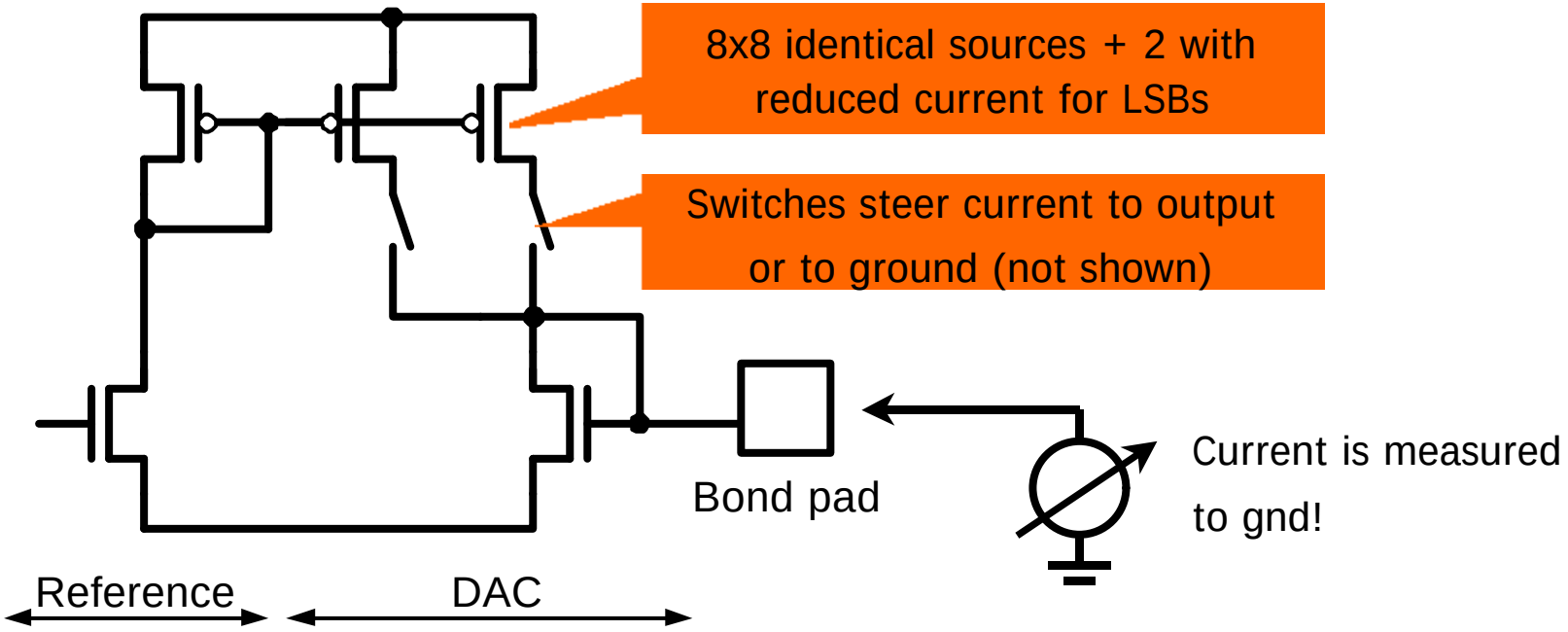




- Very high output resistance of R_{out} > 200 MΩ
- Reference works at 1 V !
- Normal operation and reset behavior are well described by simulation

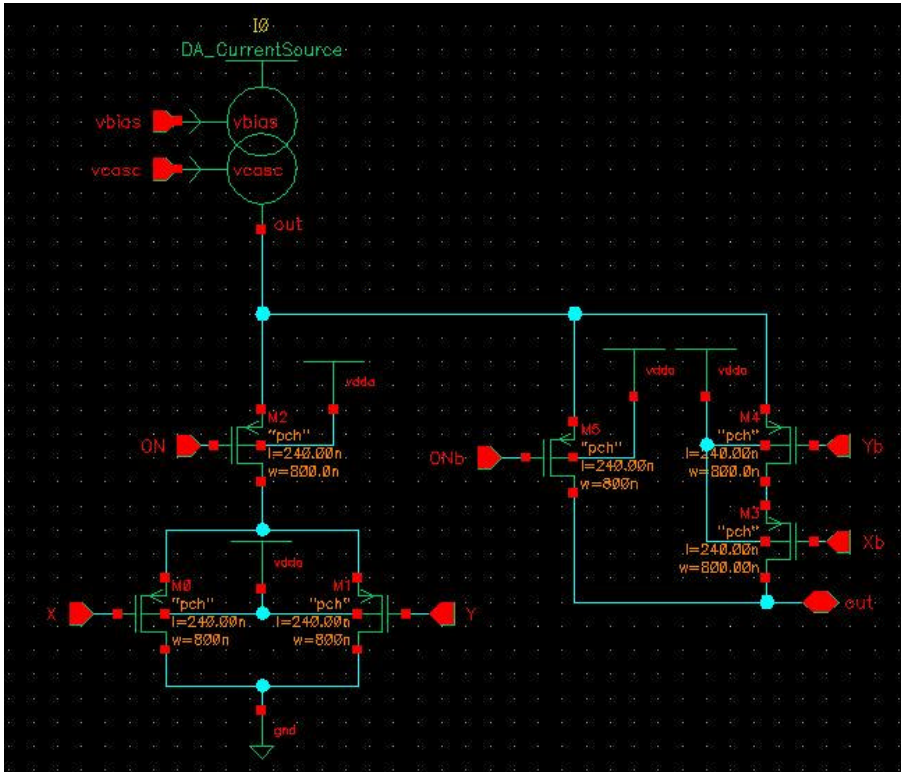
DAC principle

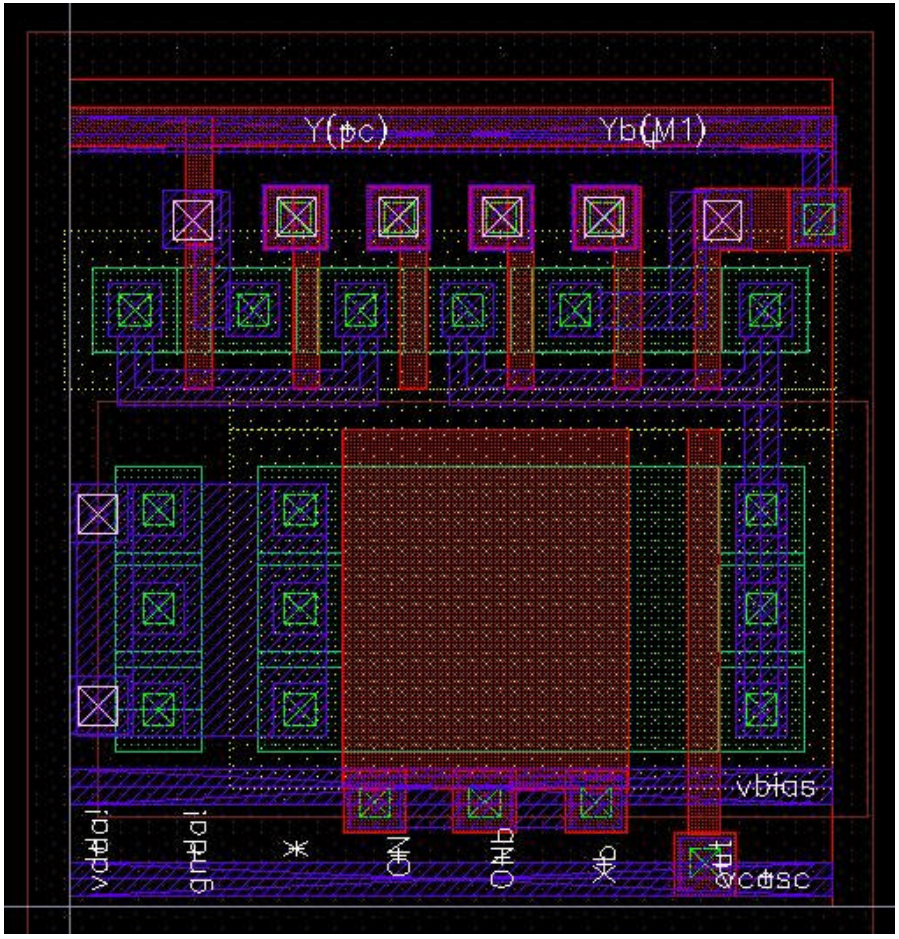
- 8 bit DAC has basically same design as DAC in DMILL chip which workes nicely.
- 8 x 8 = 64 unit current sources are used in a matrix, the 2 LSBs are down scaled sources
- The switches steer current to output *or* ground ⇒ PMOS sources are *always on* (irradiation!)
- Output is connected to bump pad for test and to diode - MOS of current mirror



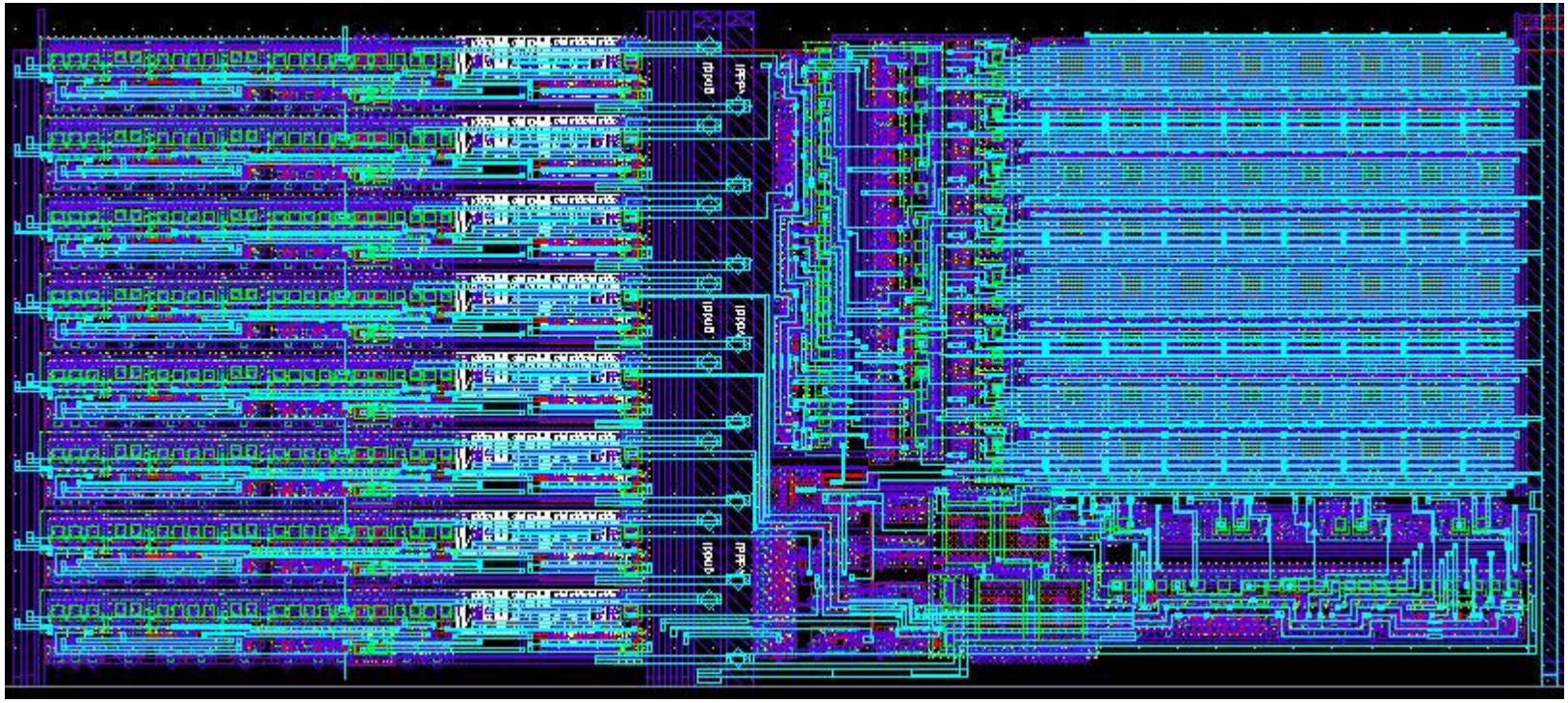
DAC unit cell schematic & layout

- Switch and x/y/row decoder are merged into one circuit





DAC + registers: complete layout



Shift register and SEU FFs

Size is 80 µm x 200 µm

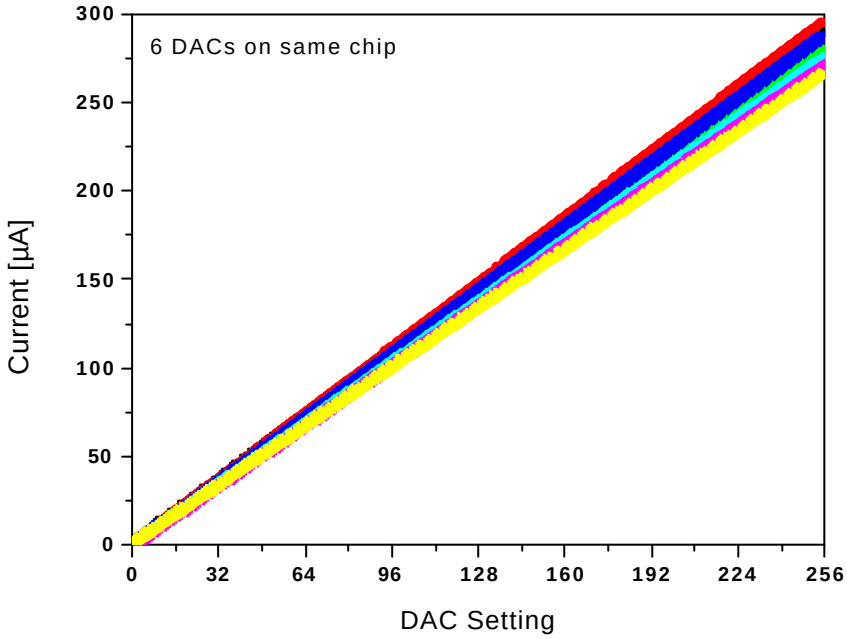
y - decoders

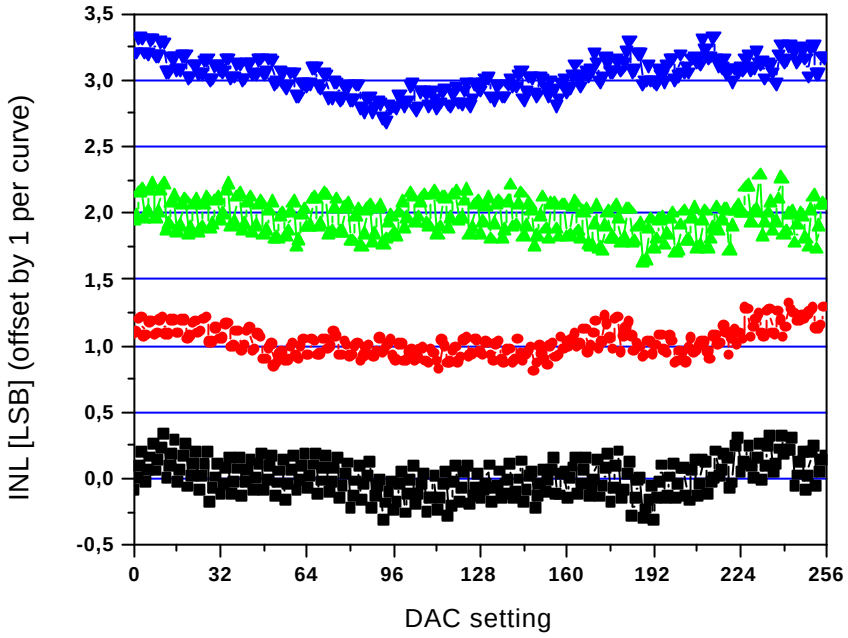
LSBs

Current sources and Switch Matrix

x - decoders

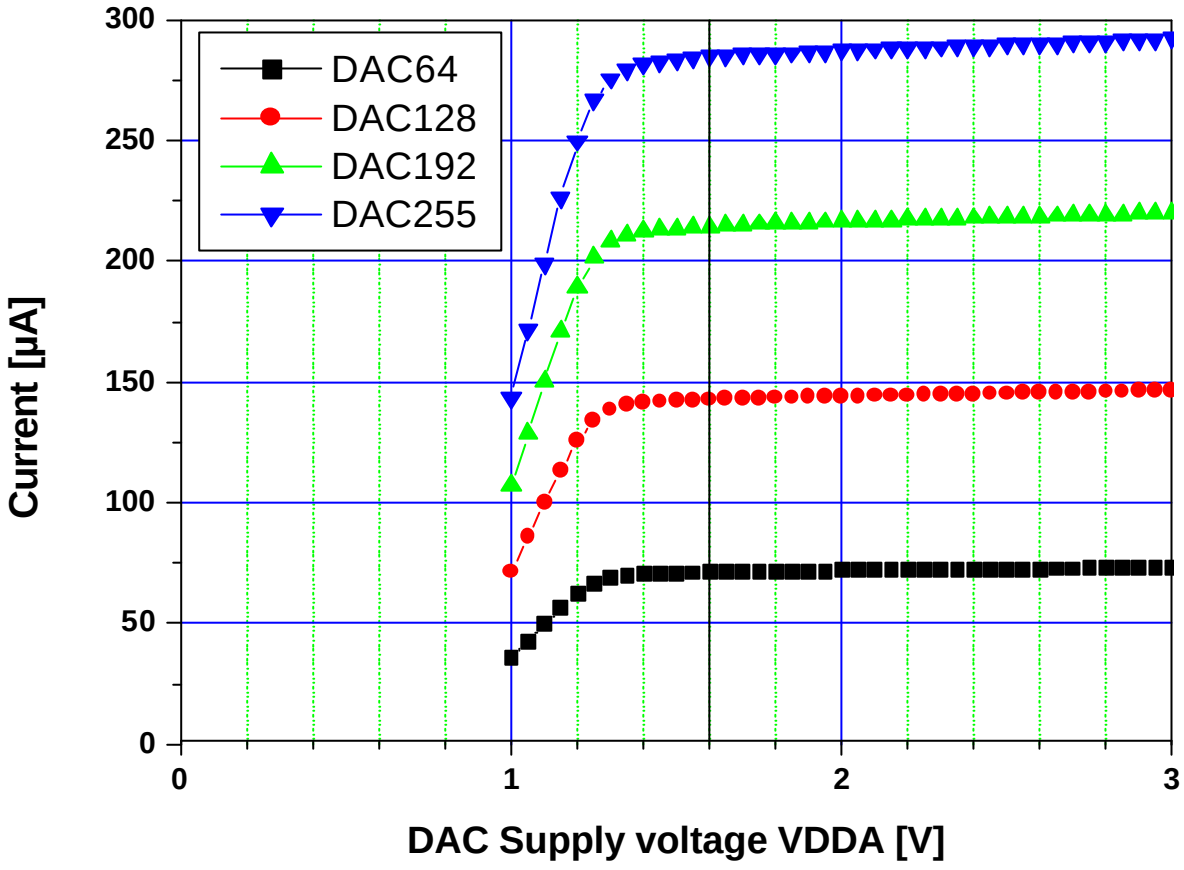
Measured DAC linearity





- Full scales on one chip vary by 10%
  (probably due to voltage drops on positive supply - see later)
- Integral non linearity < 0.5 LSB on all measured DACs ⇒ real 8 bit resolution

Measured DAC PSRR

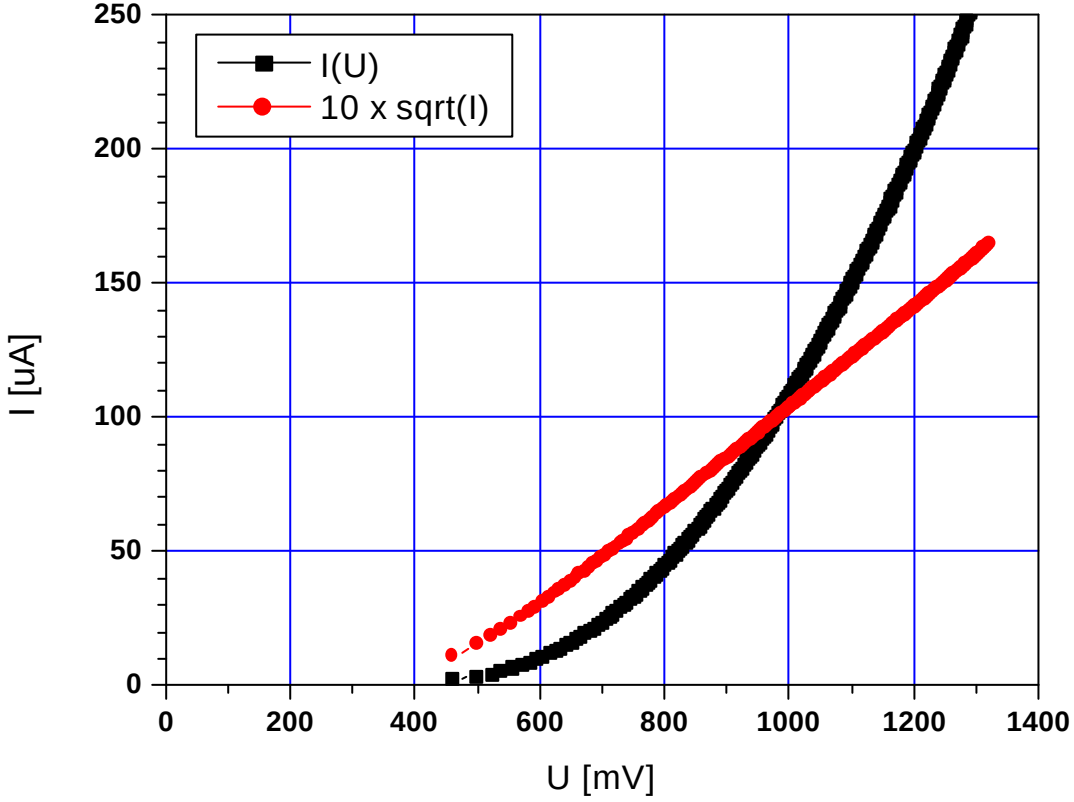


- Operation ok at VDDA = 1.4 V
- Current variation in range VDDA = 1.6 V … 1.8V is 1 %

For fun: Characteristic of diode MOS

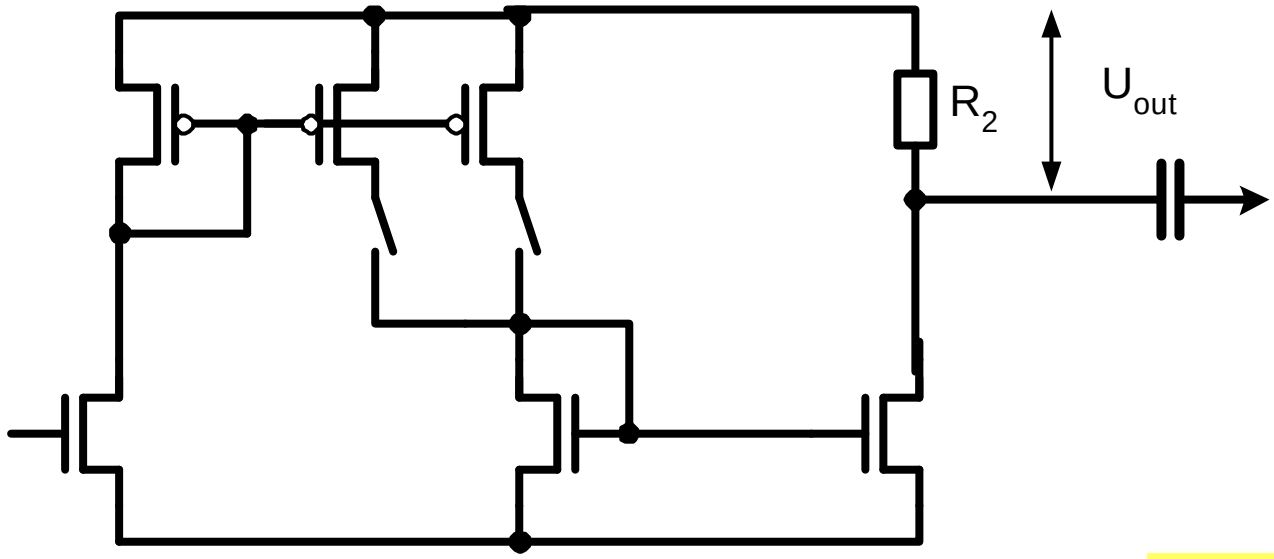
- Current is measured by shorting output to gnd! ⇒ I(DAC setting)
- Voltage can be measured when output floats ⇒ U(DAC setting)

⇒ Plot I(U) = characteristics of diode connected NMOS (here 5.8µ / 1.5µ):



Generation of calibration voltage

- Try to avoid dependence on absolute values



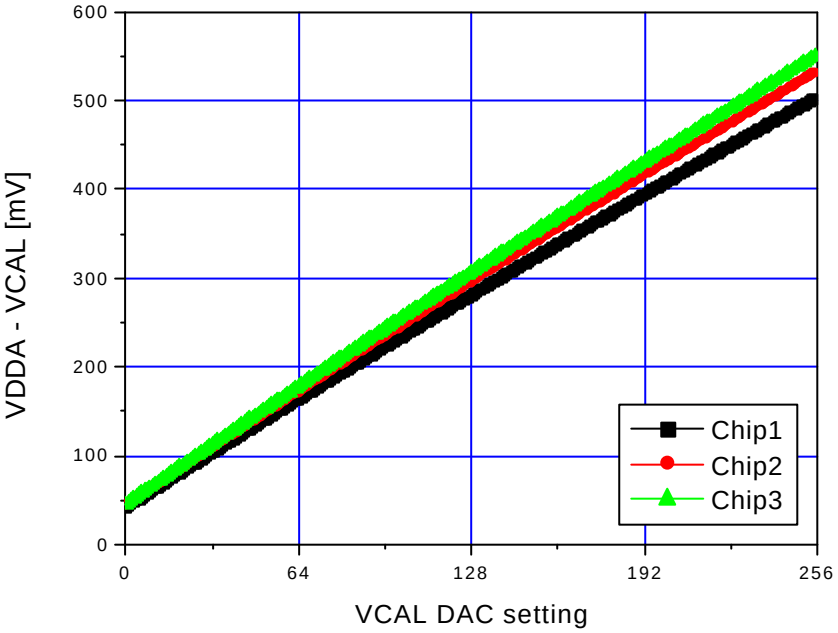
Reference ⟷ DAC ⟷ Voltage Gen.

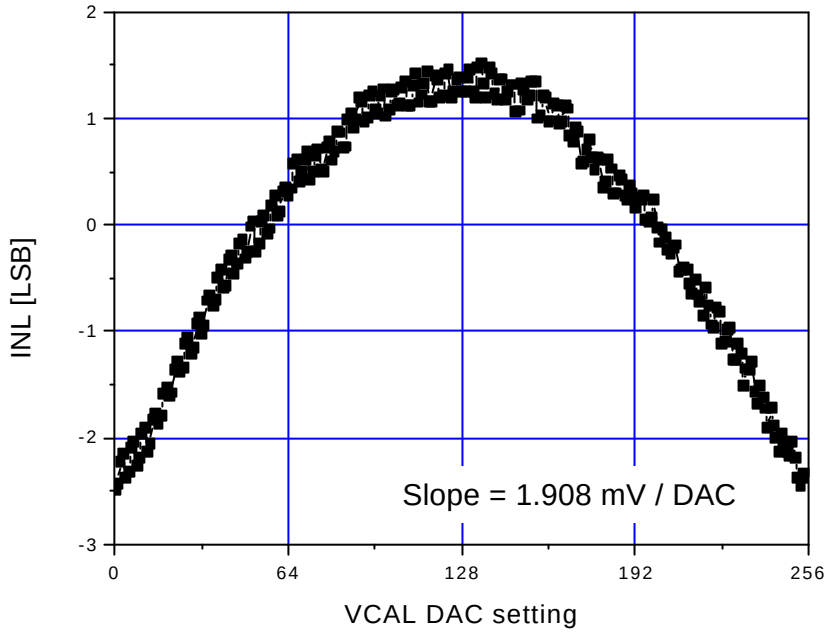
$$I_{ref} = \frac{a}{R_1} \qquad I_{out} = NI_{ref} = \frac{Na}{R_1} \qquad U_{out} = R_2 I_{out} = Na\frac{R_2}{R_1}$$

Voltage depends on resistor *ratio* only! ☺

⇒ Use same resistor types in reference and in VCAL generation

VCAL output - linearity and offset

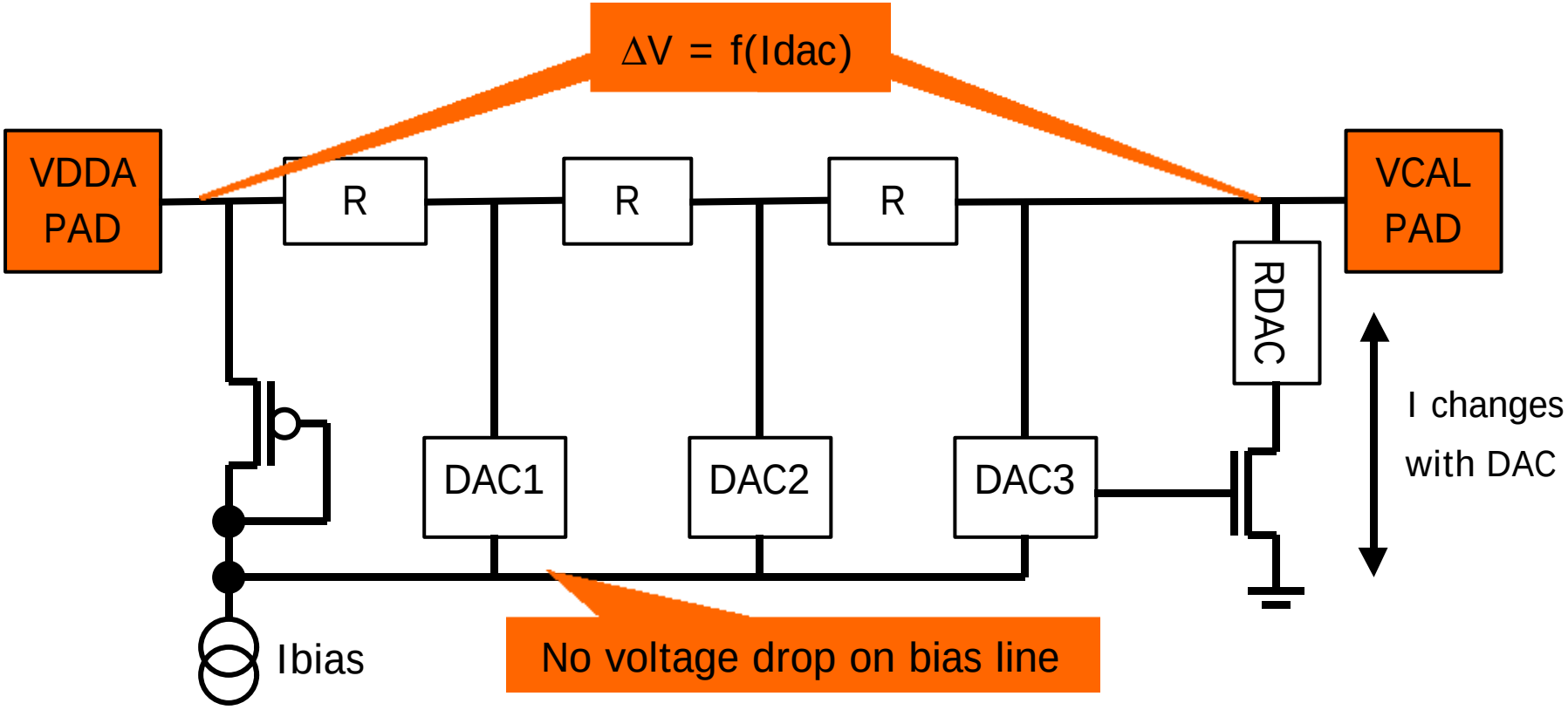




- Observe an offset of 42mV - 45mV !!
- Integral non linearity is bad (4 LSB) !
- Remember: Current is provided by DAC identical to the ones presented before.

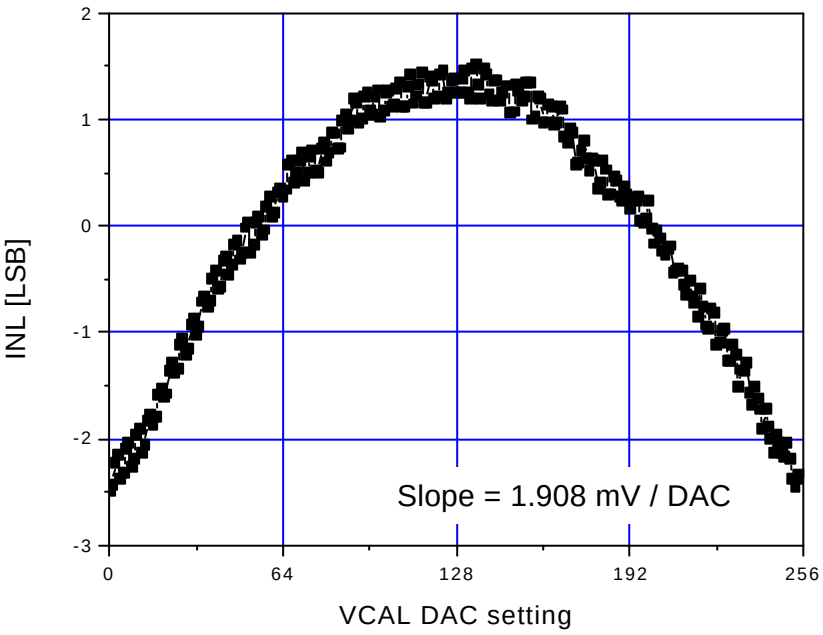
VCAL problem - Explanation

- Observations are perfectly explained by voltage drop on vdda! Line (which is 10µm wide M3 ! - Current is ~ 4 mA)
- Calculation gives 40mV offset, simulation shows observed non linearity.
- (Effect not seen in other DACs because current does not change with setting!)

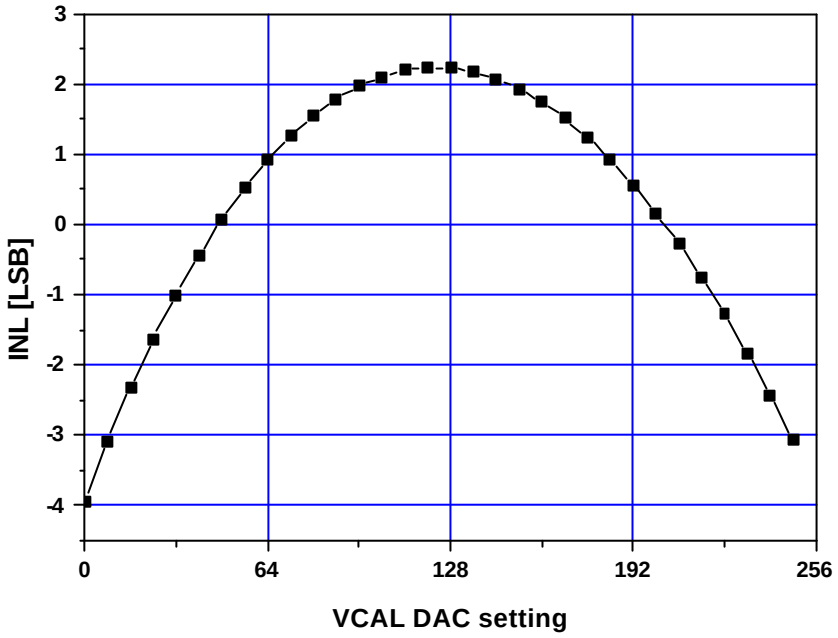


Simulation of voltage drop

Simulation done with Rs extracted by hand with technology parameters



Measurement

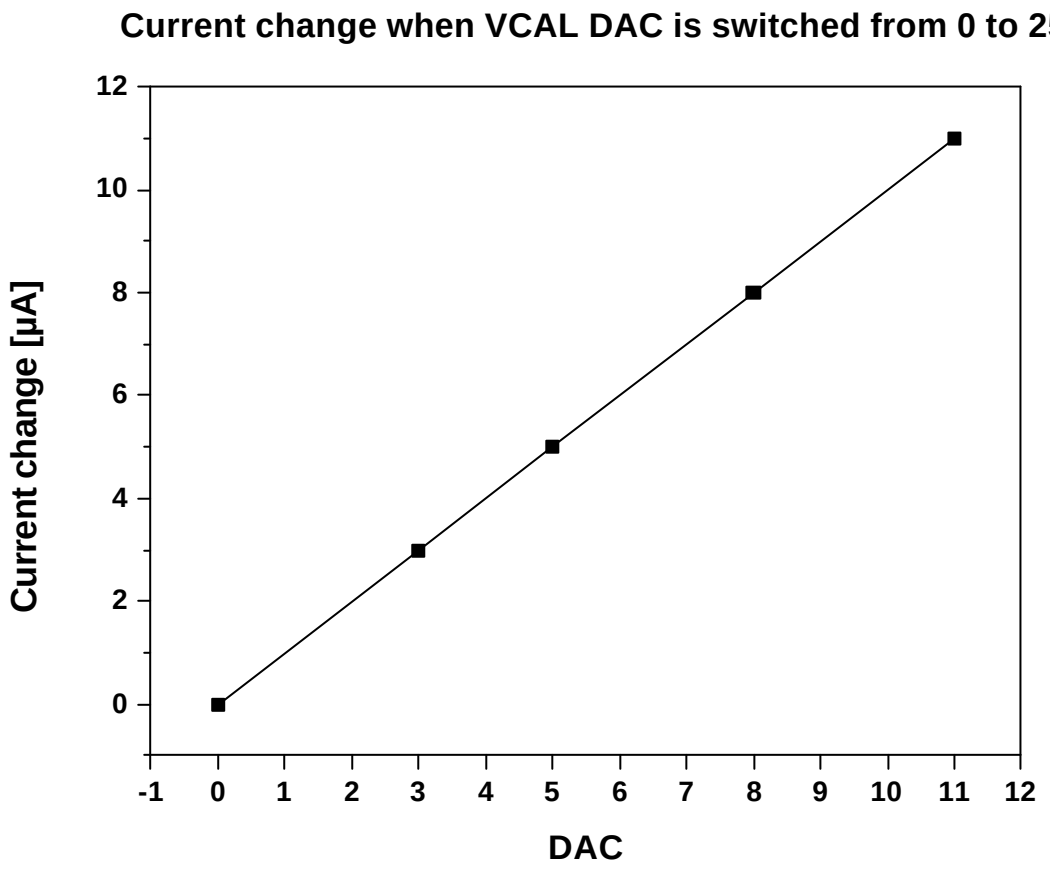


Simulation

This voltage drops leads to a (small) systematic mismatch of current mirrors from bias to pixels: Currents in the pixels are a bit SMALLER

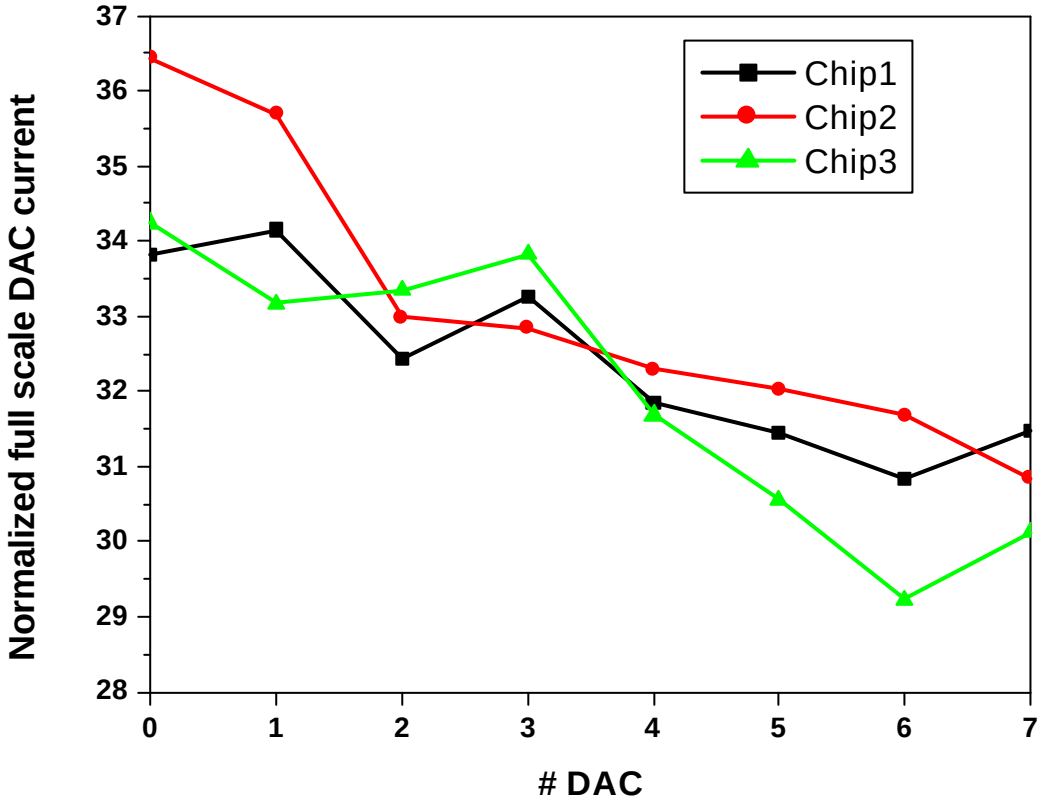
Switching voltage drop on / off:

- Current changes with VCAL DAC setting. This changes the voltage drop.
- Measurements shows DAC current for these two cases as function of DAC position:



Further consequence of voltage drop

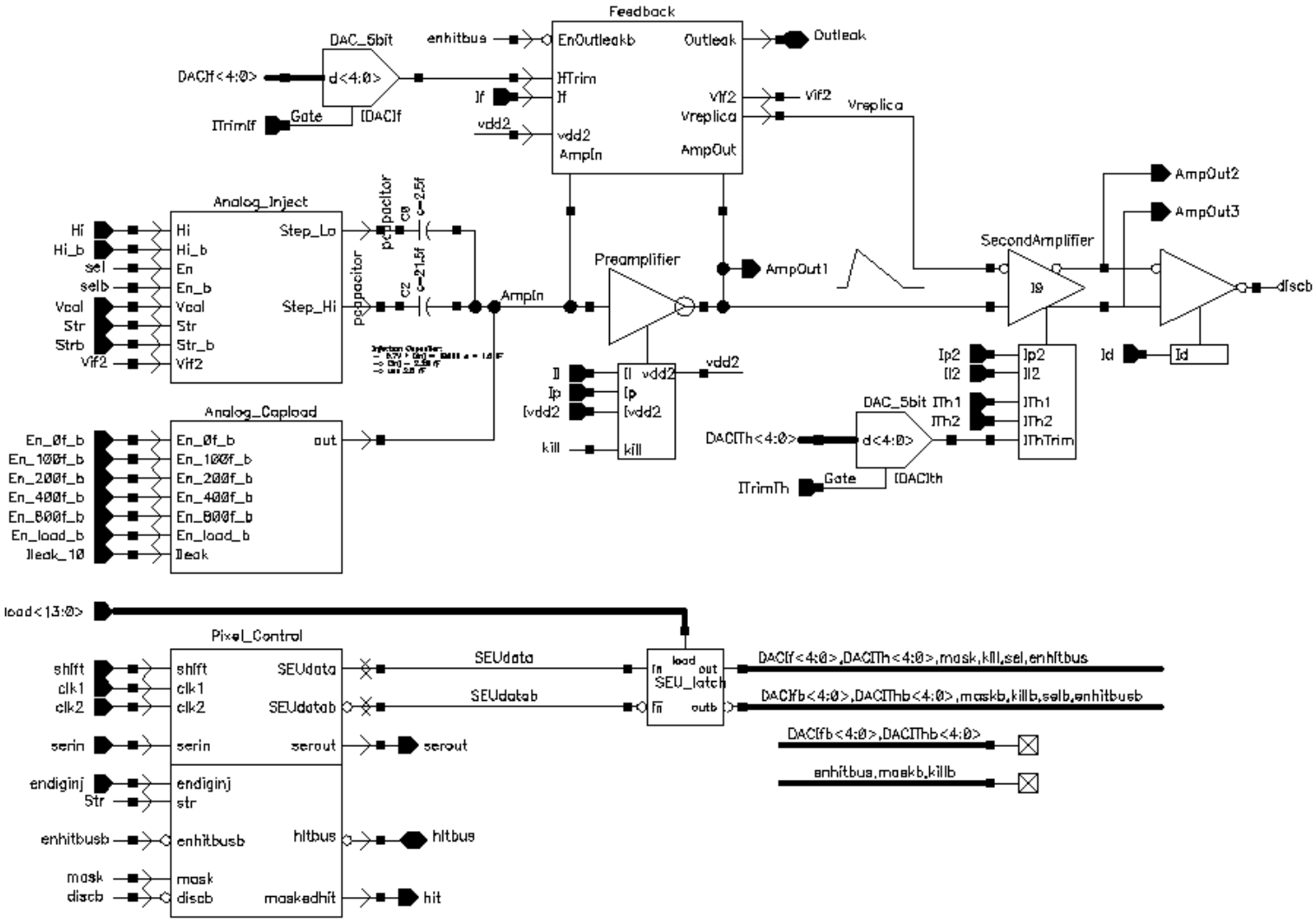
- Current provided by DACs becomes systematically smaller when DAC is further away from bond pad.
- Measurement shows full scale current of 7 DACs on 3 different chips (normalized to reference current)



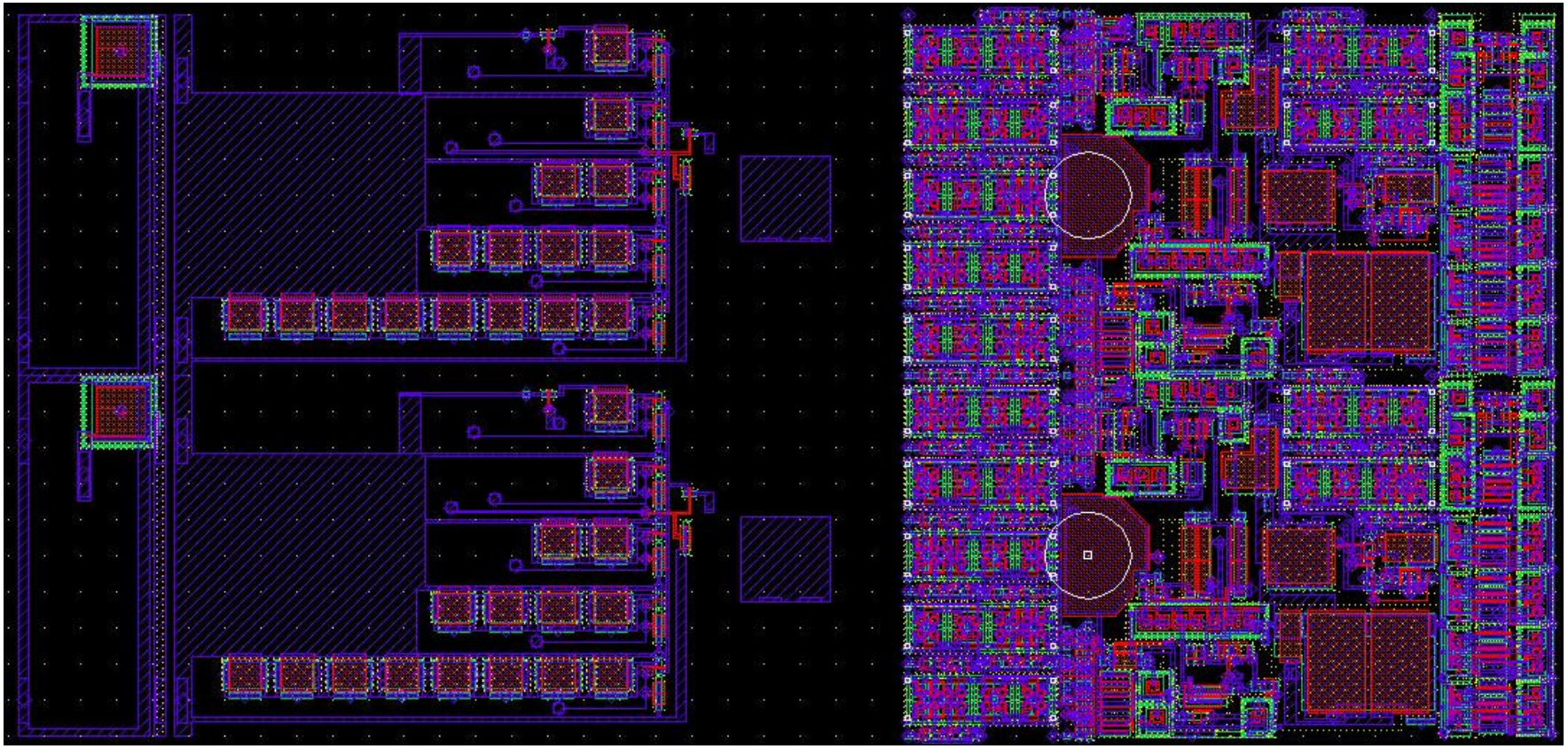
Pixel unit cell - circuit blocks

- Injection chopper with 'low' and 'high' charge injection mode
- Single ended charge sensitive preamplifier
- Novel feedback circuit (L.B.) with linear return to baseline, leakage current compensation. Measurement of leakage current in every pixel. 5 bit trim of feedback current (i.e. of ToT). Full scale set by global DAC.
- DC coupled differential second stage
- Differential discriminator. Global threshold is set by global DAC. 5 bit trim of threshold. Full scale set by global DAC.
- 4 Control bits to
  - Select pixel for injection
  - Enable fast Hitbus (Hit OR) for monitoring and self triggering
  - Mask pixel
  - 'Kill' pixel i.e. switch off analog part.
- All 14 bits are stored in SEU tolerant FFs. Readback of every FF is possible.

Pixel unit cell schematic



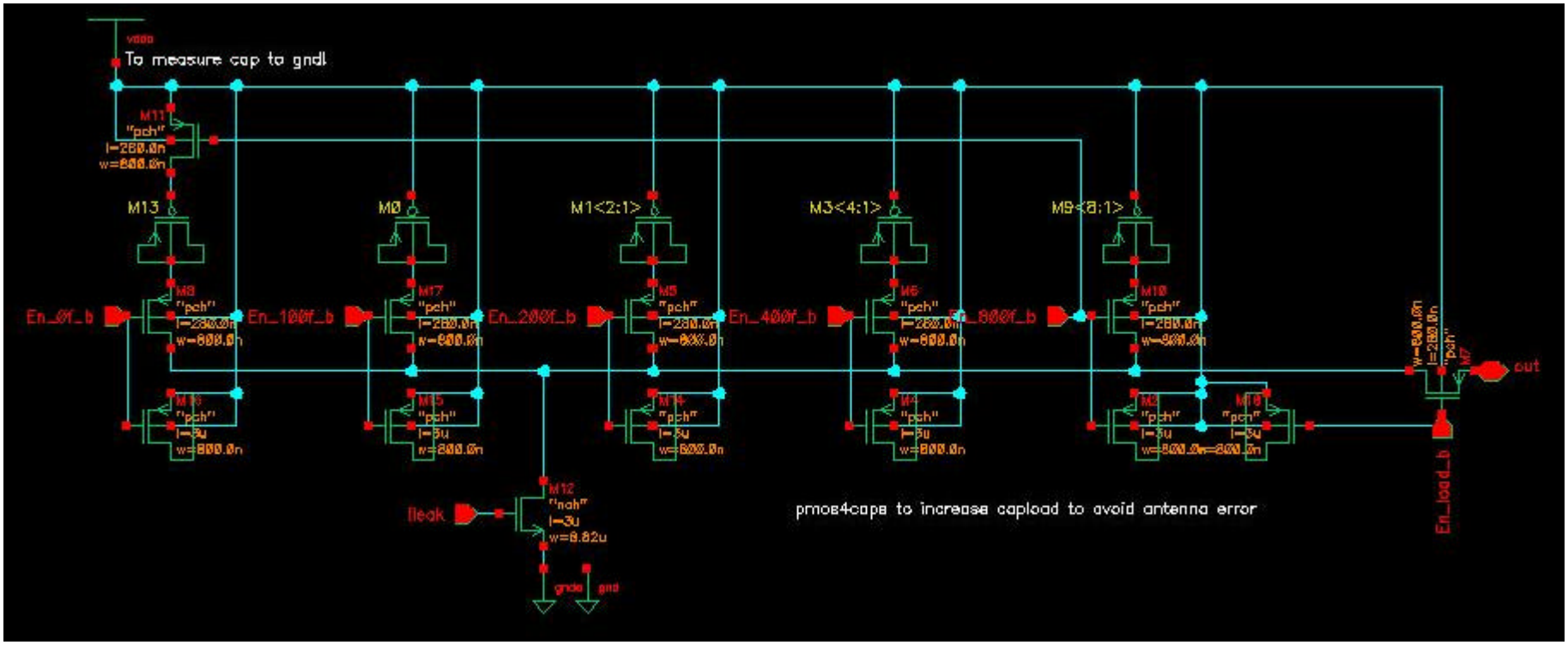
Layout (up to M1)



Capacitive loads and
leakage current source

90 µm

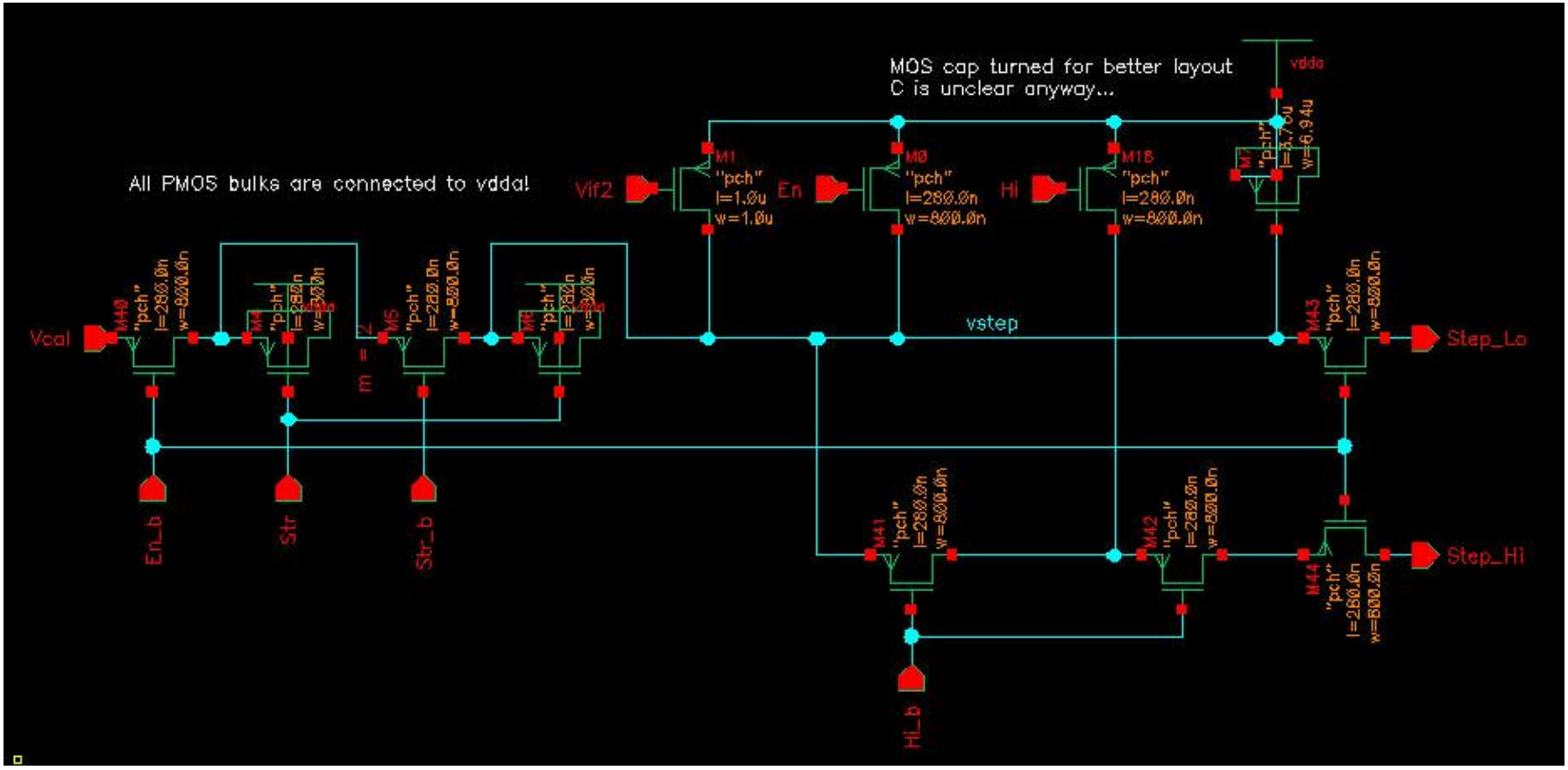
Capacitive load circuit



- Can connect 0 … 15 x C_{load} to preamplifier input
- Complete circuit can be disconnected from input for safety ('En_load_b')
- Generate leakage current with NMOS in weak inversion. Current is generated with on-chip DAC so that no external source is required!

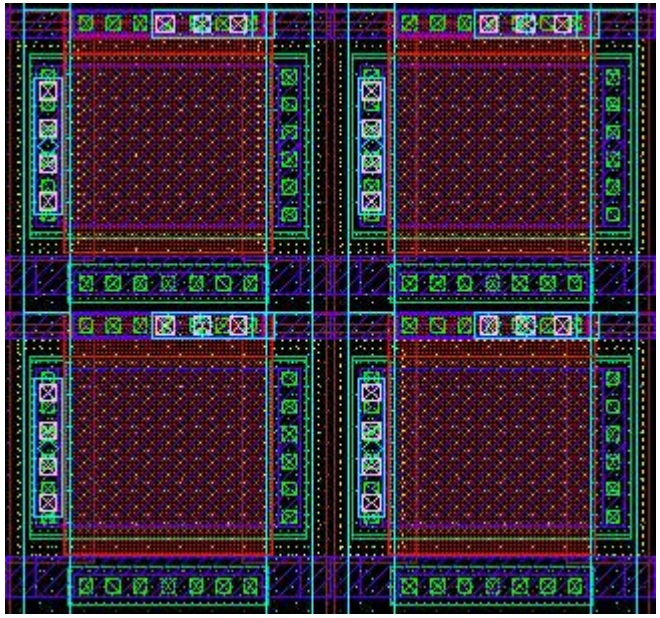
Injection circuit

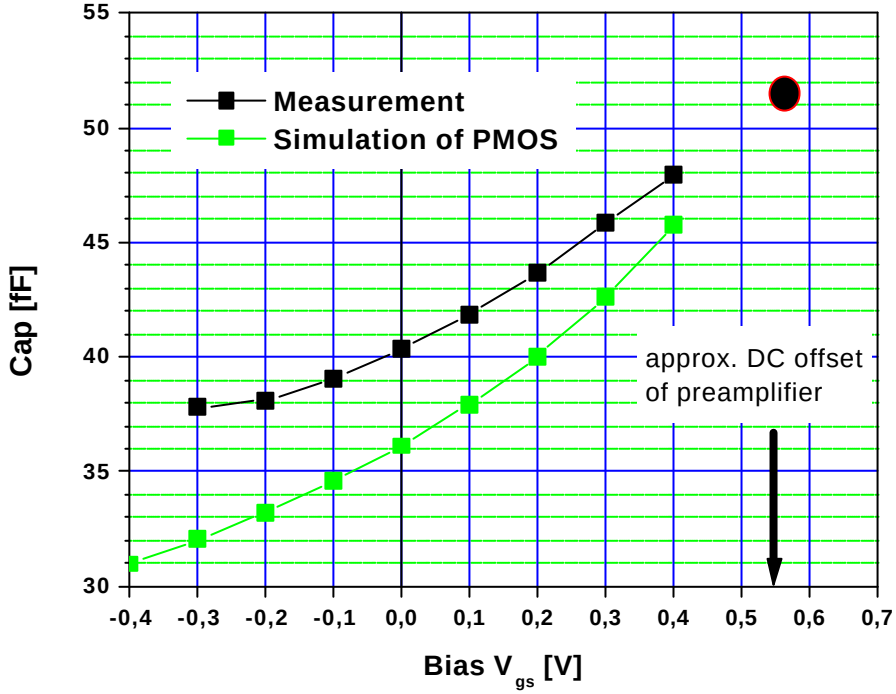
- Use two injection caps for low and high charge mode
- Use dummy switches to compensate charge injection
- wrong sign slope is slow due to discharge with small current



Calibration of C_{load}

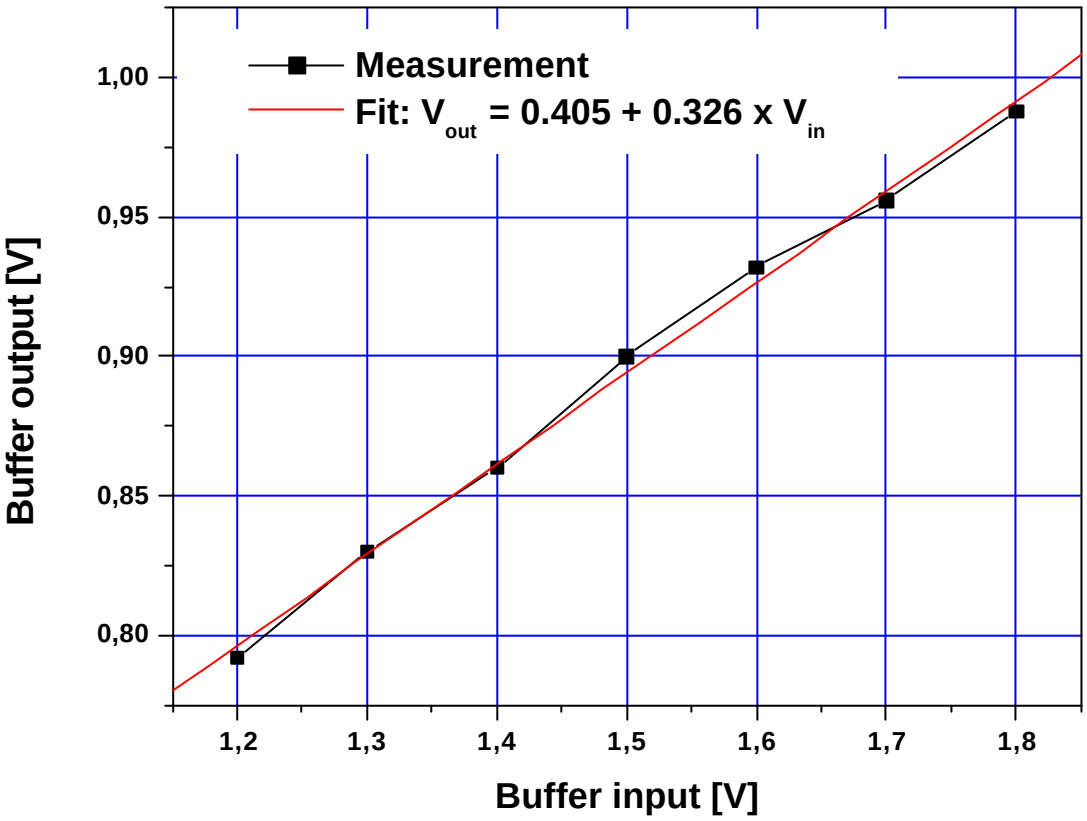
- An array of 15000 capacitors is available on the chip.
- Unfortunately, the gate has input protections, so that a sweep of C(U) is limited to ± 0.4 V.





- In application, bias voltage is ~ 0.55 V -> extrapolated C_{load} = 52 fF

Calibration of Analog Buffer



- Voltage can be injected externally (via MUX) for calibration

⇒ Measured gain is 0.326 (this includes a division by 2 to match 50 Ω cable.

Extraction of other Cs from layout

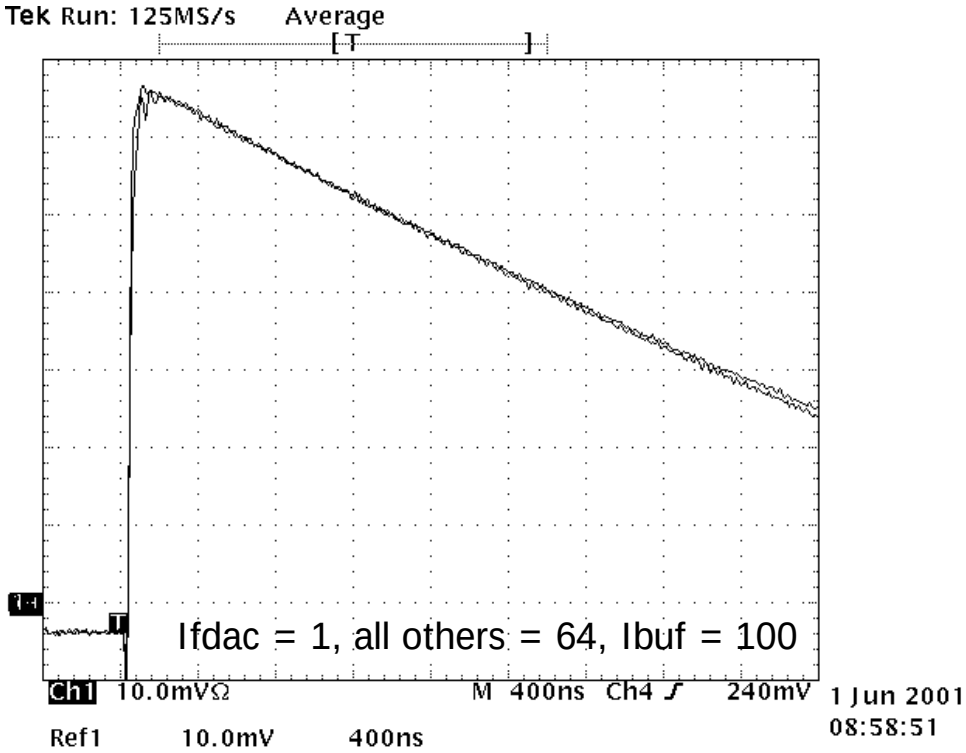
- MOSIS parameters of TSMC runs have been used
- C inject, low = 4.84 fF (2.12 fF area + 2.72 fF fringe) ⇒ 30 e/mV
- C inject, high = 26.8 fF (17.7 fF area + 9.1 fF fringe)
- In high mode, both injection caps are used ⇒ 200 e/mV

⇒ expect ratio between High and Low injection of $(C_{hi}+C_{lo}) / C_{lo}$ = 6.54

Plot shows preamp output for

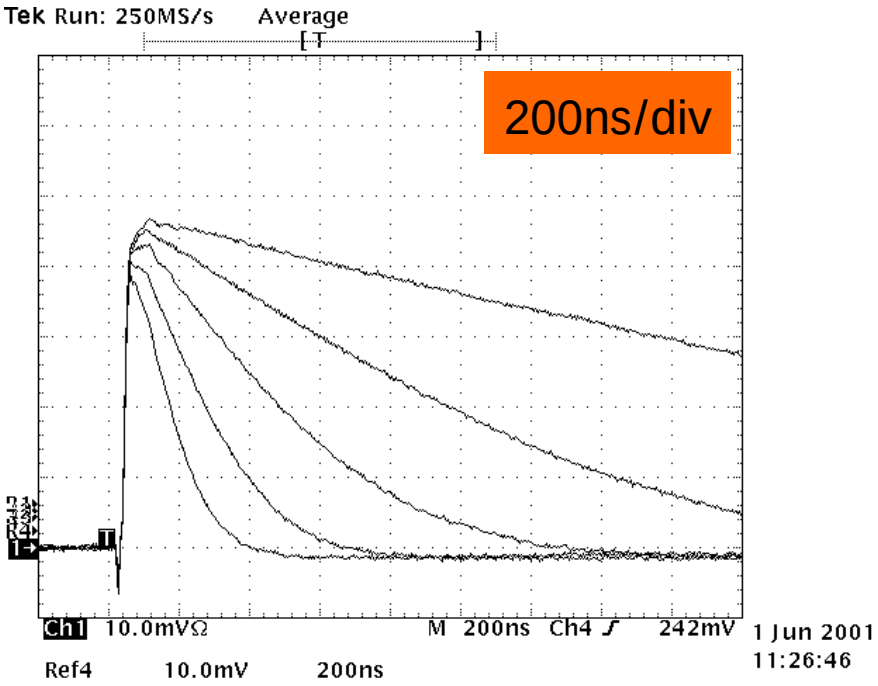
1. High mode, ΔV= 150 mV
2. Low mode, ΔV= 1050 mV

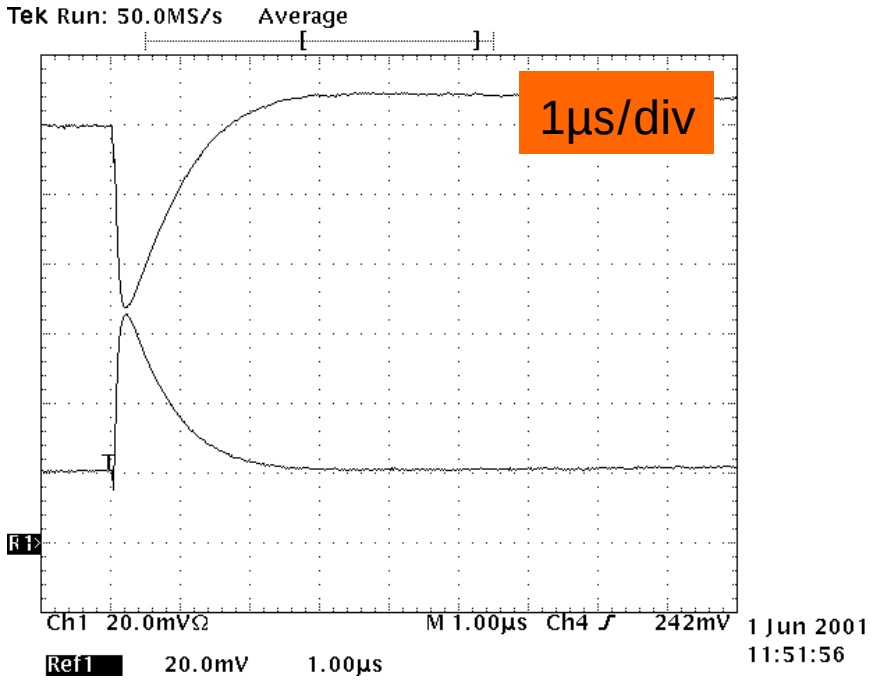
⇒ Measured Ratio is 7.0 - ok



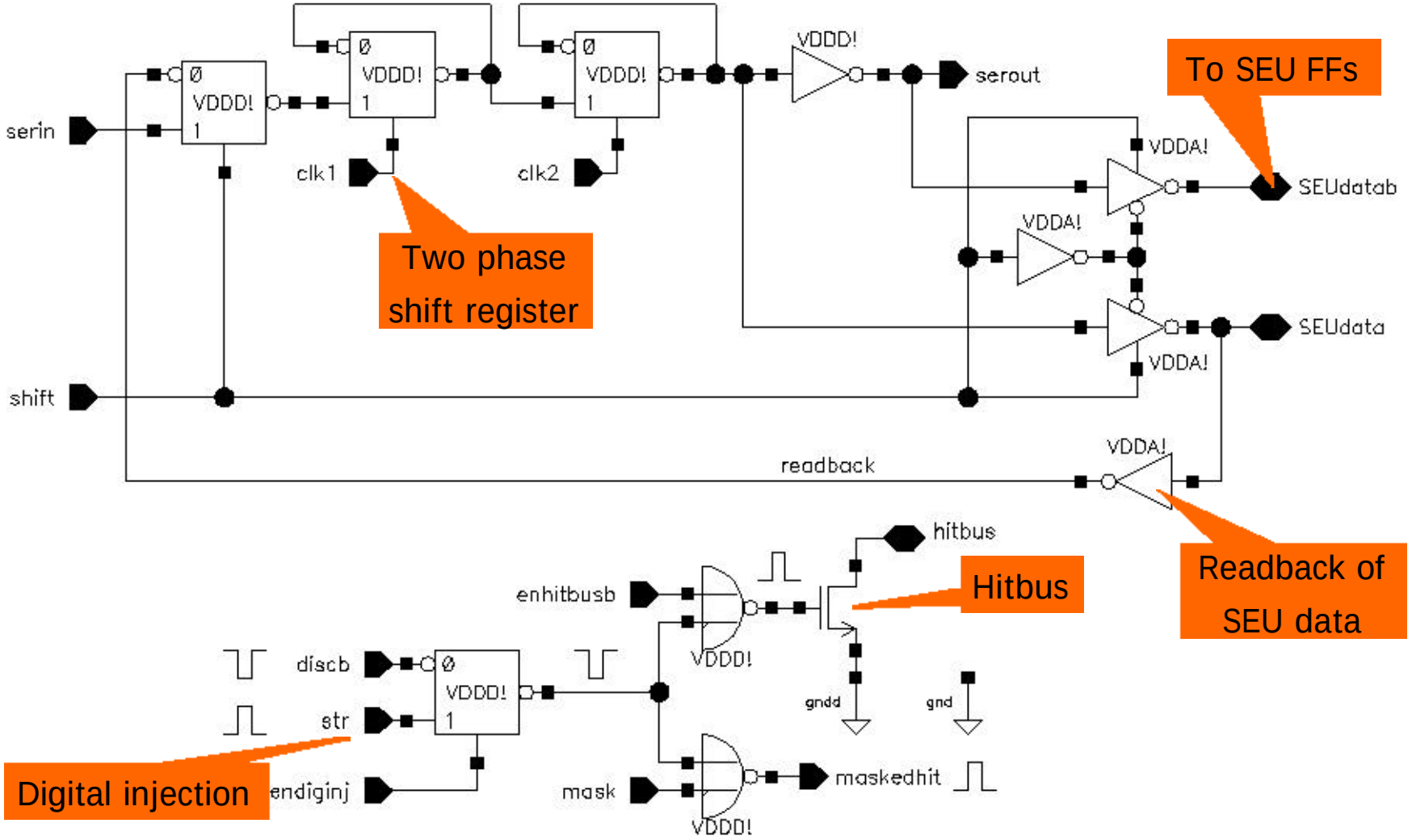
Some more plots...

- Left: If = 1,3,7,15,31 , all other biases=64, Hi mode, 100mV ~ 20ke
- Right: Ampout2, Ampout2B, low mode, If=3, 370mV, ITh1=ITh2=10
  (injected charge is just below threshold)





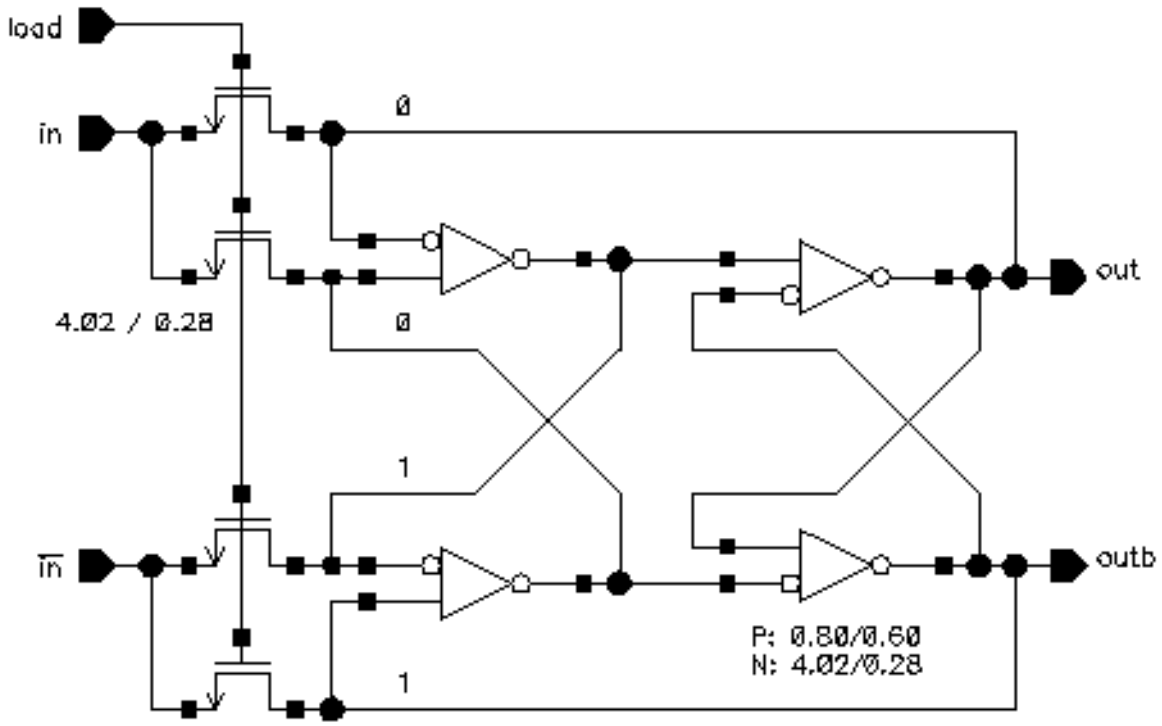
Pixel control part



Measurement: control part works down to VDDD < 1.5 V

SEU flipflop - schematic

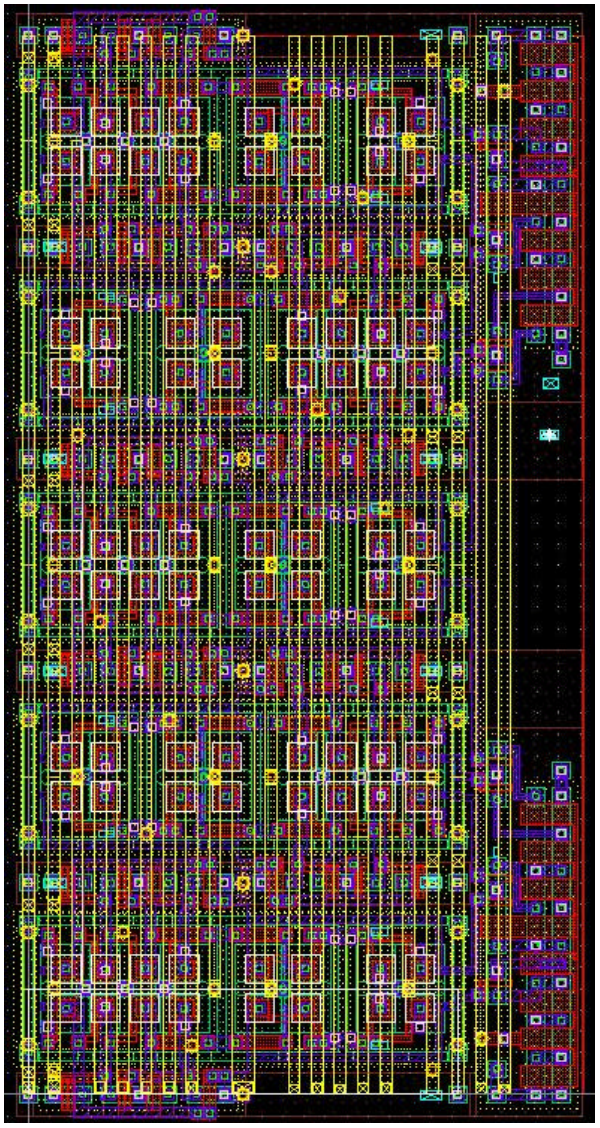
- Circuit as proposed by Calin et al. 1996 in IEEE Trans. Nucl. Sci.
- Here: PMOS are much weaker than NMOS



- one sort of transistors must always be stronger than the other one
- Input must be strong enough to overwrite (Inv_min is sufficient)
- We use ANALOG SUPPLIES to avoid digital supplies in analog part
- PMOS in Inverters are weak for easy flip and low short circuit current (also in case of yield problem)
- low supply voltage makes flipping easier + lowers short circuit current
- Body effect on NMOS input pass transistors is reduced.

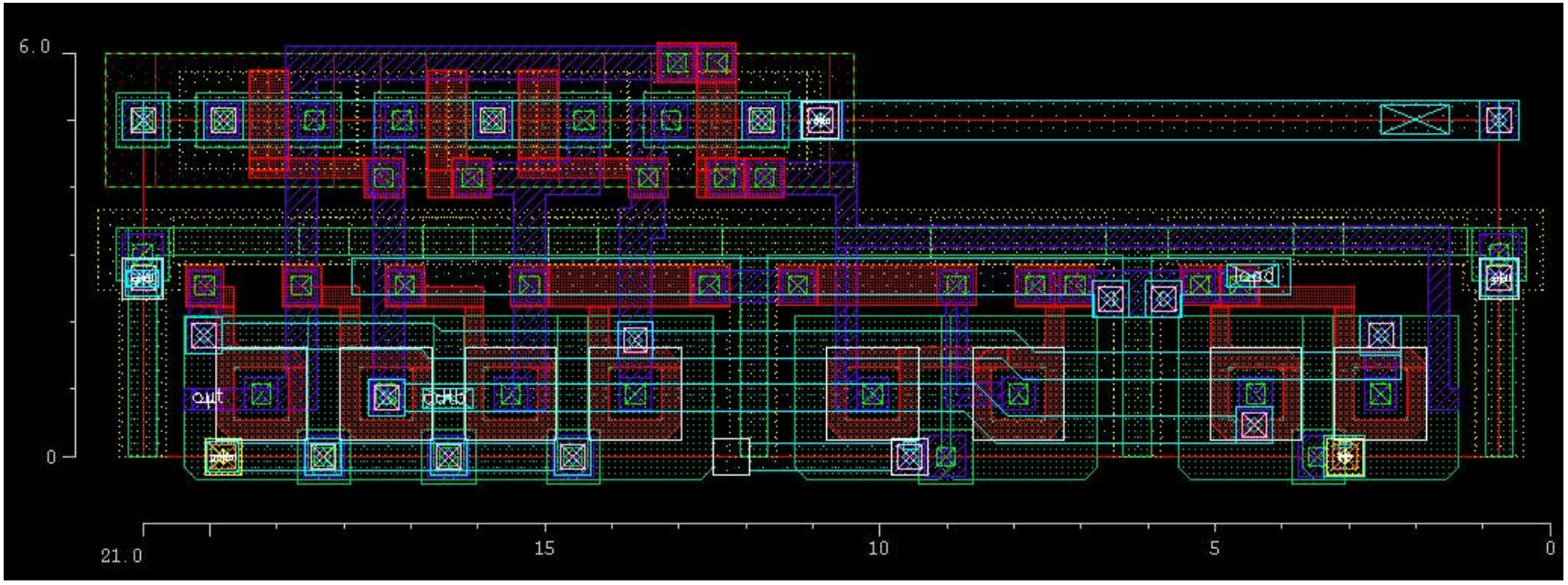
Layout of SEU FFs in pixel

- 10 (!) SEU FFs fit into 50 µm height
- They are used to control two 5 bit DACs (ToT and threshold trim)
- 4 more SEU FFs are in control part
- Control is through 14 *LOAD* lines running vertically in M3
- All 14 FFs get their input data from the pixel control shift register



SEU flipflop : individual layout

- Size is 6µm x 21µm, allows merging of two FFs



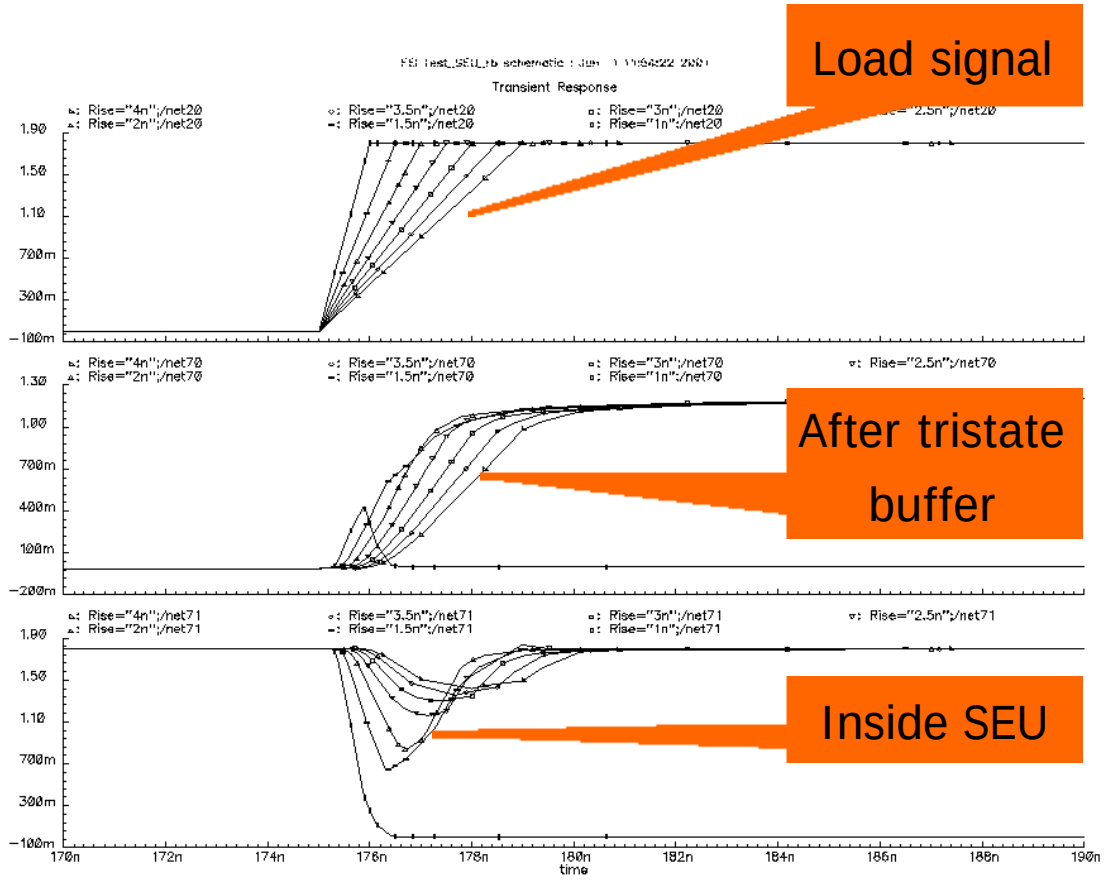
- Problem:
  - readback does not work in standard conditions.
  - It works, however, if vddd! << vdda! = (for instance 1.7V / 2.0 V)

Explanation

- The output of the tristate inverter in the control is loaded by the inputs of the 14 SEU FFs (large drains, ~ 150fF)
- When buffer is disabled, this capacitance stays precharged
- A *fast* load signal connects the SEU instantaneously to this capacitance.
- Due to simultaneous action of bit and its inverse, the SEU FF is flipped
- Therefore readback does not work.

Simulation of SEU readback problem

- Simulation with 14 FFs
- Problem is modeling of drain cap !!!
- Result:
  if rise time is too small, capacitive load on r/w busses flips the SEU.
- Simulation is OK for risetime > 1.5 ns
- If capacitive load is increased artificially, readback ALWAYS works if rise time slow enough.

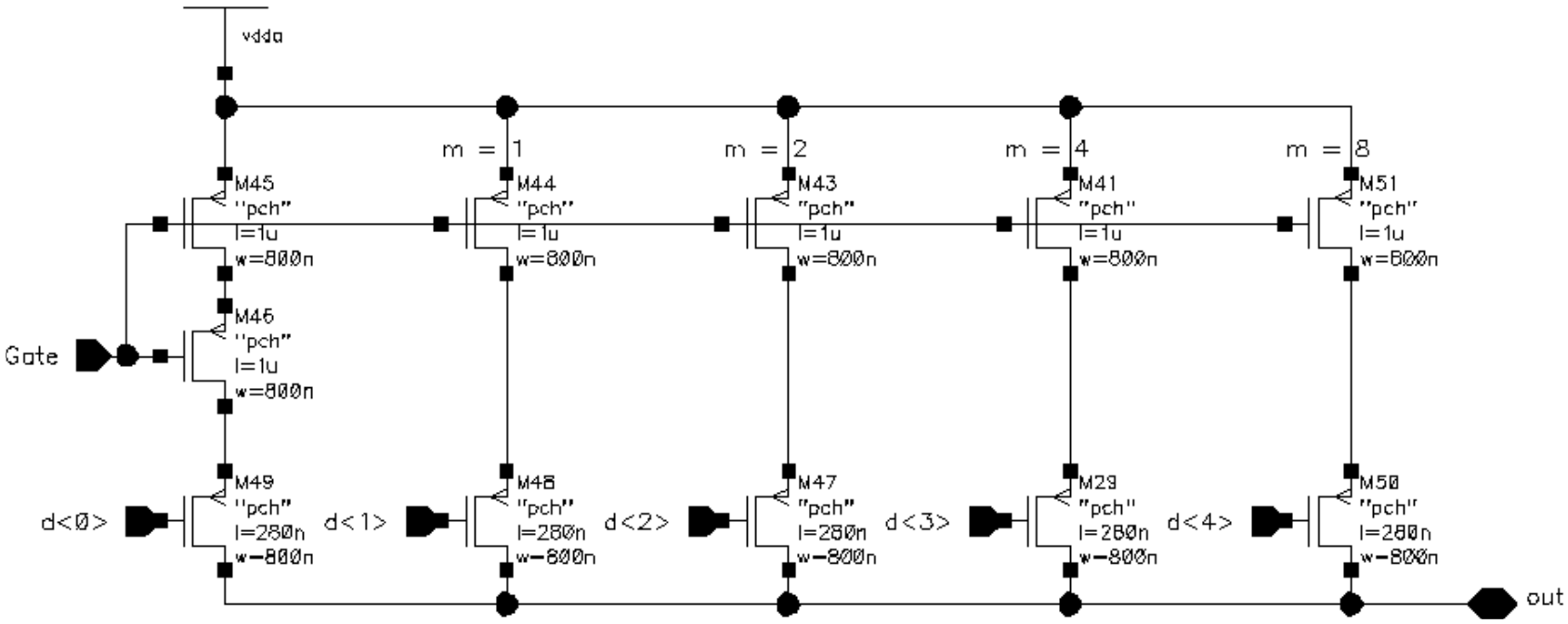


Problem solution

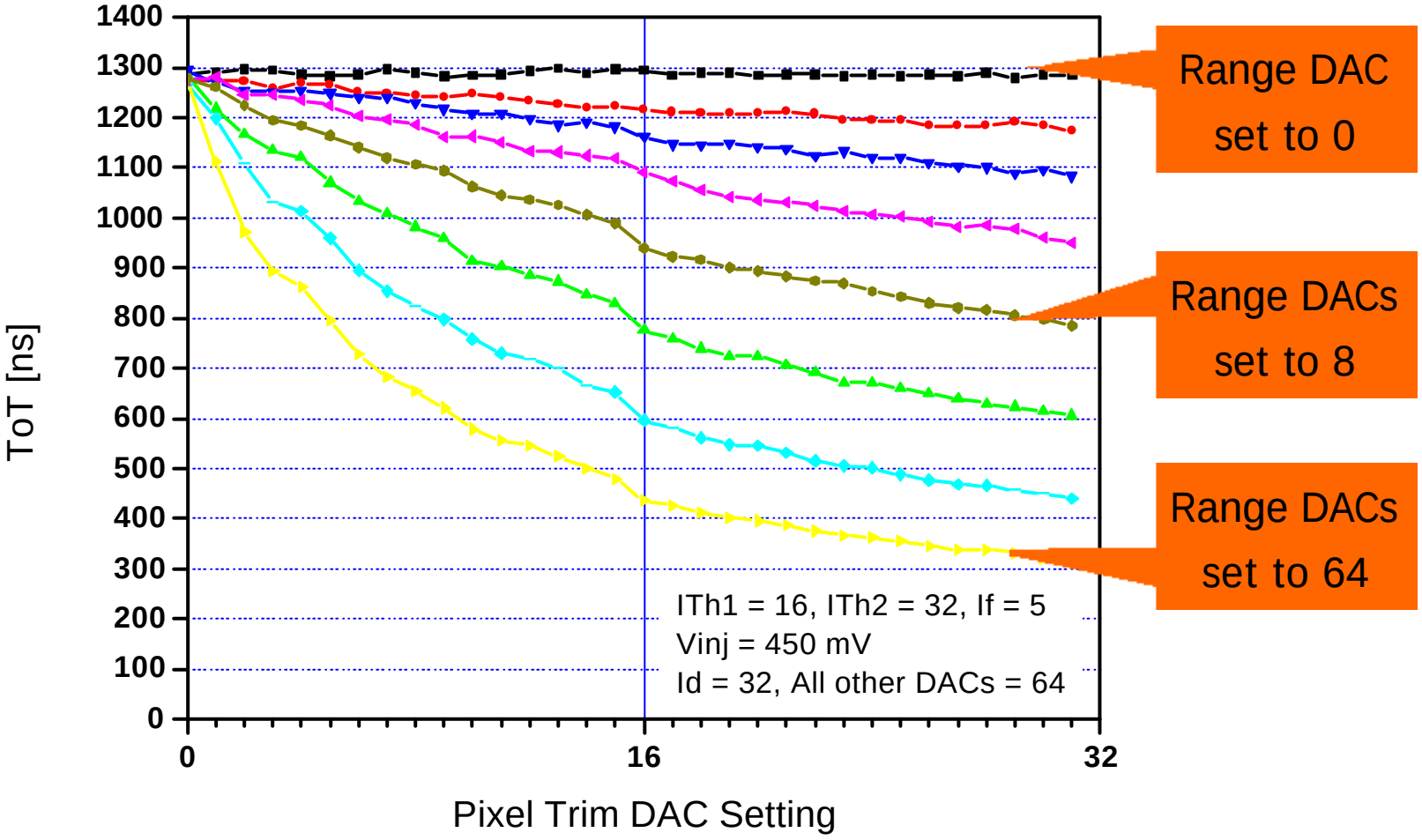
- Use a signal with reduced rise time (5ns are largely enough)
- This causes no problem for write phase (write and read are level sensitive)
- Signal is produced for each of the 14 load signals with a current starved buffer (which has to drive a large capacitive load of 160 pixels + bus anyway...)

5 bit DACs in pixel

- Use current sources with increasing multiplicity



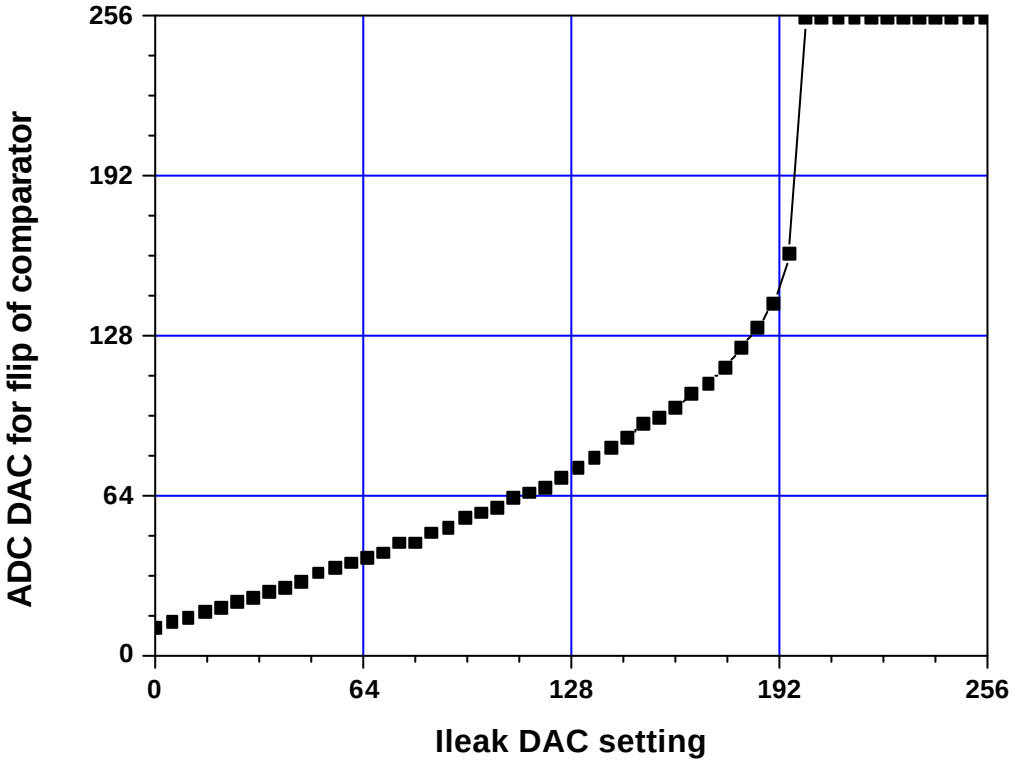
Example: ToT trim



- DAC is monotonic, scaling of range works nicely. More from John!

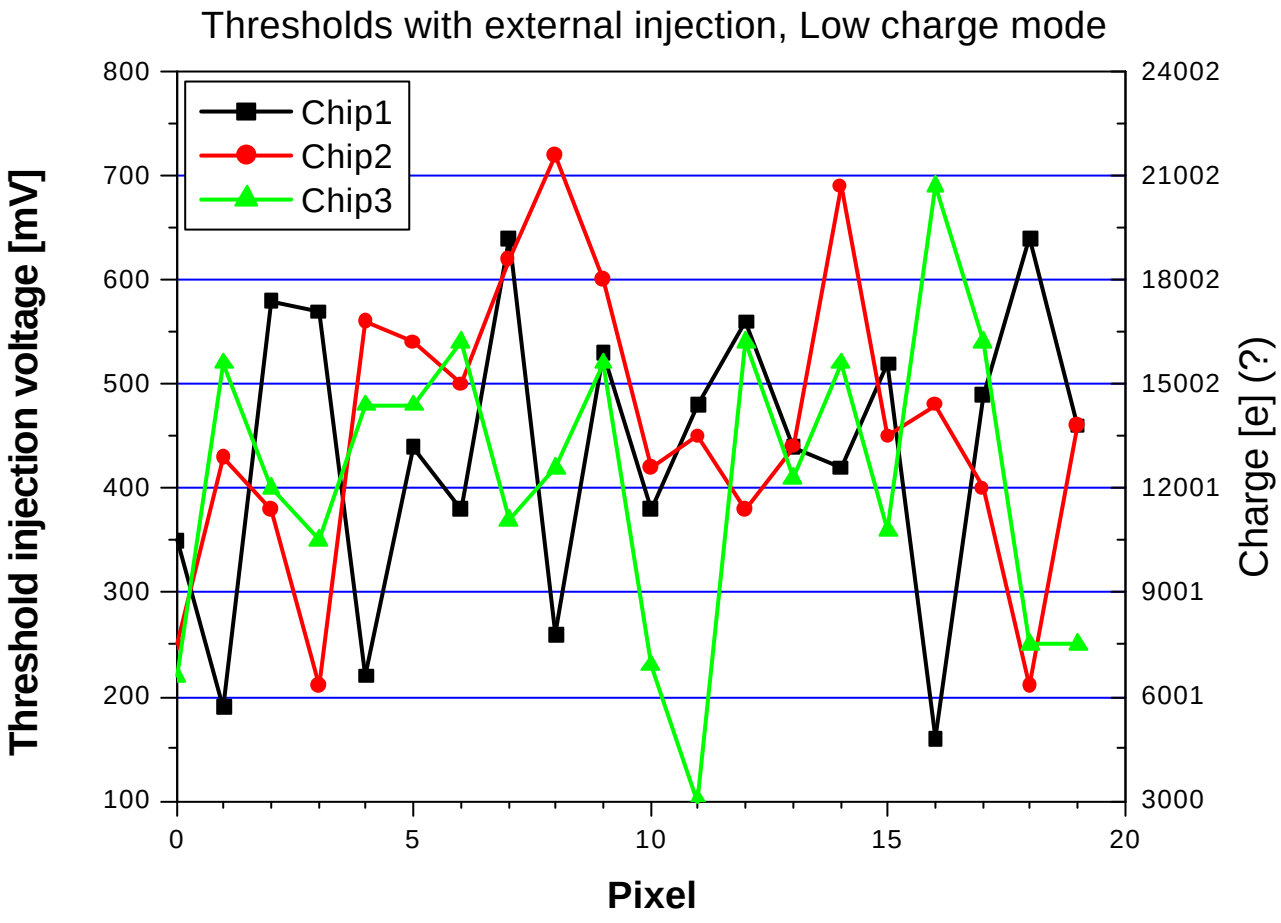
'ADC' for leakage current measurement

- A DAC is compared to the output of the leakage monitoring circuit.
- This effectively makes a 8 bit ADC.
- 8 Measurements are needed (successive approximation) to get correct value
- Linearity up to half scale is ok



Threshold dispersion in column

- Measure external injection voltage when Hitbus starts to fire (low mode)



Modification of standard cell library

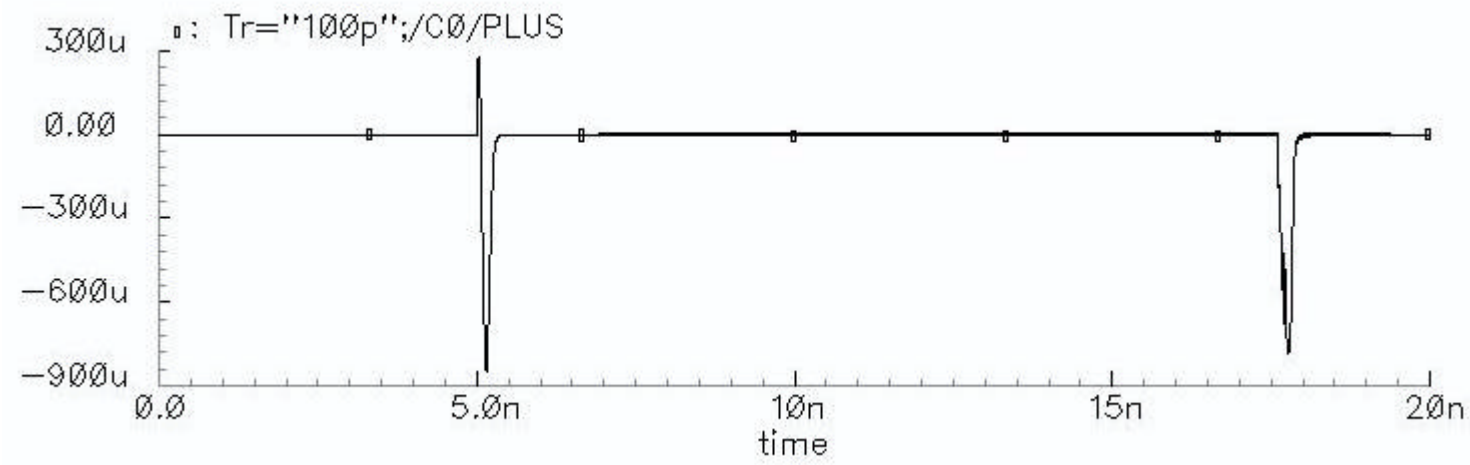
G. Comes, Bonn University

Problem with RAL library

- NMOS are large due to annular geometry. PMOS are 2-3 times NMOS.

⇒ Capacitive load is very large, Power consumption is large.
Ex.: One D-FF clocked at 40 MHz with T_r = 0.1ns needs 9µA average current.

⇒ Short circuit current (NMOS *and* PMOS conducting during transition) is large:
~ 700µA for T_r = 0.1ns. This will lead to large spikes on digital supply.
(Power supply charge needed for one period is ~ 0.2fC)



Supply current for a DFF clocked at 40 MHz with T_r = 0.1 ns

Modifications on library

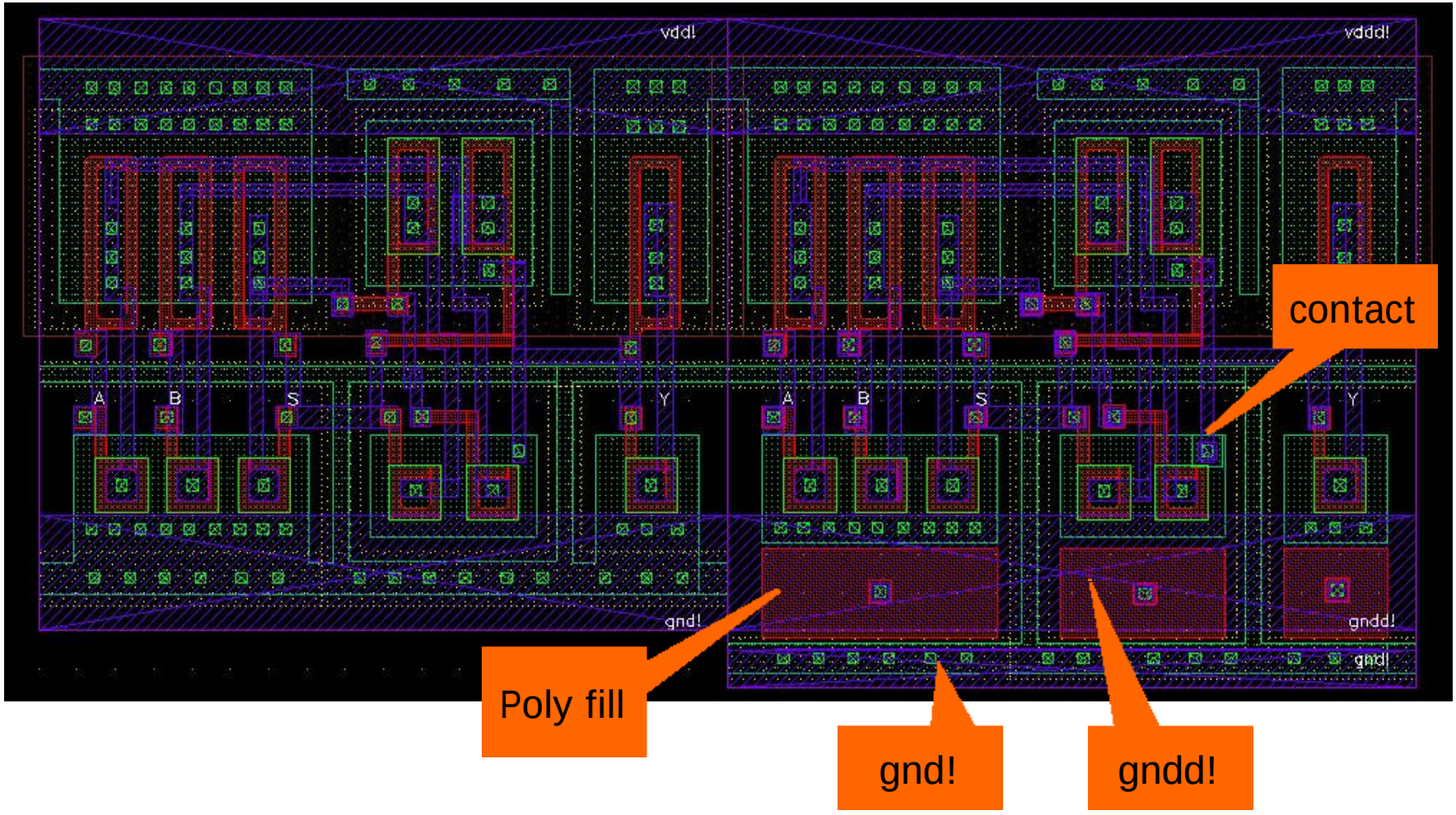
- Separate digital ground (gndd!) from substrate (gnd!) to keep substrate free of digital switching noise

- Make the layout compatible between two different 0.25µm technologies (IBM, TSMC):
  - Possibility to submit to both vendors
  - In particular access to MPW through MOSIS with fast turn around
  - This required modifications of Contacts, Vias, BP overlap etc.

- Respect locally the fill rules for poly, diffusion, metal1,...
  - No need to post process design after automatic P&R

- Cell height is increased by 1.5 µm (10%)

Example (MUX2)

CERN / RAL Library

Common Library