Pads Required

Pixel FE

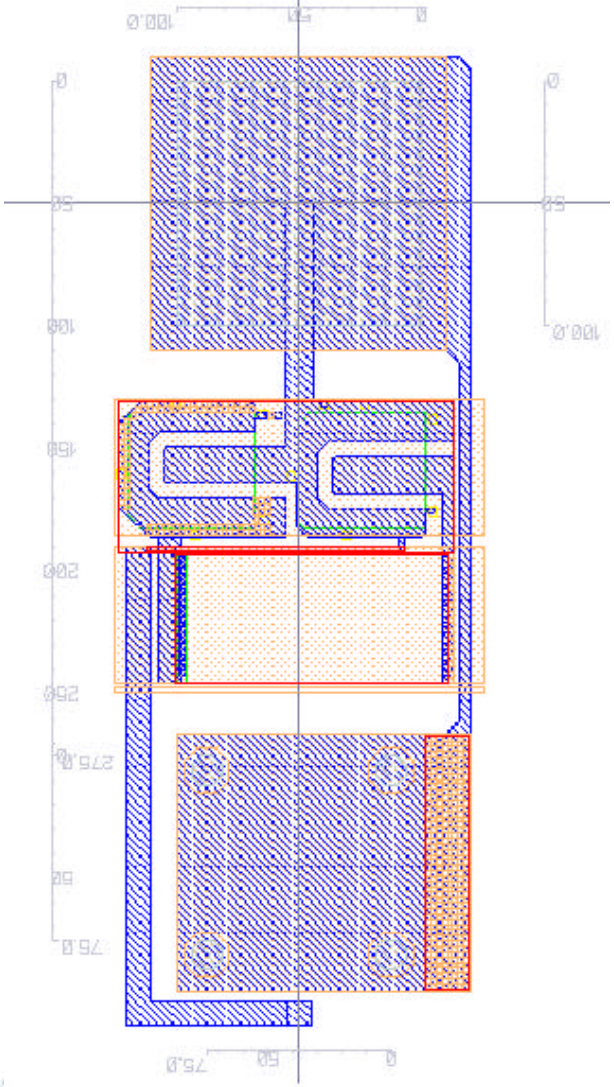
- Passive
- Power (clamp)
- Ground (2 types)
- CMOS In (+pullup/down)
- LVDS In
- LVDS Out (0.5 mA)

Pixel MCC

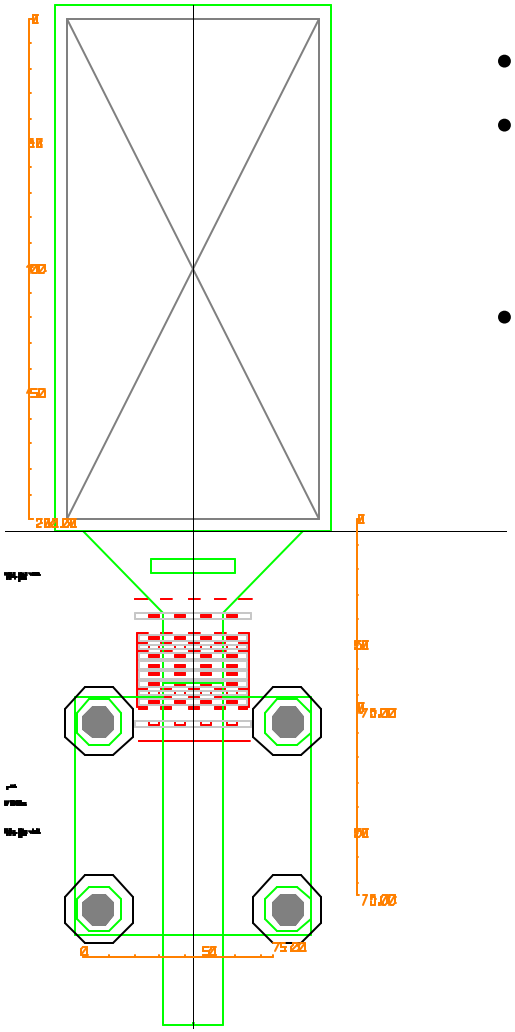
- Power (clamp)
- Ground
- CMOS In (+pullup/down)
- LVDS In
- LVDS In (integrated 500Ω)
- LVDS Out (3 mA)

Pad Geometry

DMILL

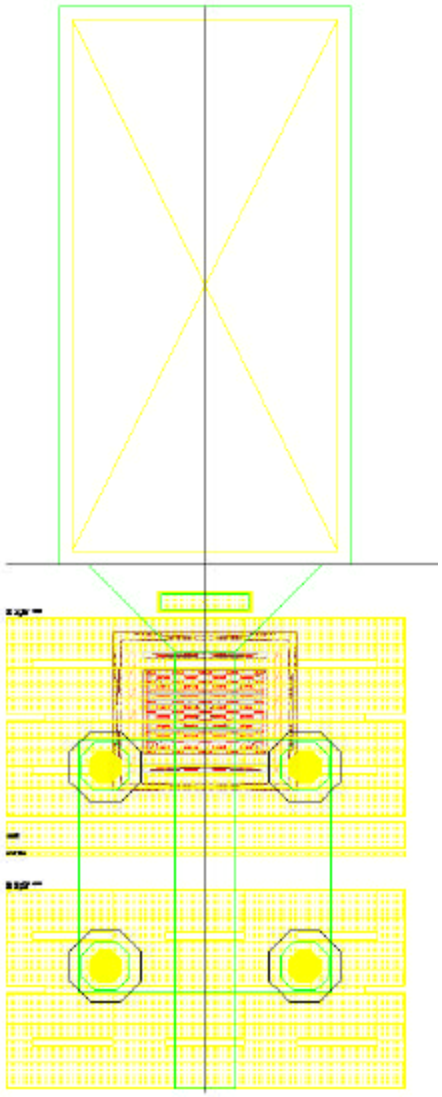


IBM



- MCM bump pads
- IBM: 100μ × 200μ
  (passivation opening)
  Separate test/bond locations
- DMILL: 100μ × 100μ

Pad Layout



M5 - Pad
M4 - VDDA
M3 - VDDA
M2 - GND
M1 - routing

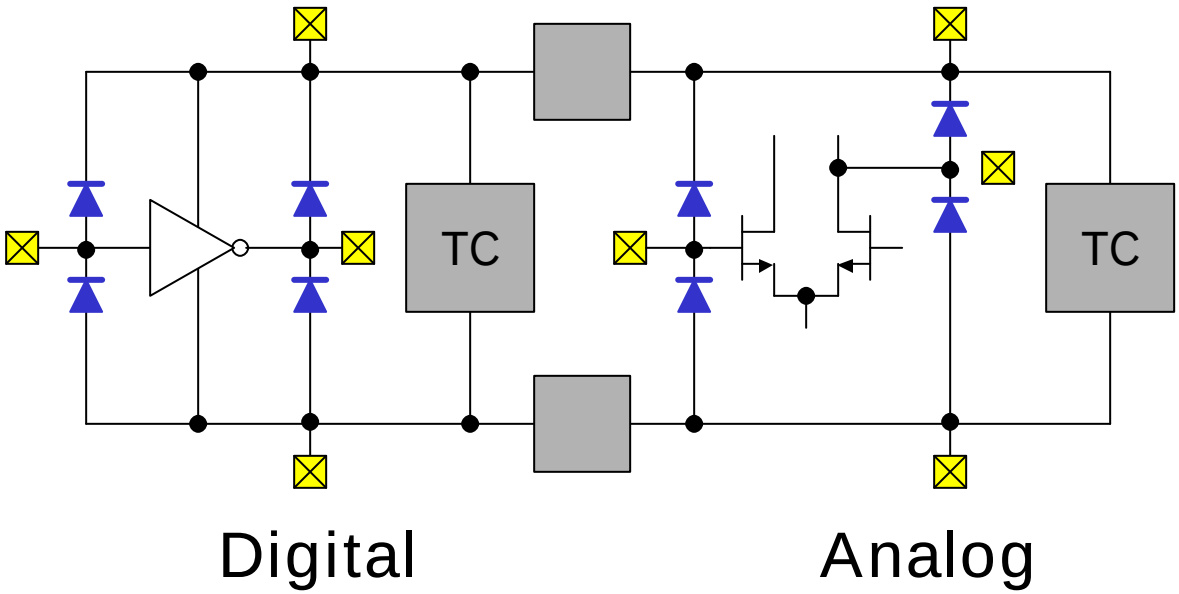
M5 - Pad
M4 - VDDD
M3 - VDDD
M2 - GND
M1 - routing

- 75μ rails
- 2 rails per voltage
- rails are ~ 0.5 Ω/mm

(M2..4 = 0.78 Ω/sq.)

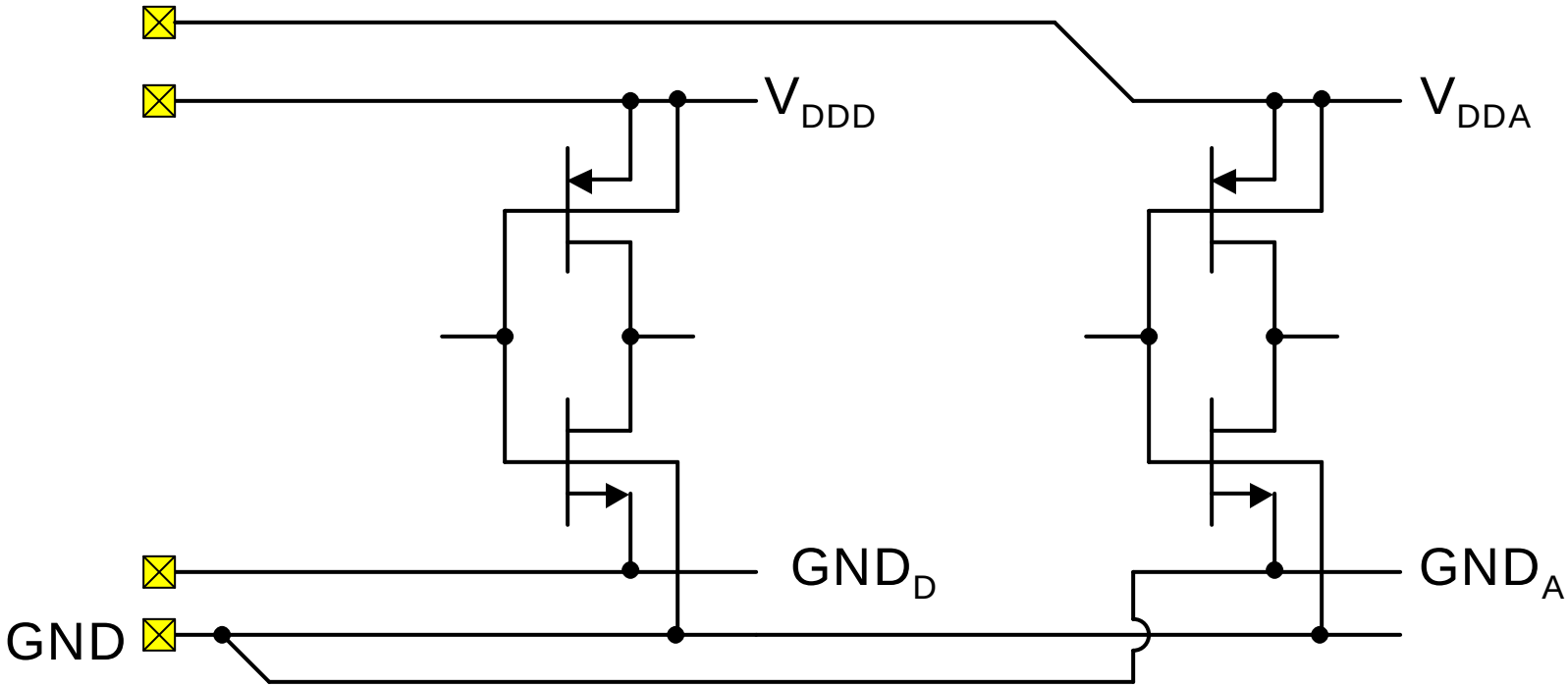
ESD Scheme – In principle

- Mixed-mode (see →)
- Power sequence independent
- V_{DDA} is a very sensitive node

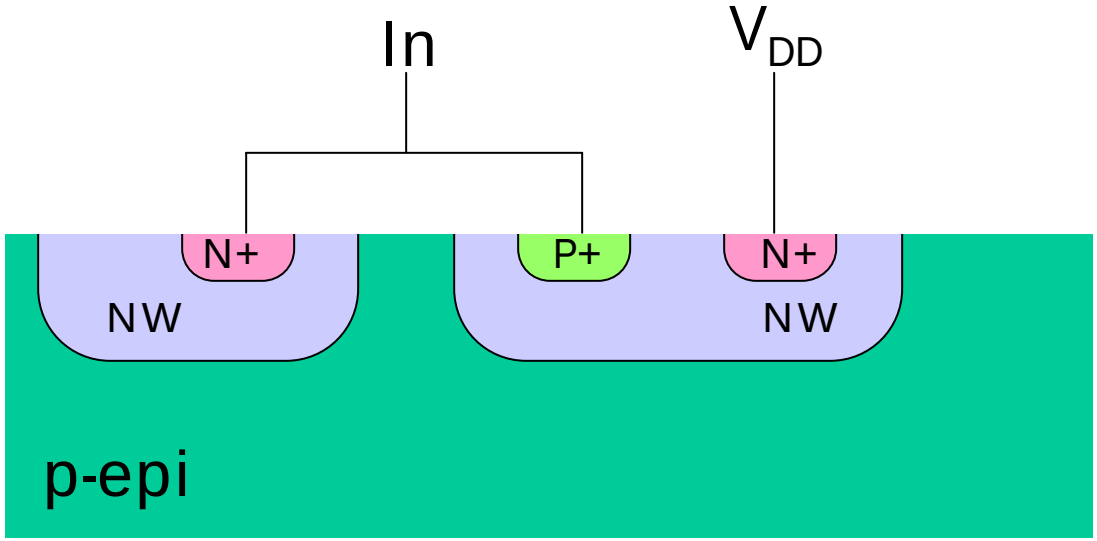


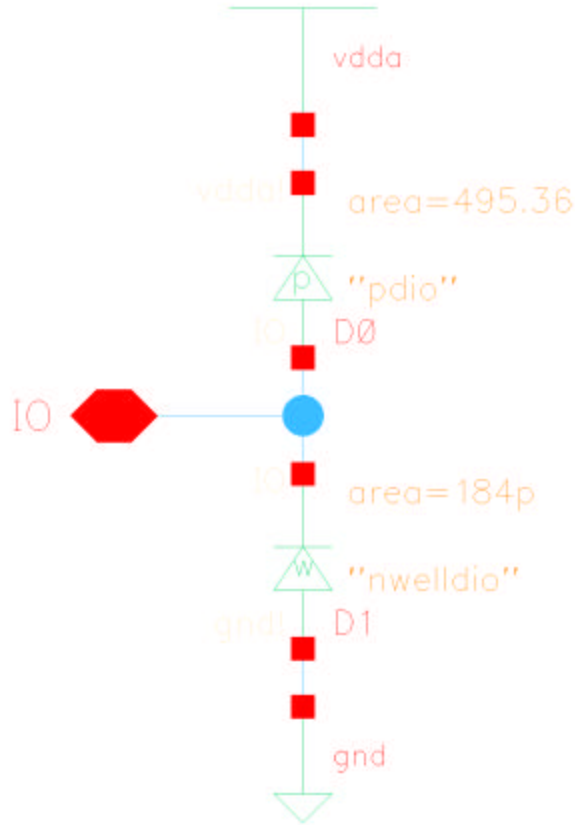
Mixed Mode

- 2 V_{DD}
- 2+1 V_{SS}



ESD Diodes





IBM – Substrate for ESD (–) node
(TSMC – MOS Diodes to metal traces)

IBM "kit"

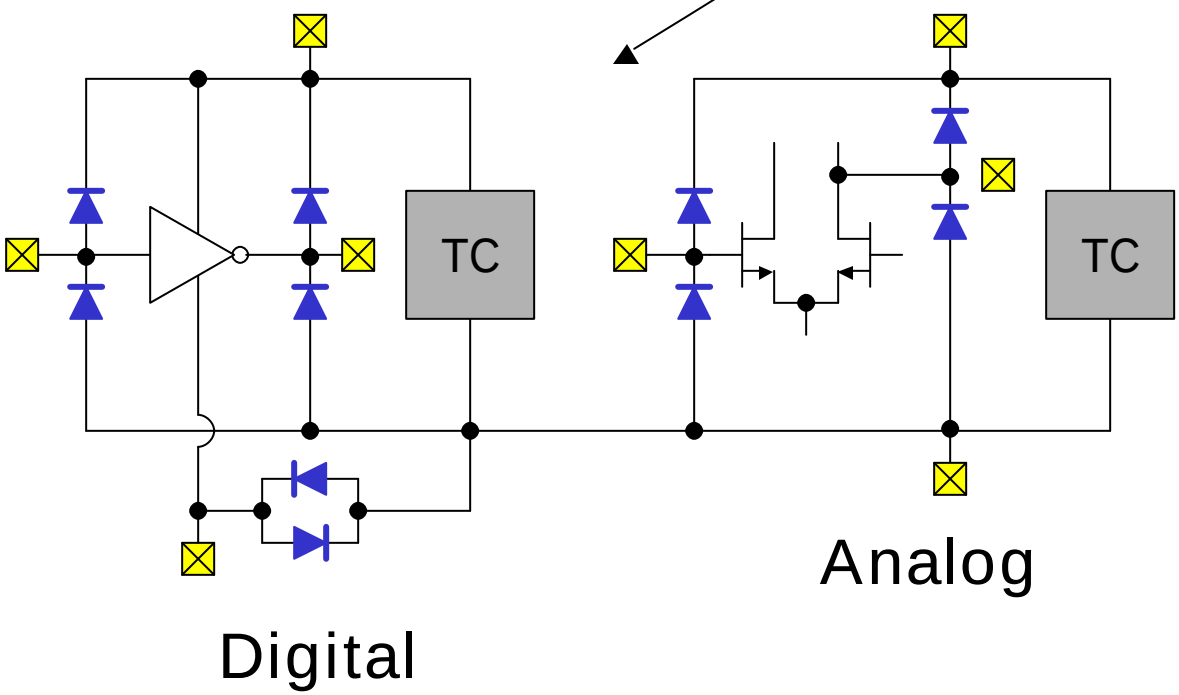
CMOS6SF ESD Design KIT

01/27/99 Version

Robert Gauthier
IBM Microelectronics
Phone: (802)769-5509
Fax: (802)769-9659

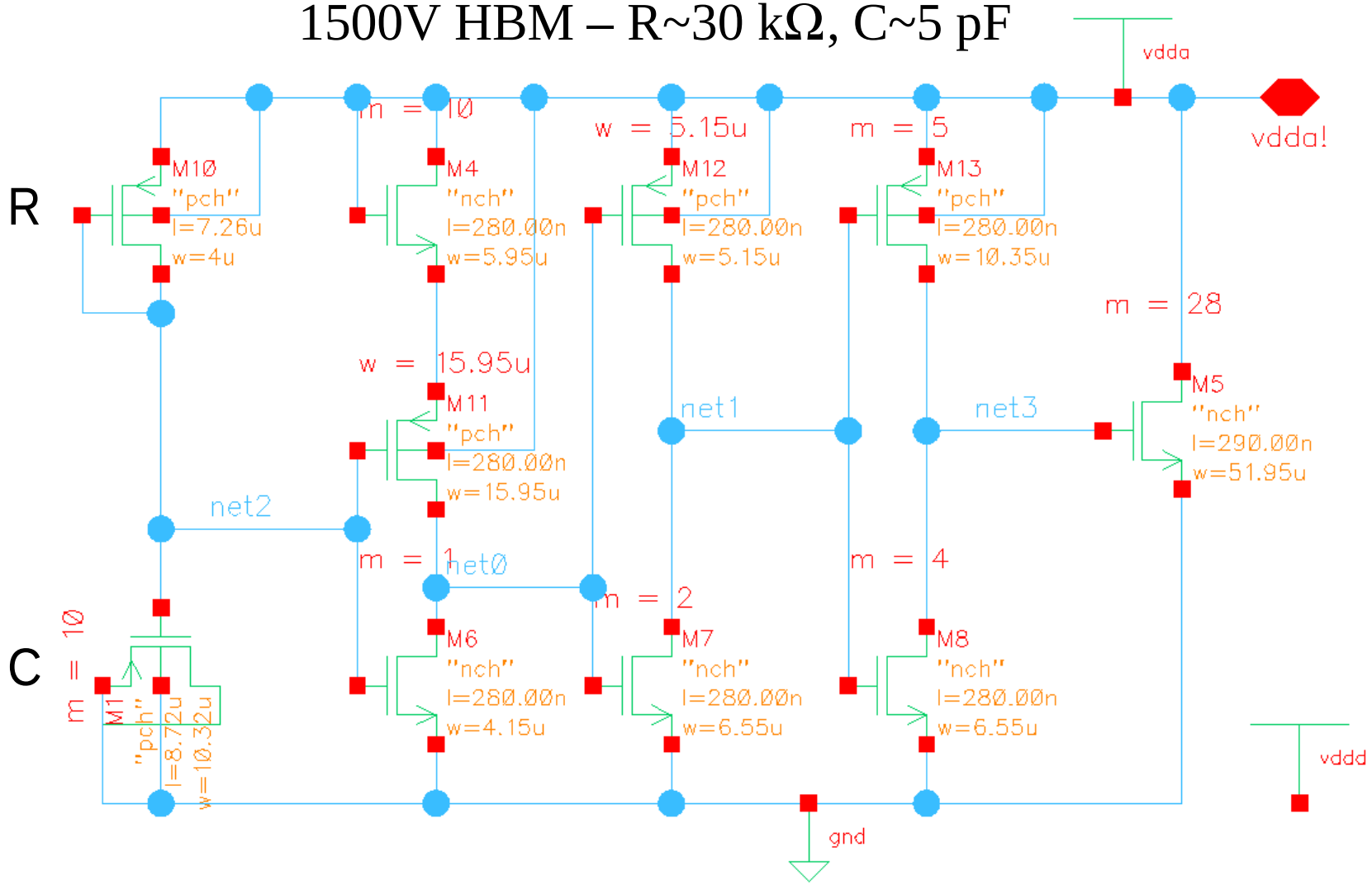
ESD Scheme – In practice

- Mixed-mode
- Power sequence independent
- V_{DDA} is a very sensitive node

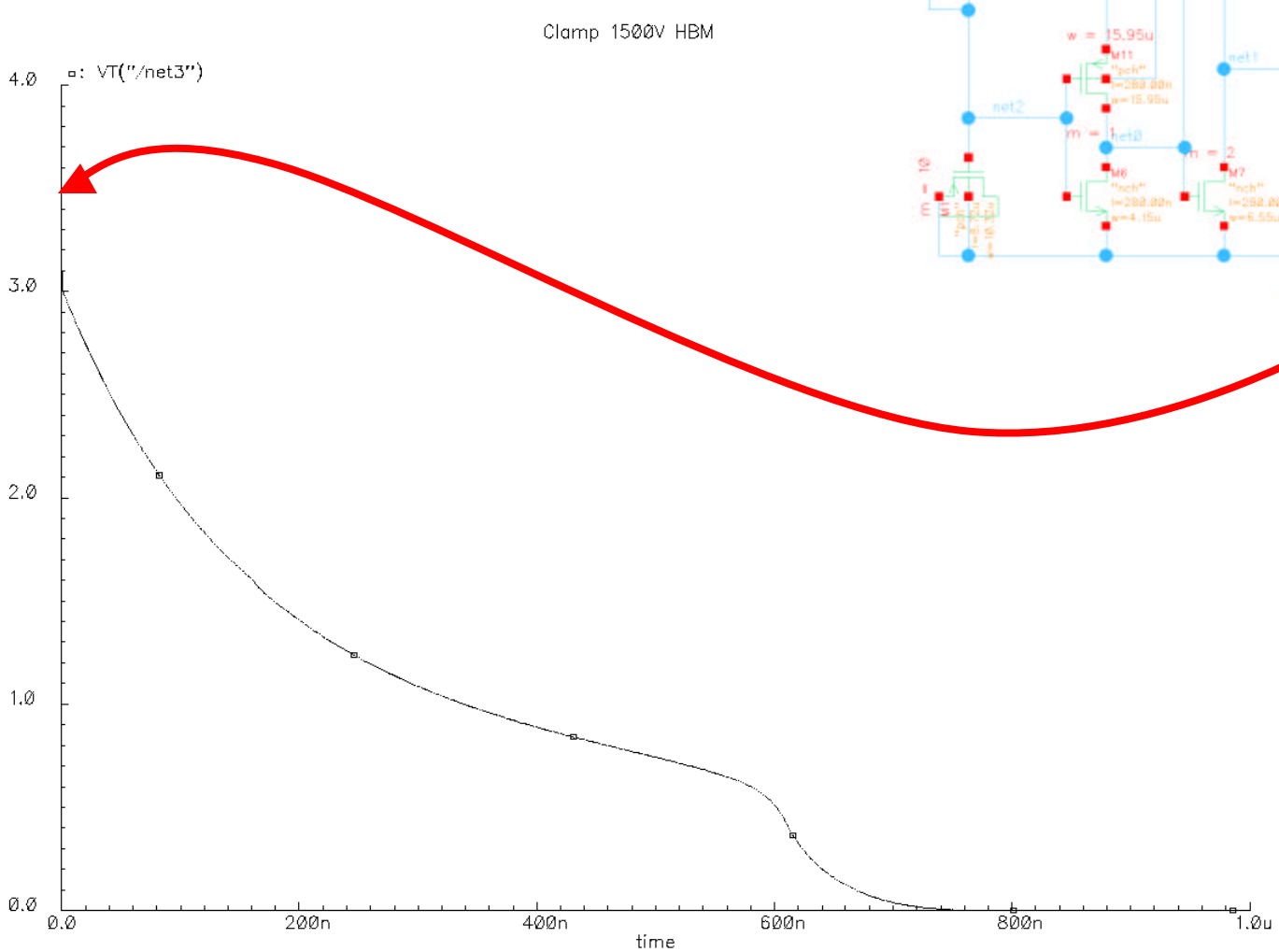


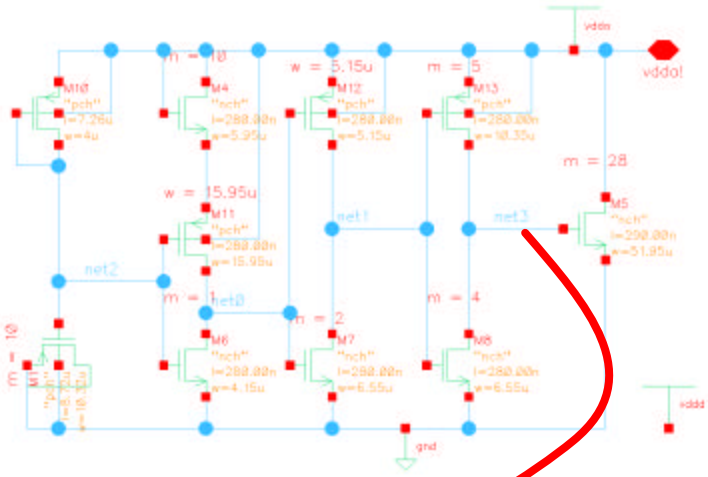
V_{DD} Clamp - Schematic

1500V HBM – R~30 kΩ, C~5 pF

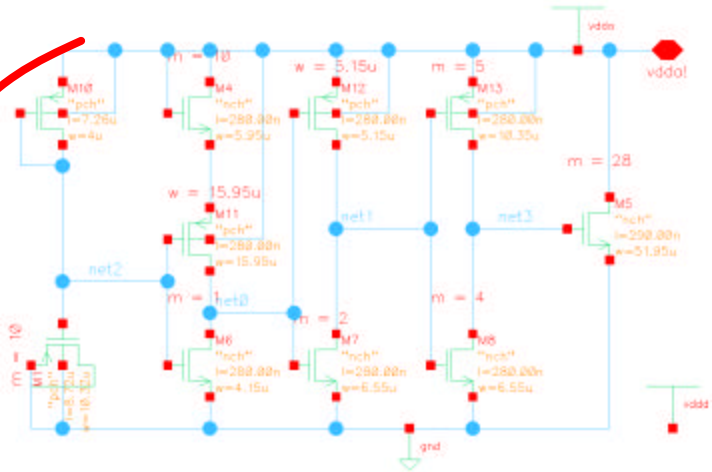


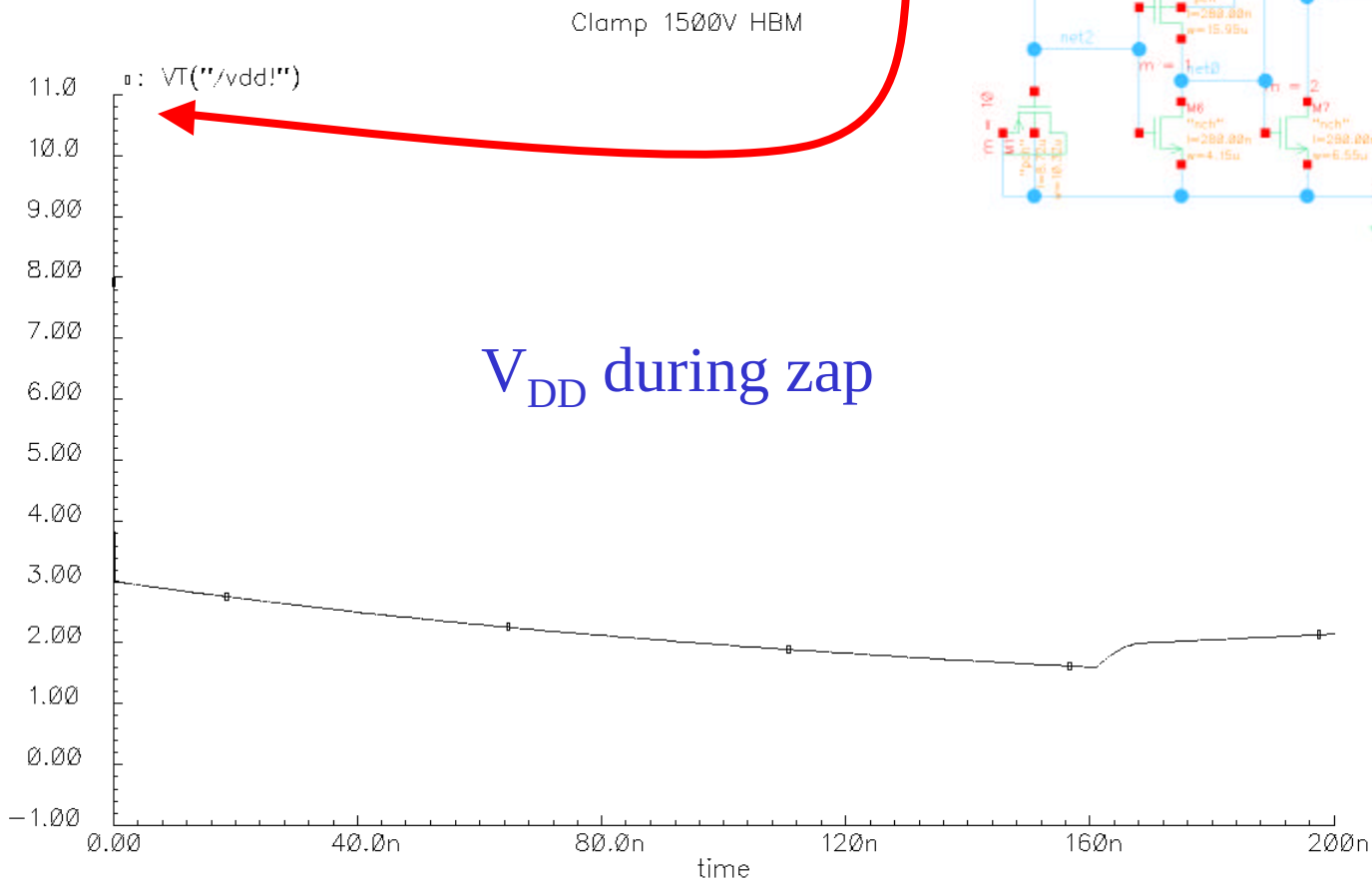
V_{DD} Clamp - Driver





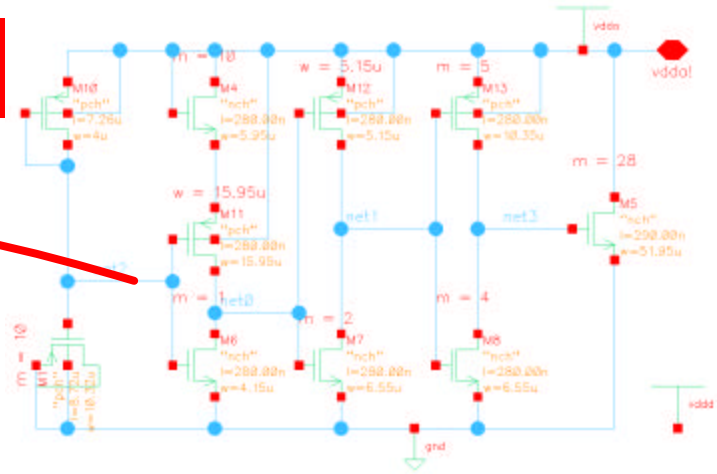
V_{DD} Clamp - V_{DD}

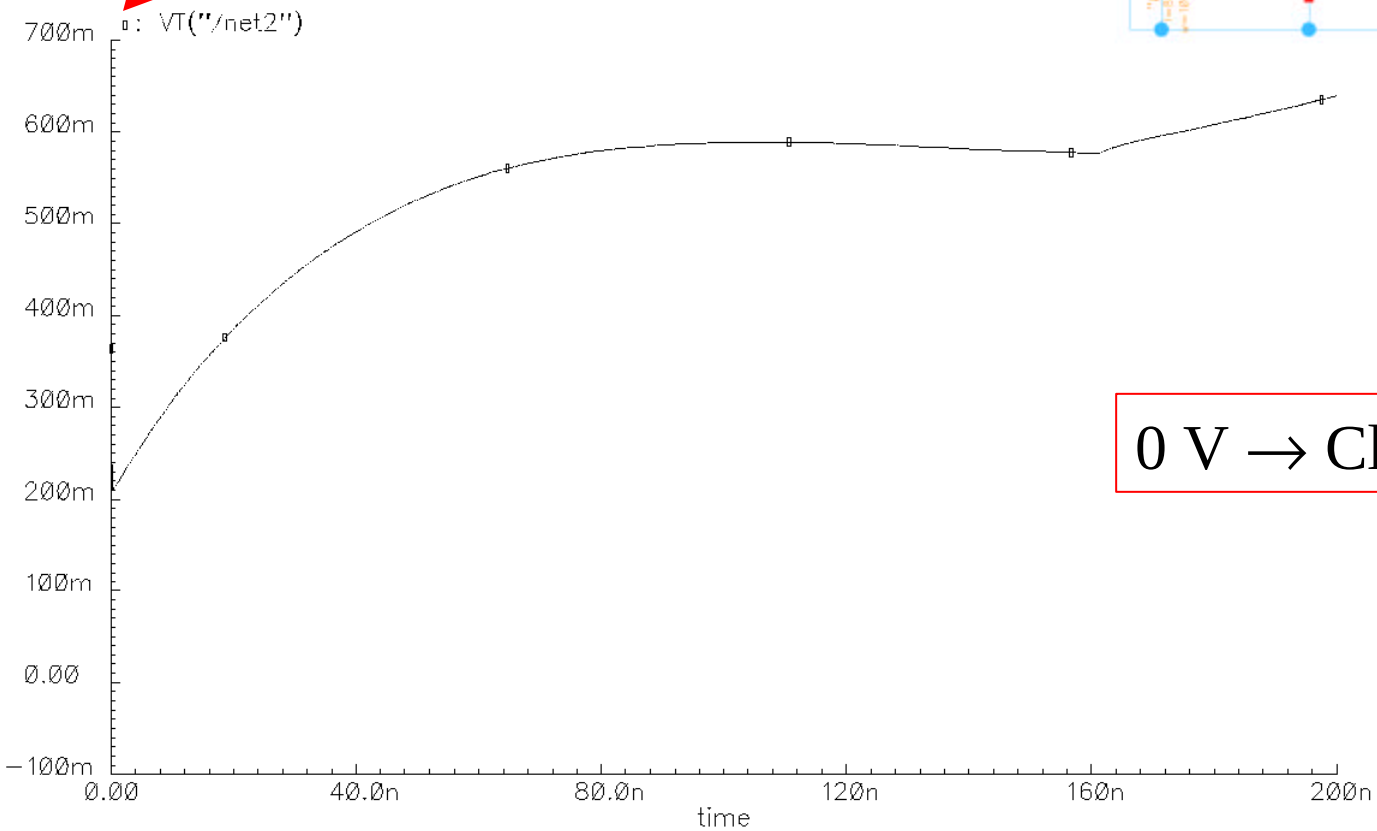




V_{DD} during zap

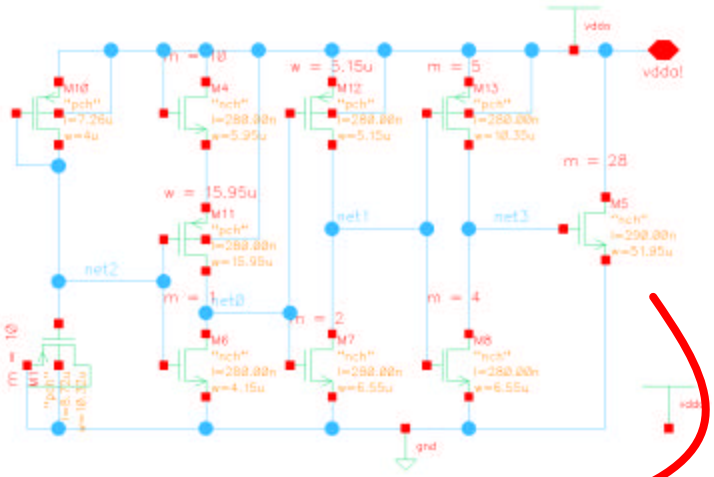
V_{DD} Clamp - On/Off

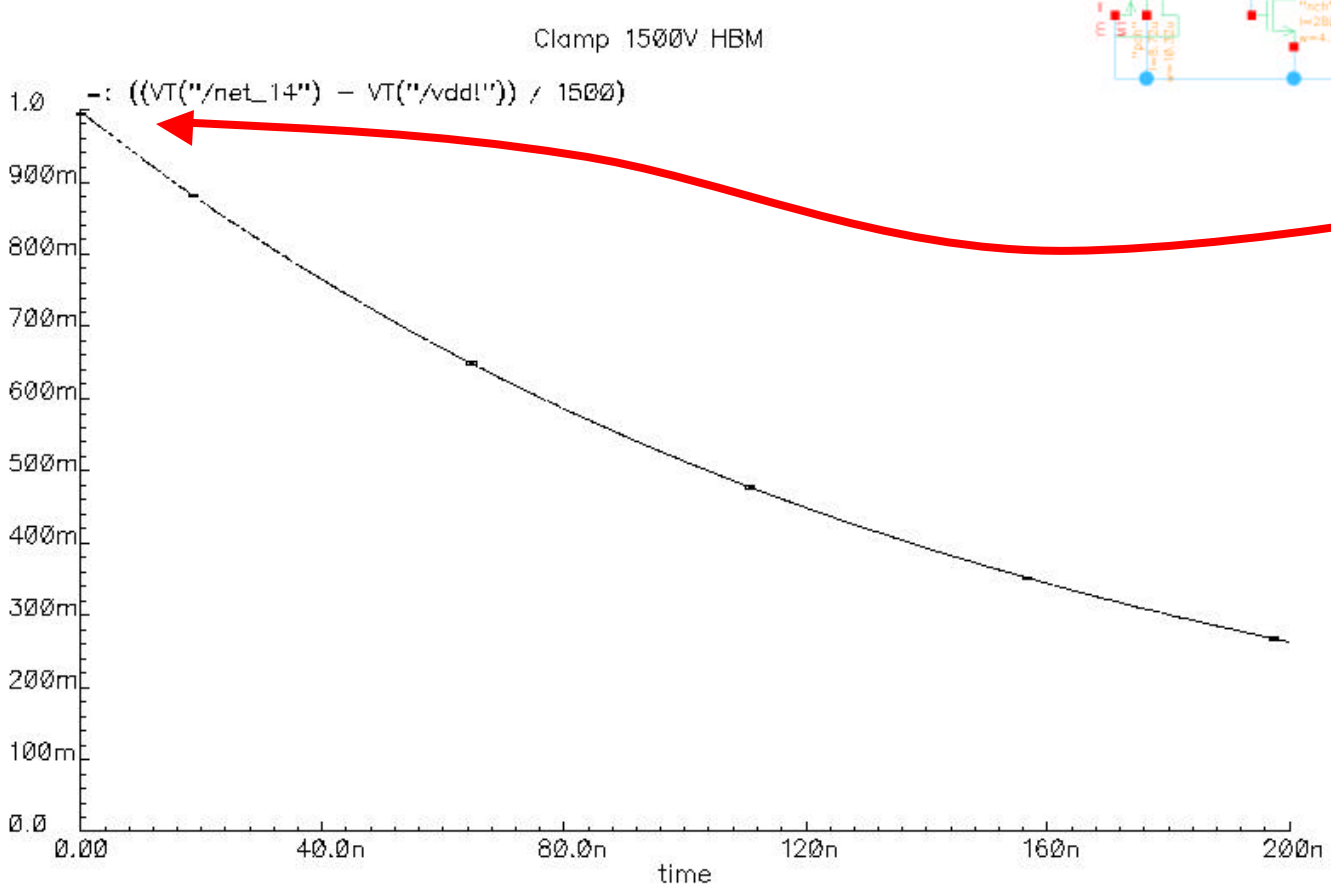




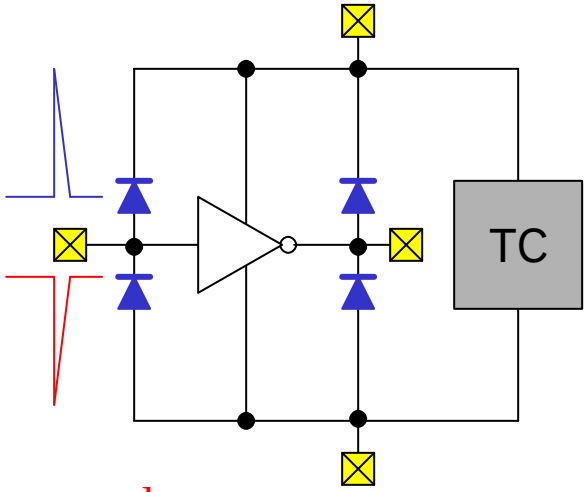
0 V → Clamp ON

V_{DD} Clamp - Current

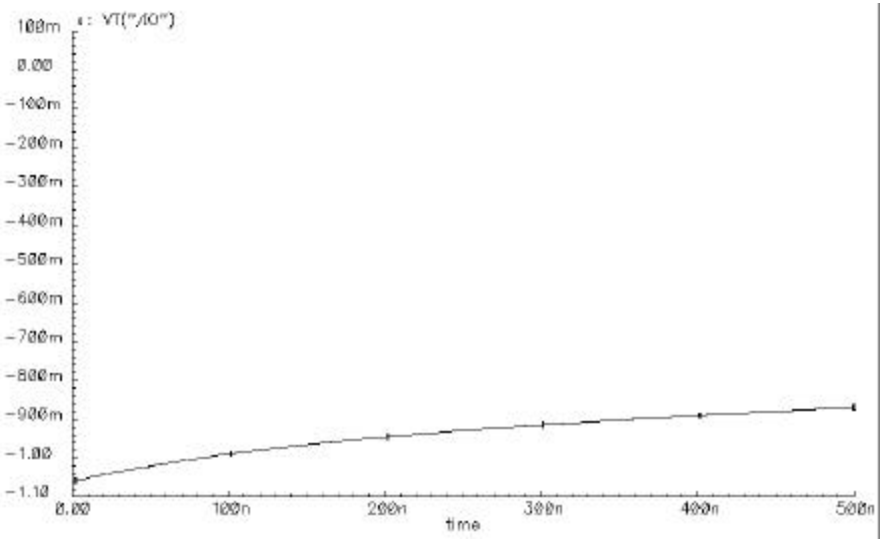




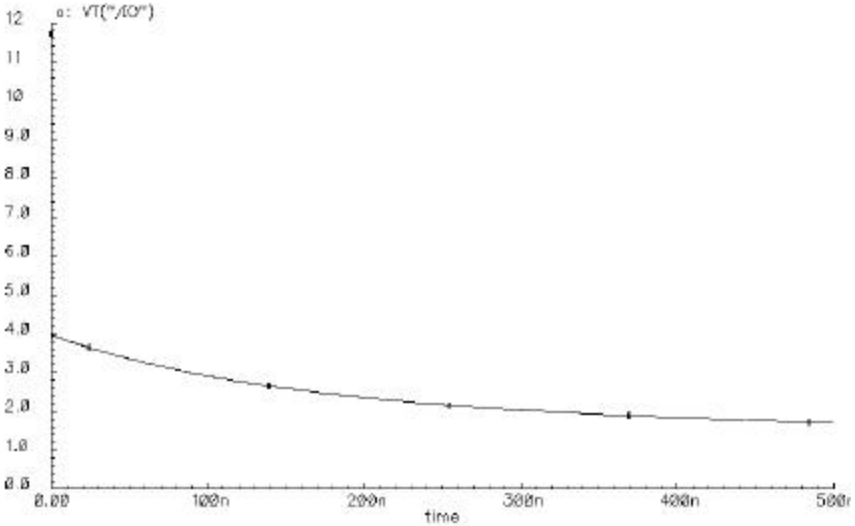
ESD Event Example



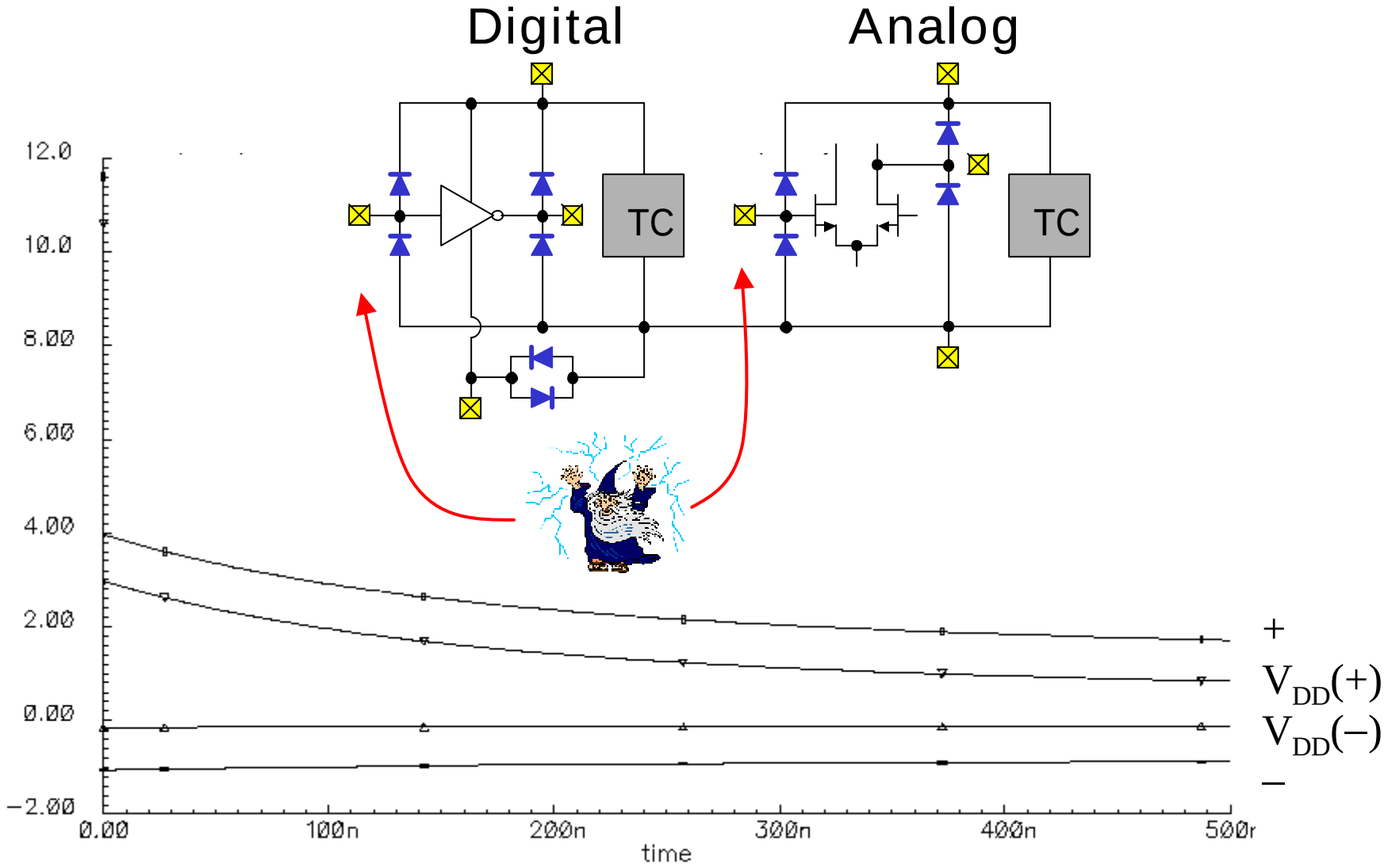
Negative spike w.r.t. gnd



Positive spike w.r.t. gnd

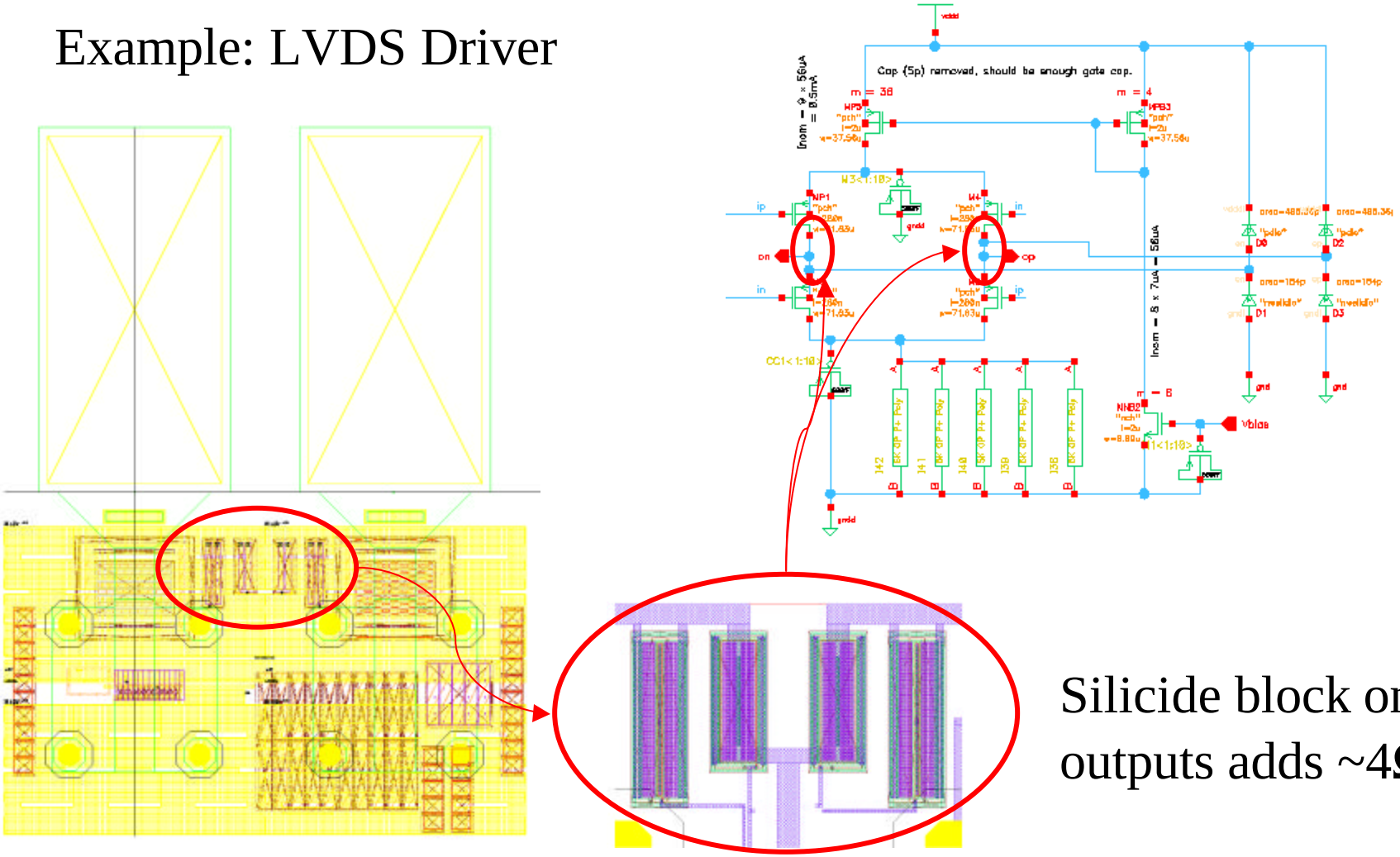


Worst Case


Digital
Analog
TC
TC
12.0
10.0
8.00
6.00
4.00
2.00
0.00
−2.00
0.00
100n
200n
300n
400n
500n
time
+
$V_{DD}(+)$
$V_{DD}(-)$
−

Output Pads - Resistive Outputs

Example: LVDS Driver

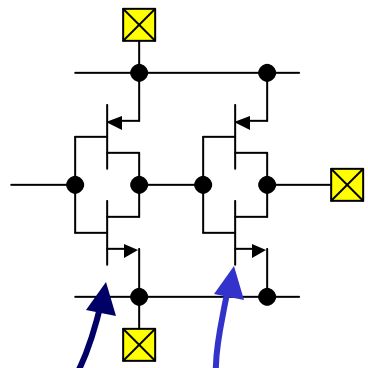


Silicide block on outputs adds ~4Ω

DRC

There are a number of layout rules specifically for devices that have an ESD function. These rules are not correctly and consistently checked by the DRCs we have available.

Example



These are “normal” transistors but generate errors because they are **also** connected to pads (V_{DD}, V_{SS})

These transistors need special layout considerations because they are connected to a pad

Approach: verify each *ESDnn* error by hand.

Conclusion

- Mixed-mode set of pixel FE pads
- Uses IBM ESD guidelines and devices (modified where needed for radiation hardness)
- Wide rails for good ESD conductivity (0.5 Ω/mm)
- Protection for zaps between any 2 pads (1500V HBM)