End Of Column Buffer

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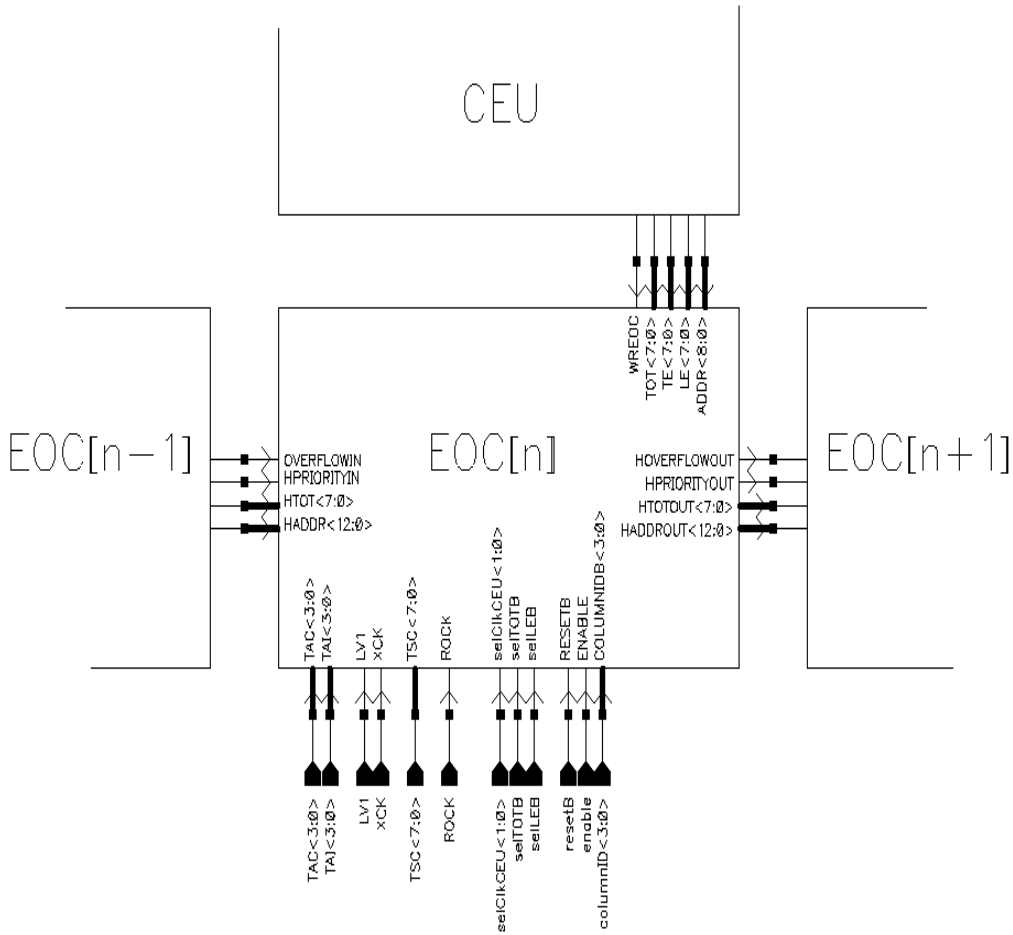
End of Column Buffer



Basic Function :

- Storage of pixel/event data (LE, TOT, address, TAI)

  40 EOC buffers

- Data reduction :

  Only data coinciding with the L1 Trigger is kept

- Read out : Transfer of data to BofC (Bottom of Chip) serializer

End of Column Buffer

Control/Data signals from CEU to EOC

Normal Operation

- WREOC : Write pulse, 25ns, 50ns, 100ns wide, depending on CEU clock speed (40/20/10/0 MHz)
- TOT<7:0> : Time Over Threshold data stored in RAM
- ADDRESS<8:0> : Pixel address stored in RAM
- LE<7:0> : Leading Edge data stored in LE-CAM

Test Mode (LE or TE stored in RAM instead of TOT)

- TE<7:0> : Trailing Edge data
- LE<7:0> : Leading Edge data

End of Column Buffer

Control/Data signals from Left Column

- HTOT<7:0> : TOT data from left column
- HADDRESS<13:0> : Address from left column
- HPRIORITYIN : Horizontal priority scan input

  HPRIORITYIN = 0, HTOT/HADDRESS is transferred to output

  HPRIORITYIN = 1, column data, if present will be transferred to output
- OVERFLOWIN : overflow bits of preceding (left) columns OR-ed

End of Column Buffer

Control/Data signals to Right Column

- HTOTOUT<7:0> : TOT output data
- HADDRESSOUT<13:0> : Address output data
- HPRIORITYOUT : Horizontal priority scan output

  HPRIORITYOUT = 0, current or left column has priority

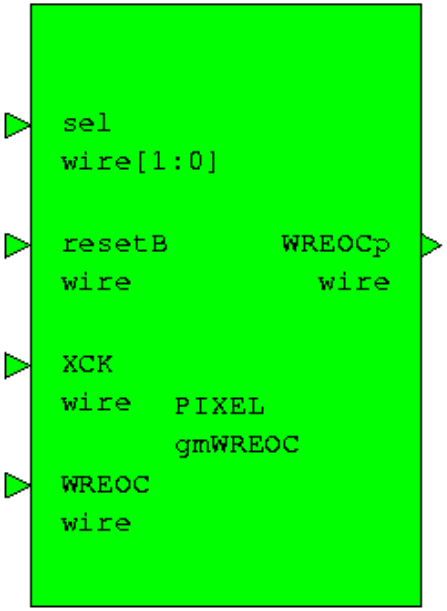
  HPRIORITYOUT = 1, priority transferred to right column
- OVERFLOWOUT : overflow bits of left columns and current column OR-ed

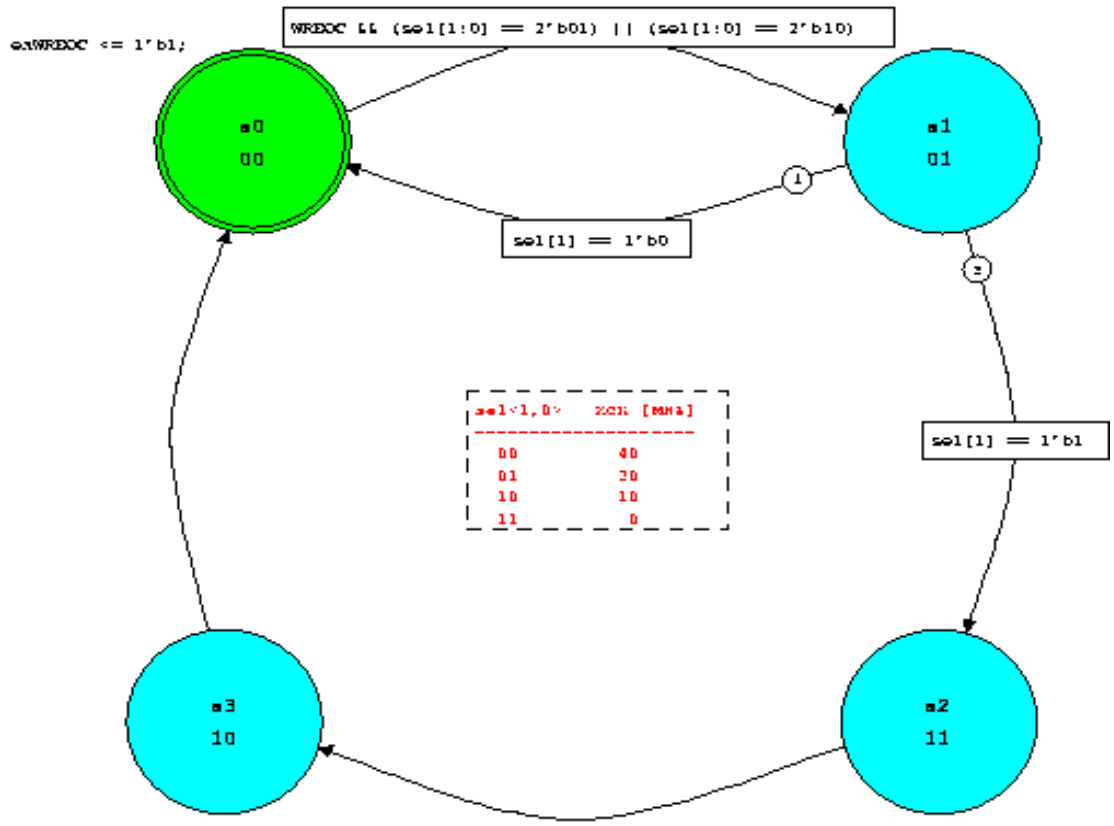
End of Column Buffer

Control signals from Bottom of Chip

- XCK : 40 MHz clock
- resetB : Reset, active low
- LV1 : Level1 trigger
- ROCK : Read Out ClocK, initiates read out sequence
- TSC<7:0> : Time Stamp Compare (LE – Latency)
- TAI<3:0> : Trigger Address Index
- TAC<3:0> : Trigger Address Compare
- ENABLE : Enable Column
- selTOTB : selTOTB = 0, TOT stored in RAM
- selLEB : selLEB = 0, LE stored in RAM
- selClkCEU : CEU clock speed (40/20/10/0 MHz)

Write Pulse Generator





Signals Status

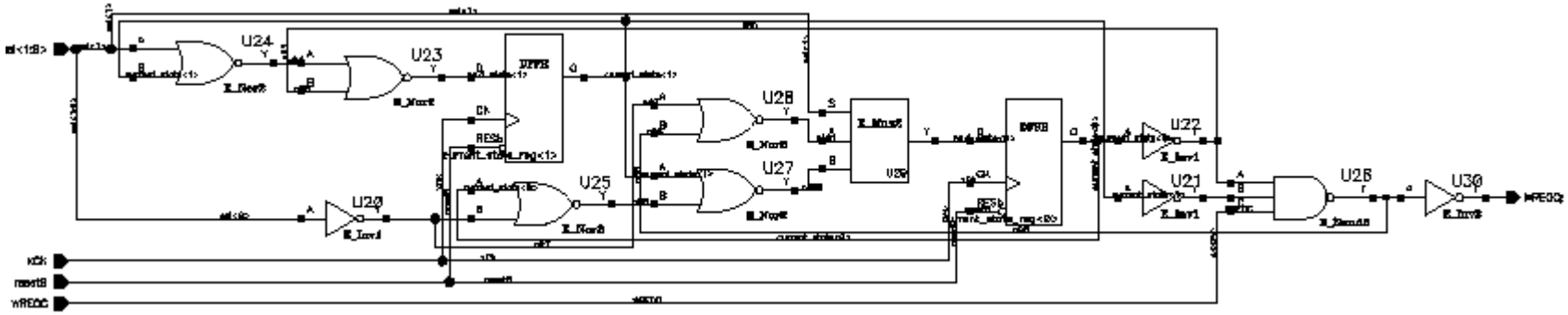
SIGNAL	SCOPE	DEFAULT	RESET	STATUS
WREOCp	OUT			COMB
gmWREOC	INT	1'b0		COMB

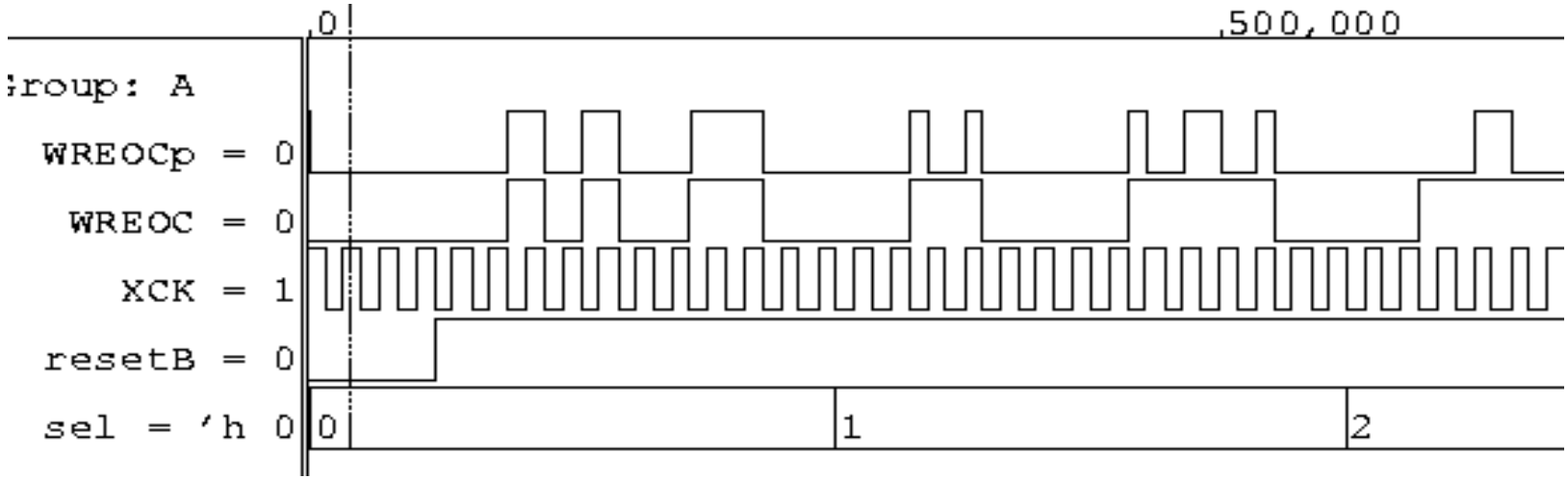
Module Declarations

```
reg gmWREOC;
assign WREOCp = gmWREOC & WREOC;
```

Compiler Directives

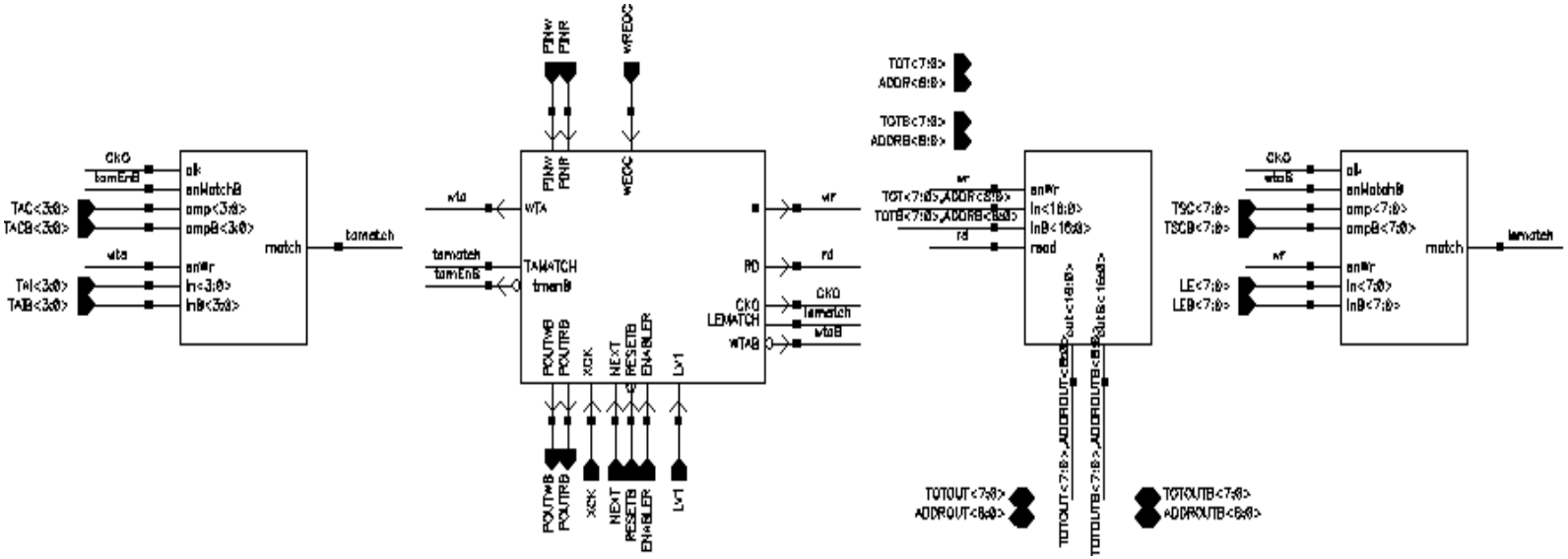
Write Pulse Generator





End of Column Buffer

Trigger Index CAM (4 bit) EOC Controller TOT, Address RAM (17 bit) Leading Edge CAM (8 bit)

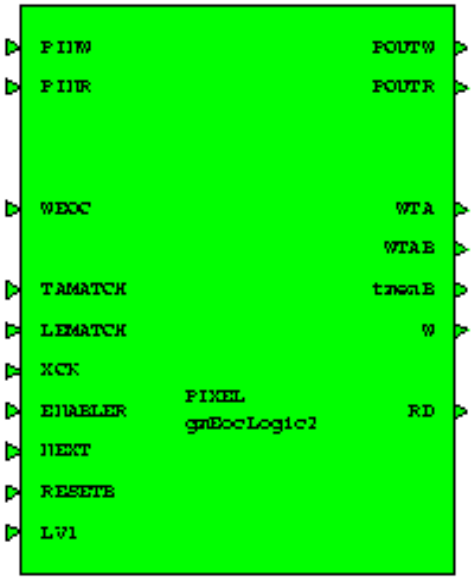


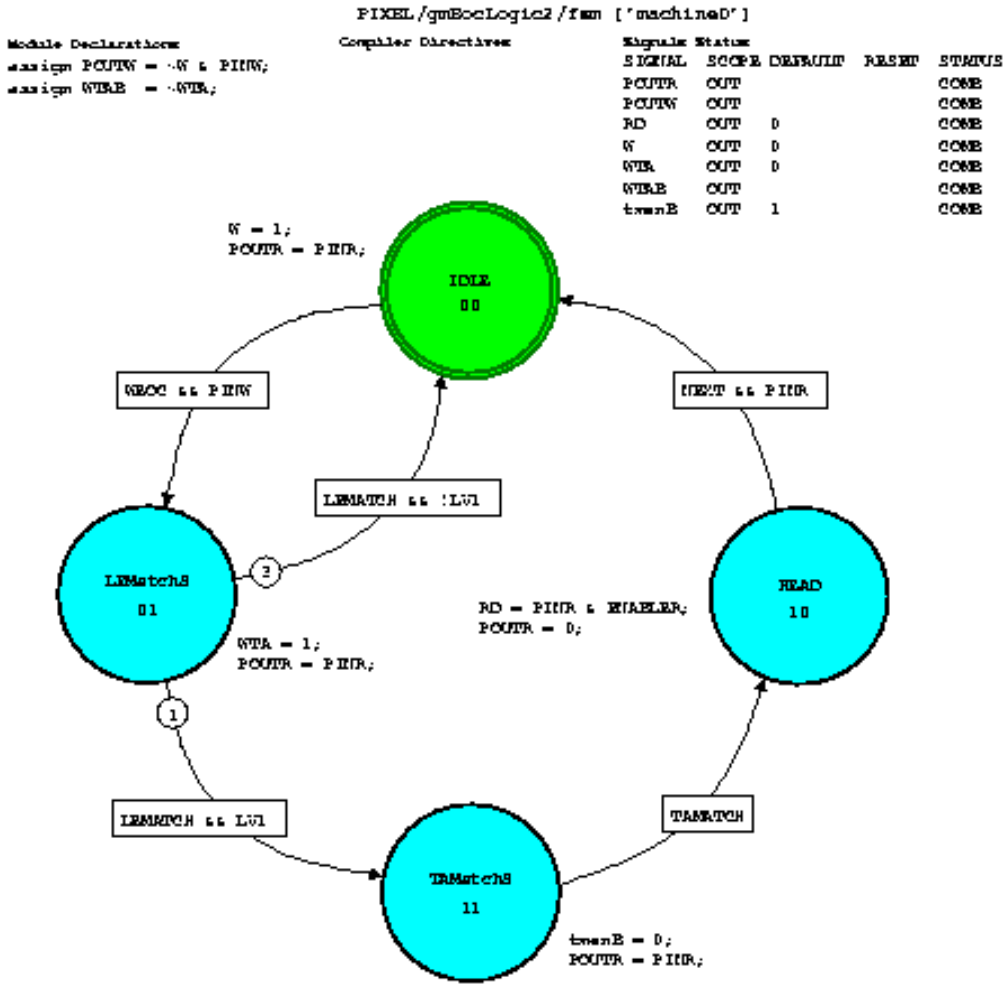
Critical path : PINW/POUTW (Write Priority Scan) has to ripple through 40 levels of logic to find empty buffer (worst case)

Hspice simulation, max. delay: 4-5 ns (typical, 2V VDD)

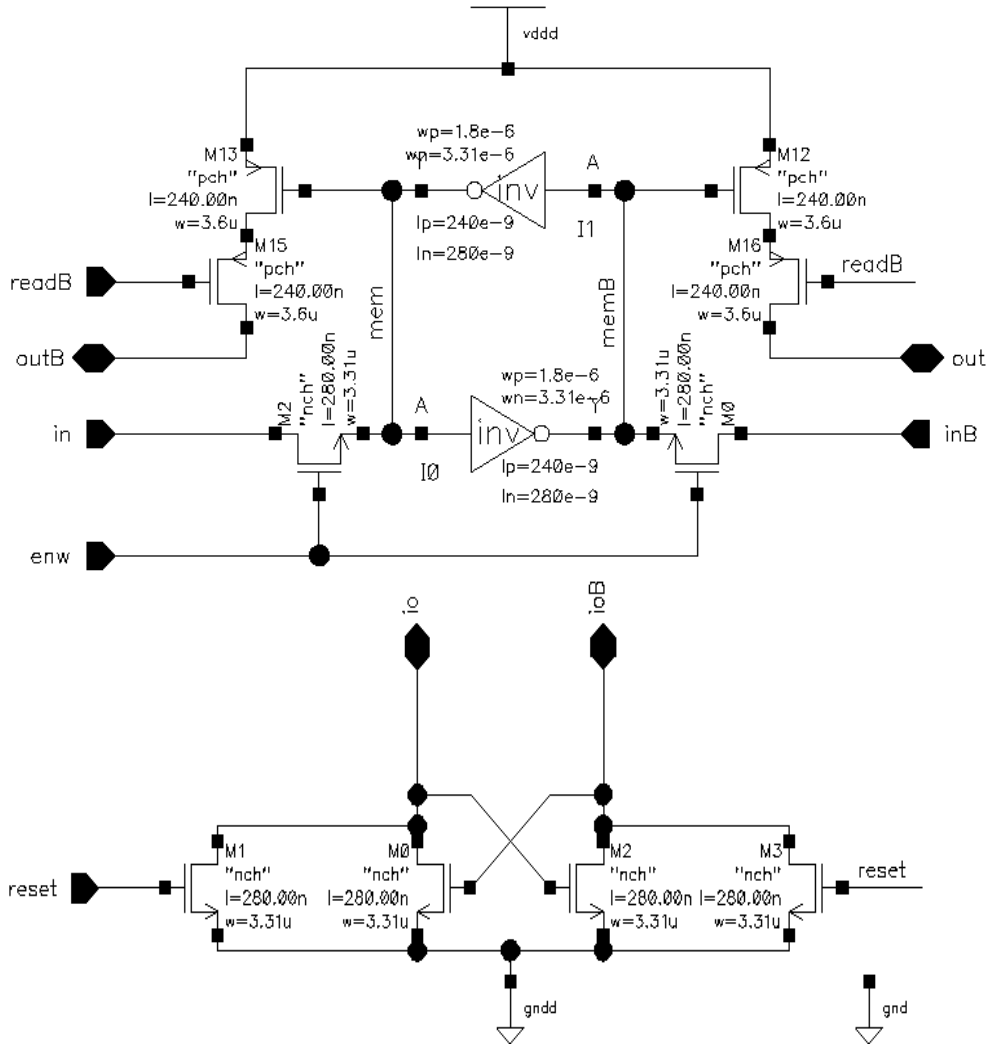
15ns (-3 sigma models, 1.6V VDD)

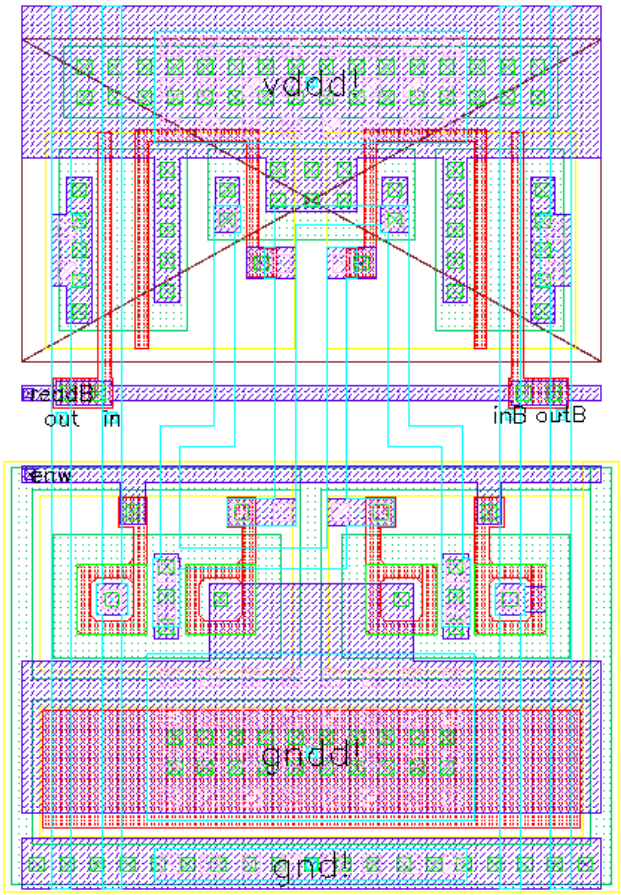
EOC Controller



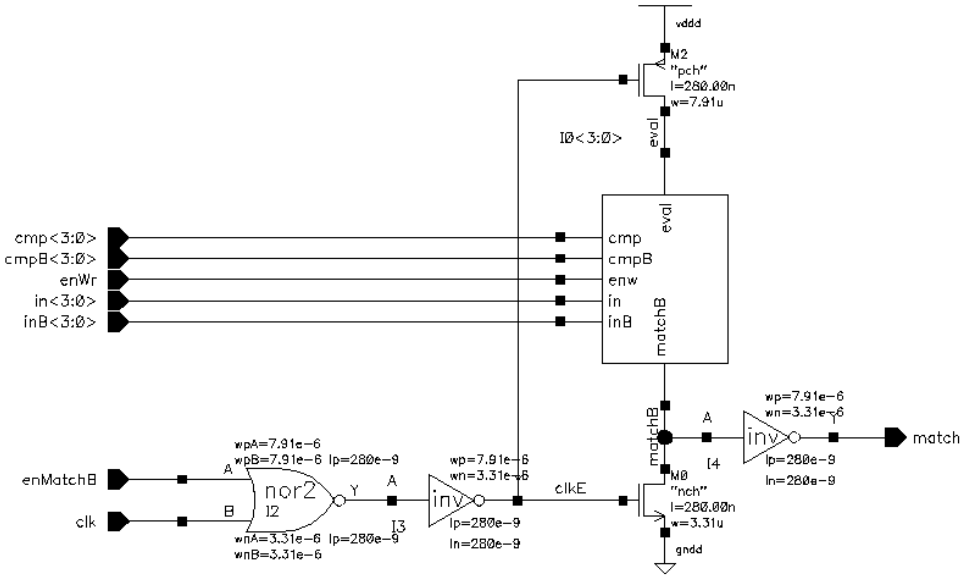


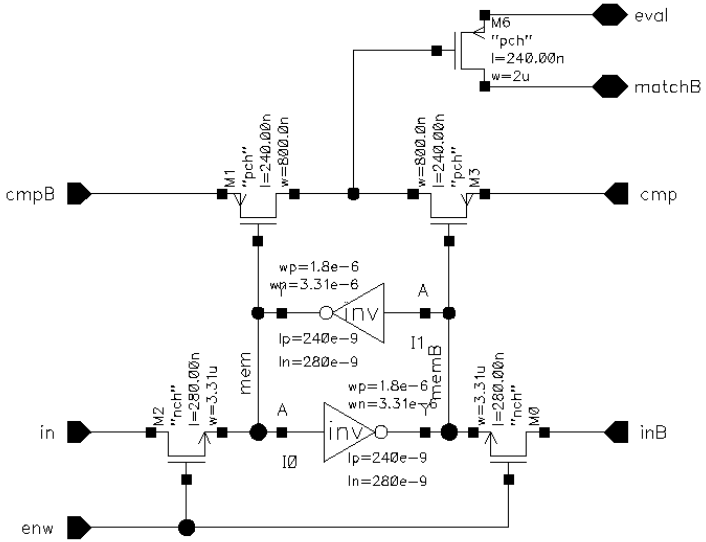
RAM Cell

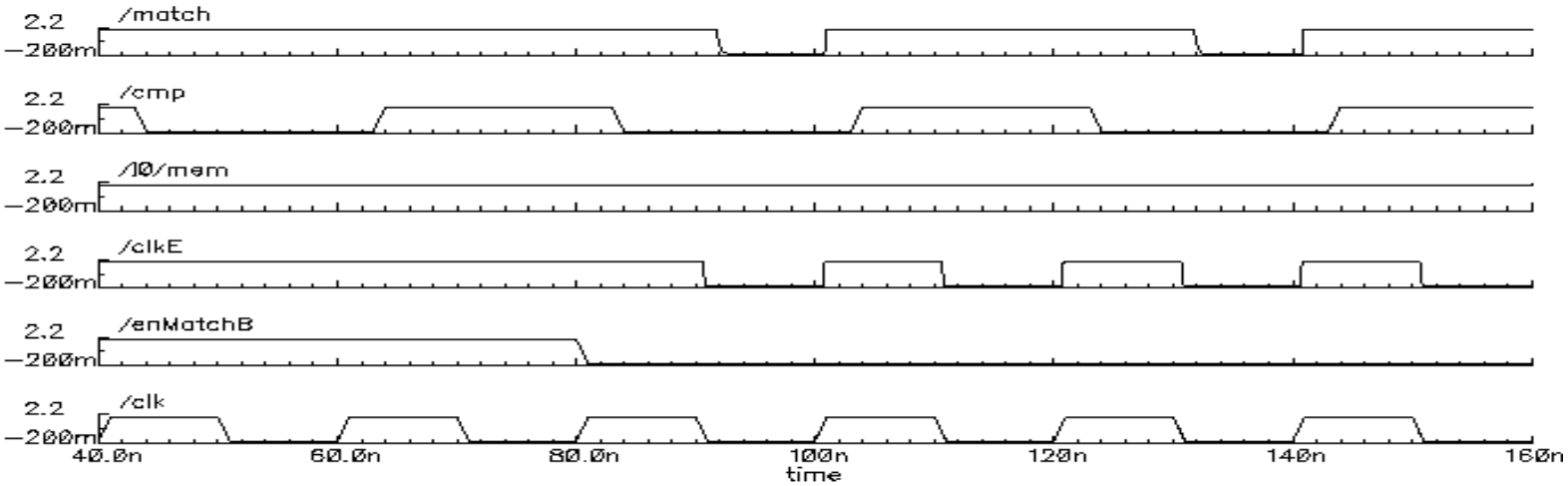

vddd
M13
"pch"
l=240.00n
w=3.6u
wp=1.8e-6
wn=3.31e-6
inv
A
M12
"pch"
l=240.00n
w=3.6u
lp=240e-9
ln=280e-9
I1
M15
"pch"
l=240.00n
w=3.6u
M16
"pch"
l=240.00n
w=3.6u
readB
readB
outB
out
mem
memB
M2
"nch"
l=280.00n
w=3.31u
wp=1.8e-6
wn=3.31e-6
w=3.31u
l=280.00n
"nch"
M0
in
inB
A
inv
I0
lp=240e-9
ln=280e-9
enw
io
ioB
M1
"nch"
l=280.00n
w=3.31u
M0
"nch"
l=280.00n
w=3.31u
M2
"nch"
l=280.00n
w=3.31u
M3
"nch"
l=280.00n
w=3.31u
reset
reset
gndd
gnd


vddd
readB
out
in
inB
outB
enw
gndd
gndd

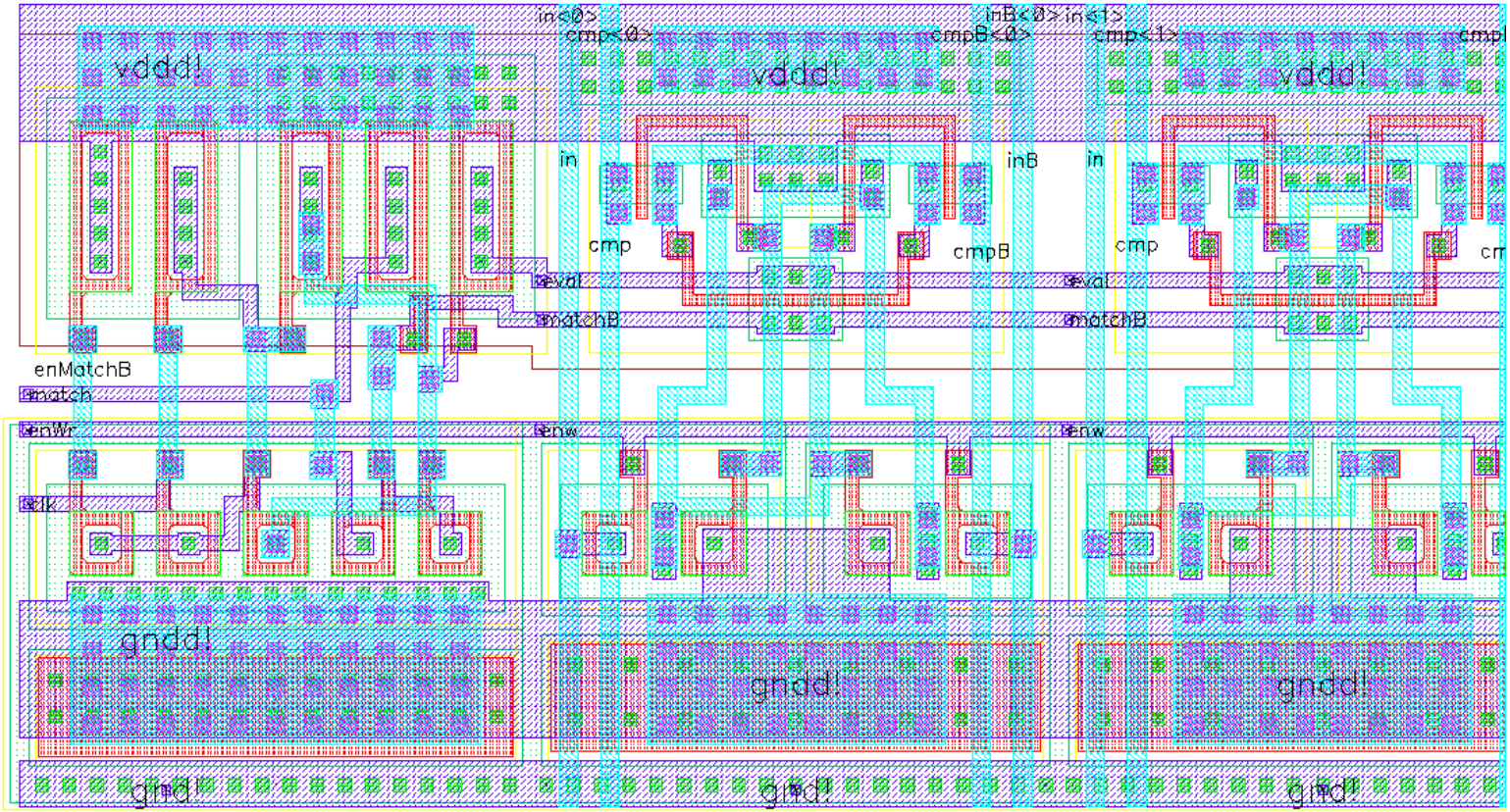
Leading Edge/Trigger Index CAM



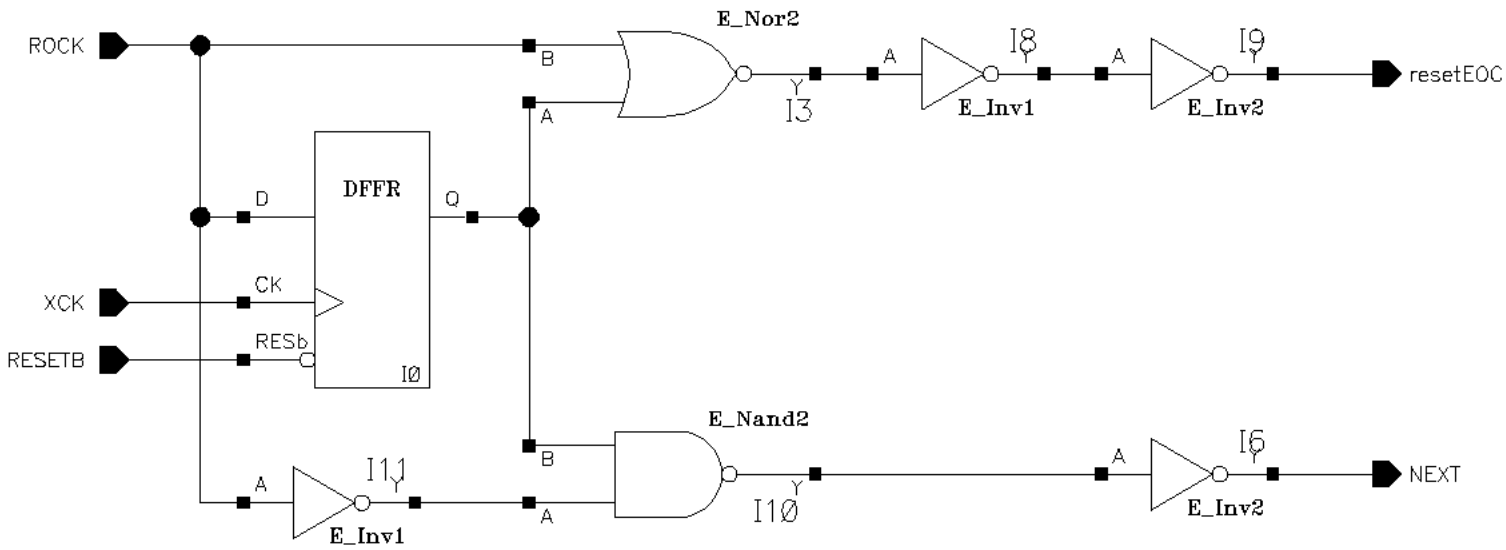


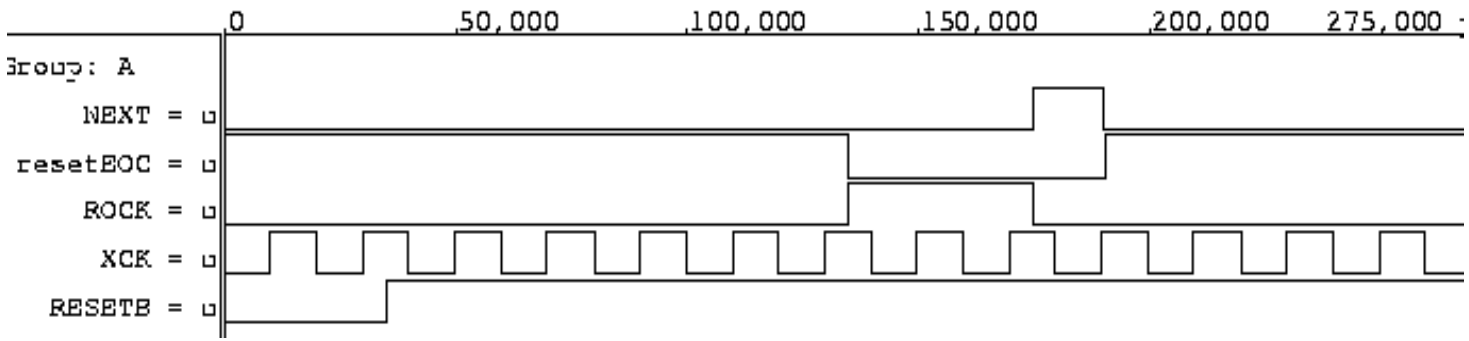


Trigger Index CAM



EOC Read Pulse Generator

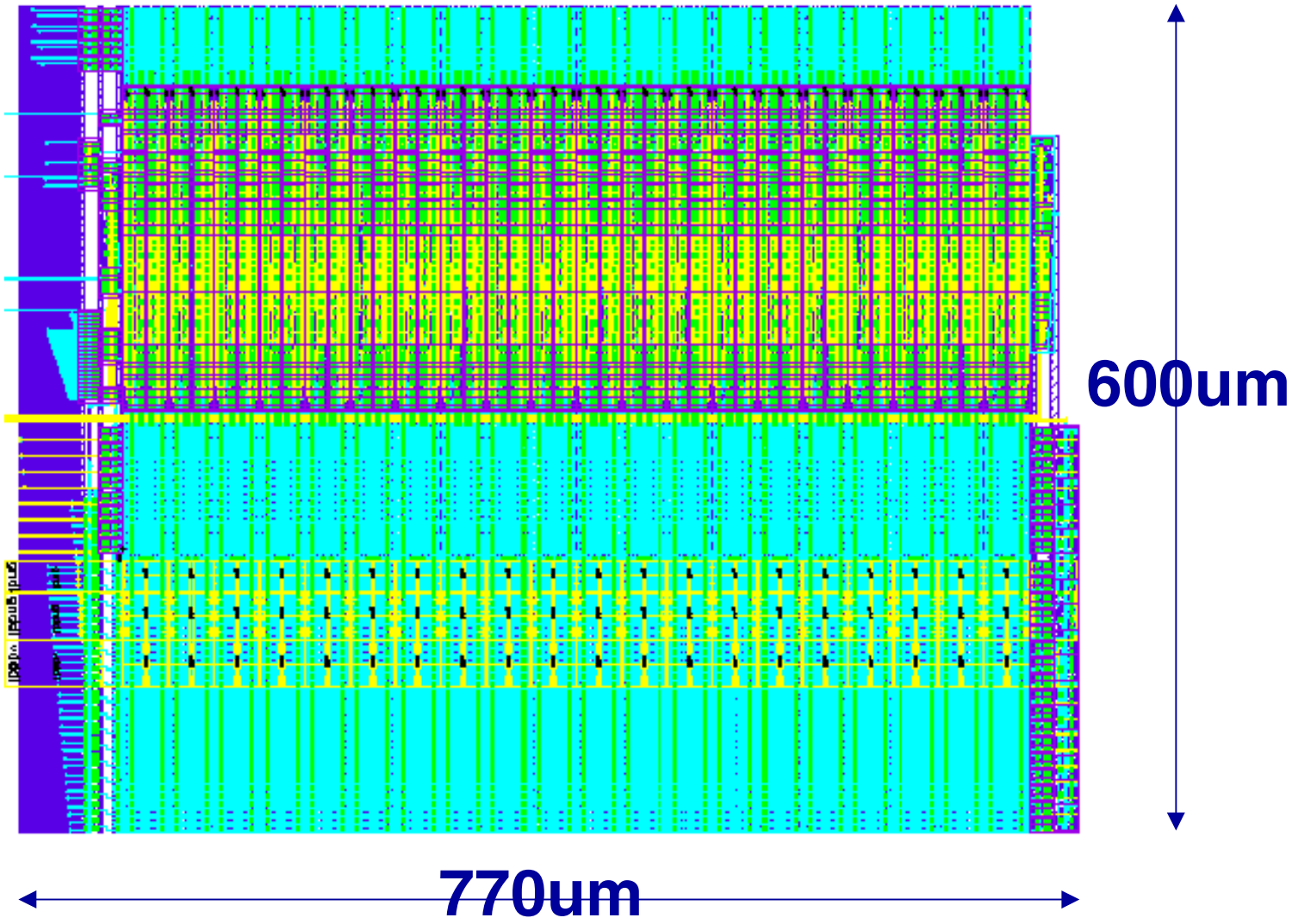




Horizontal Scan

```
module gmEocHScan2 (ADDROUT, PRIORITYOUT, TOTOUT, OVERFLOWOUT, ROCKCOL, COLUMNIDB,
            ENABLE, HADDR, HPRIORITYIN, HTOT, OVERFLOWIN,ROCK, VADDRB, priorityR, priorityW, VTOTB);
 output [12:0] ADDROUT;
output  [7:0] TOTOUT;
output       PRIORITYOUT, OVERFLOWOUT, ROCKCOL;

input [12:0] HADDR;
input  [3:0] COLUMNIDB;
input  [8:0] VADDRB;
input  [7:0] HTOT, VTOTB;
input       ENABLE, HPRIORITYIN, OVERFLOWIN, ROCK;
input       priorityR, priorityW;

wire SELVERTICAL;

assign OVERFLOWOUT =  OVERFLOWIN | (priorityW & ENABLE);  // ERROR ??
assign PRIORITYOUT =  (priorityR | ~ENABLE) & HPRIORITYIN;
assign SELVERTICAL = ~(priorityR | ~ENABLE) & HPRIORITYIN;
assign ROCKCOL     =  ROCK & SELVERTICAL;

assign TOTOUT  = SELVERTICAL ? ~VTOTB : HTOT;
assign ADDROUT = SELVERTICAL ? ~{COLUMNIDB,VADDRB} : HADDR;
endmodule
```

End Of Column Buffer



End of Column Buffer

Finished

- Schematic/layout
- Verilog simulations

Things to do

- Simulations (Analog, Digital with delay)
- Power estimate
- Fix error (?) in “OVERFLOWOUT”