

Digital Verification Using Verilog

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- High Level Verilog simulation
- Self-checking
- Load dependent delays
- Backannotation
- Include MCC in the Verilog simulation

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High Level Verilog simulation

- Started with writing simple tasks, e.g. write_cmd, write_configreg, etc.
- Created some tasks for simple checks, deserializer, compare_cmd, etc.

Final goal: Make the testbench selfchecking

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Verilog models with load dependent delays

Standard Cell Library: delay models exists

Custom cells: write/adapt Verilog models to include load dependent delays, incl. Timing checks.

Not clear yet how to do this using the Cadence TLF, SDF, ... format.

Back Annotation

Place & Route Part

Silicon Ensemble provides an SDF file with load dependent delays after routing.

Custom layout

For the “old” Cadence delay format skill routines were available to extract parasitics and backannotate the parasitics into the Verilog simulation (Robert Szczygie).

Not clear if and how this can be used with TLF/SDF

Summary

- The functional Verilog simulation seems to be fairly straightforward
- Self-checking, do-able
- Back annotation/Load dependent delays:
Time to get out the manual