

IBM/TSMC Common Design Rules

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RAL/CERN IBM Design Kit

- Schematics - Cadence Analog Artist
- Analog Simulation - Hspice
- Custom Layout - Cadence Virtuoso
- Place and Route - Silicon Ensemble
Standard Cell Library
- Synthesis - Synopsys
- Digital Simulation - Verilog
- Static Timing Analysis - Pearl
- DRC - Diva, Dracula, Hercules@CERN
- Extract - Diva
- LVS - Diva

IBM/TSMC Design Kit

Based on IBM Design Kit

IBM startup script with new IBM/TSMC Technology library
using IBM layers

Conversion to TSMC using StreamIn/StreamOut

Changes/Additions :

- Custom layout : New set of “design rule correct”
symbolic contacts and transistor pcells
- Standard Cells : Separate “power gnd” and “substrate gnd”
- Place and Route : Added Double-Cut contacts/vias and
stacked contacts/vias

IBM/TSMC Design Kit

Changes/Additions :

- DIVA DRC :

divaDRC_IBM.rul - Original IBM DRC rules files, with
0.01 offGrid drc check instead of 0.02

divaDRC_TSMC.rul - CMC/TSMC DRC rules file with
TSMC layers renamed to IBM layers

divaDensity.rul - Pattern density rules check

Layout has to pass all three DRC rule checks !

IBM/TSMC Design Kit

Changes/Additions :

- Mentor Calibre DRC :

DRC rules files available for IBM and TSMC

Cadence interface

Grouping of errors

Fast

Conversion IBM to TSMC

Procedure:

- StreamOut the IBM layout using the default IBM Stream layernumbers
- StreamIn the IBM layout into a TSMC library using the IBM layernumbers with corresponding TSMC layernames
- Resize contacts from 0.28x0.28 to 0.3x0.3 (skill procedure)
- Generate nplus layer using Diva DRC
- Run TSMC DRC/Extract/LVS
- StreamOut using TSMC Stream layernumbers
- Submit

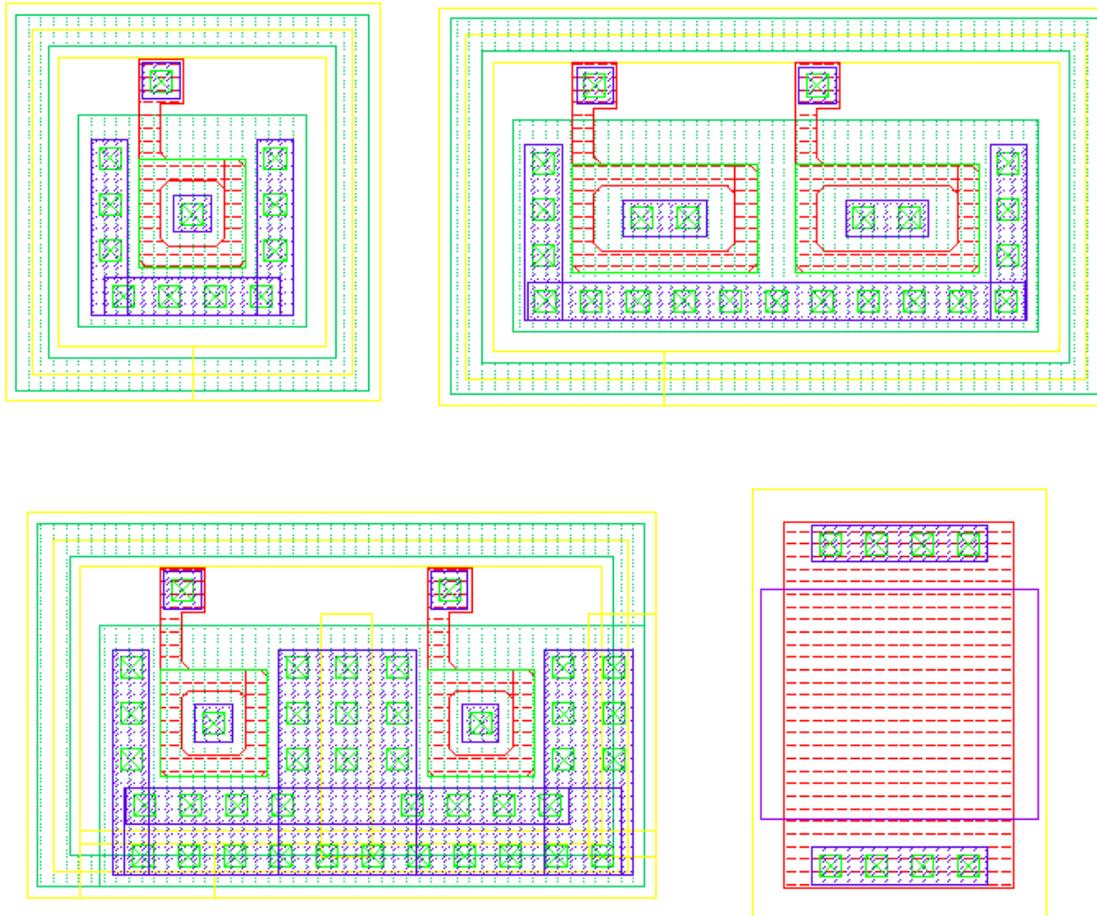
Conversion IBM to TSMC

Restrictions:

- Layers allowed RX, NW, PC, BP, OP, CA, M1, V1, M2, V2, M3, V3, M4, V4, (MZ, LM, MT)
- No MIMCAPs
- Use only low resistance P+Poly resistor

PCELLS

Make life easy, use pcells, design rule correct for IBM/TSMC



CONCLUSION

- Minor changes to RAL/CERN IBM Design kit to accommodate common IBM/TSMC 0u25 design
- Using Pcells for “design rule” correct layout