

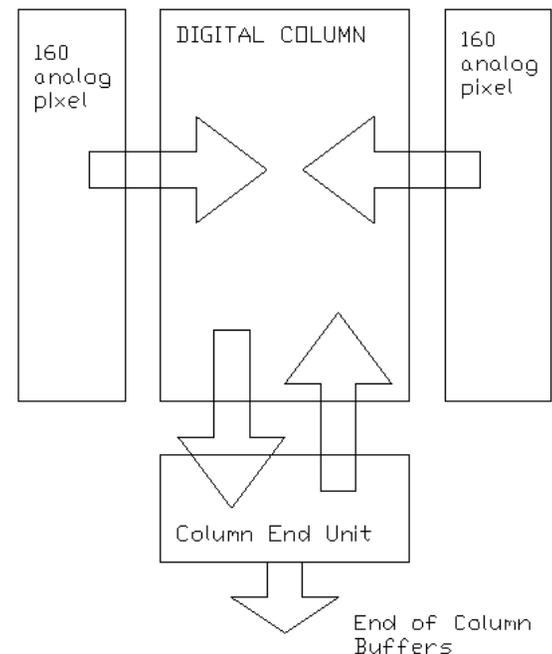
Atlas Pixel FE 0.25 Readout Chip

Digital Column Readout Logic

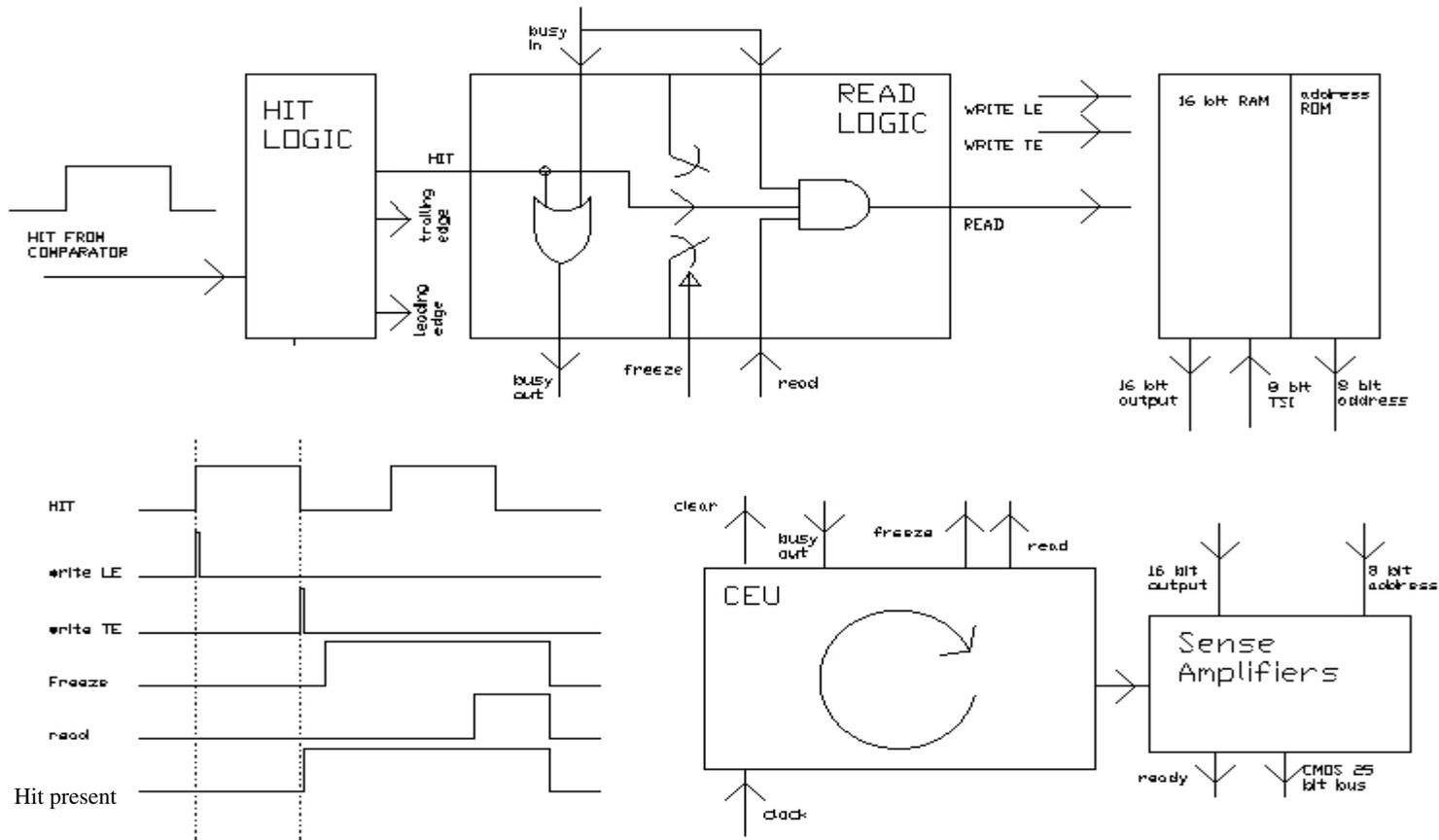
Emanuele Mandelli
Lawrence Berkeley National Laboratory

Digital Column Readout

- The digital column readout logic accepts hits from the comparator outputs of two columns of analog pixels (160x2), associate them with a global clock (TSI) and regulates the flow of data to the end-of-column buffers. Each hit is composed by 8 bits LE, 8 bits TE and 9 bits ADDR.



Digital Pixel Functional Diagram



Changes

- The pixel hit logic is based on a static design;
- Double hit corruption is possible but unlikely; only pulses that are already high when the pixel is being readout will have wrong LE;
- wLE and wTE pulses width is determined by a delay chain implemented with 10 inverters;
- No Clear signal is necessary since the RAM cells are static and write pulses are used;

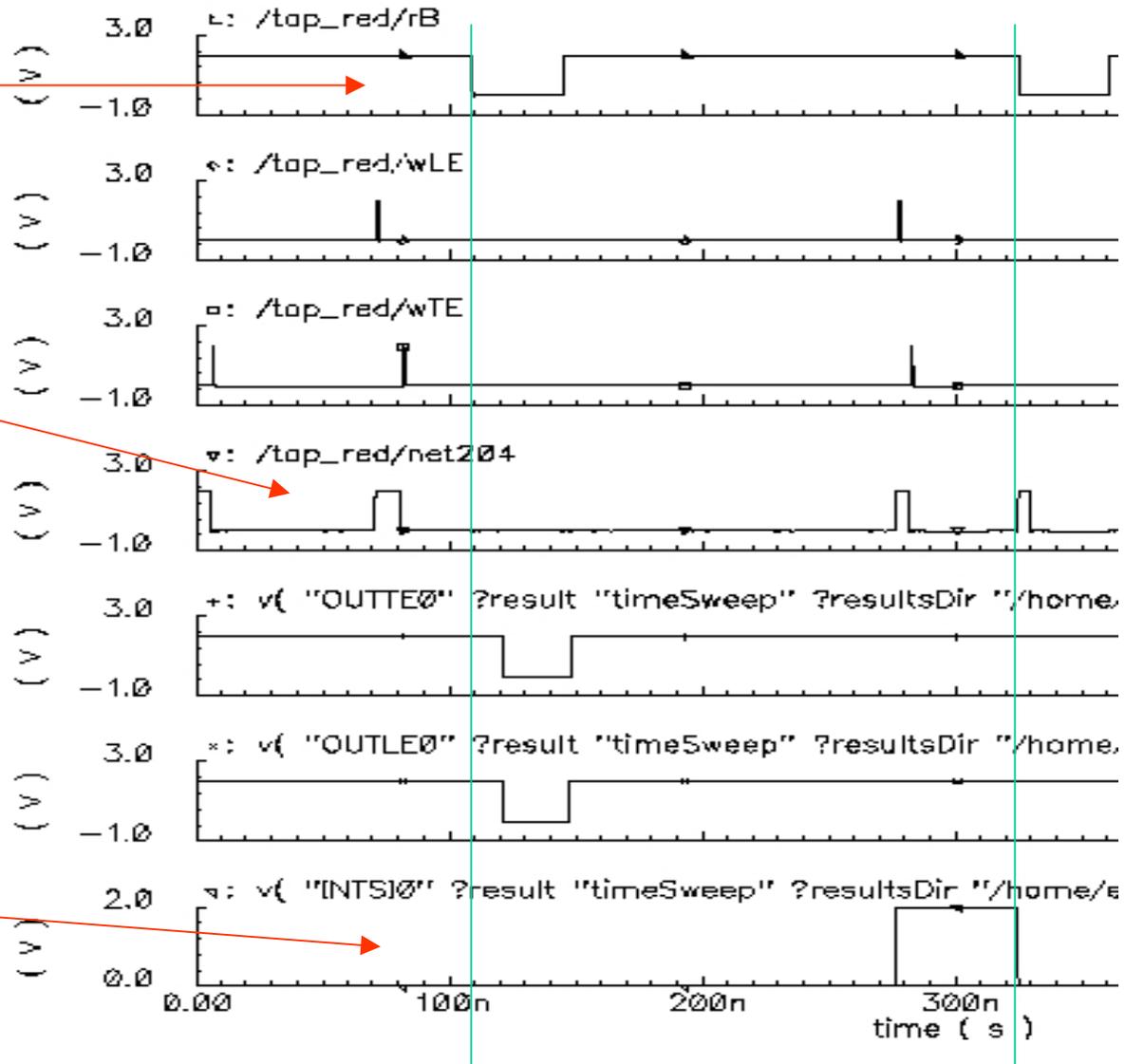
Pixel Logic Sim

Transient Response

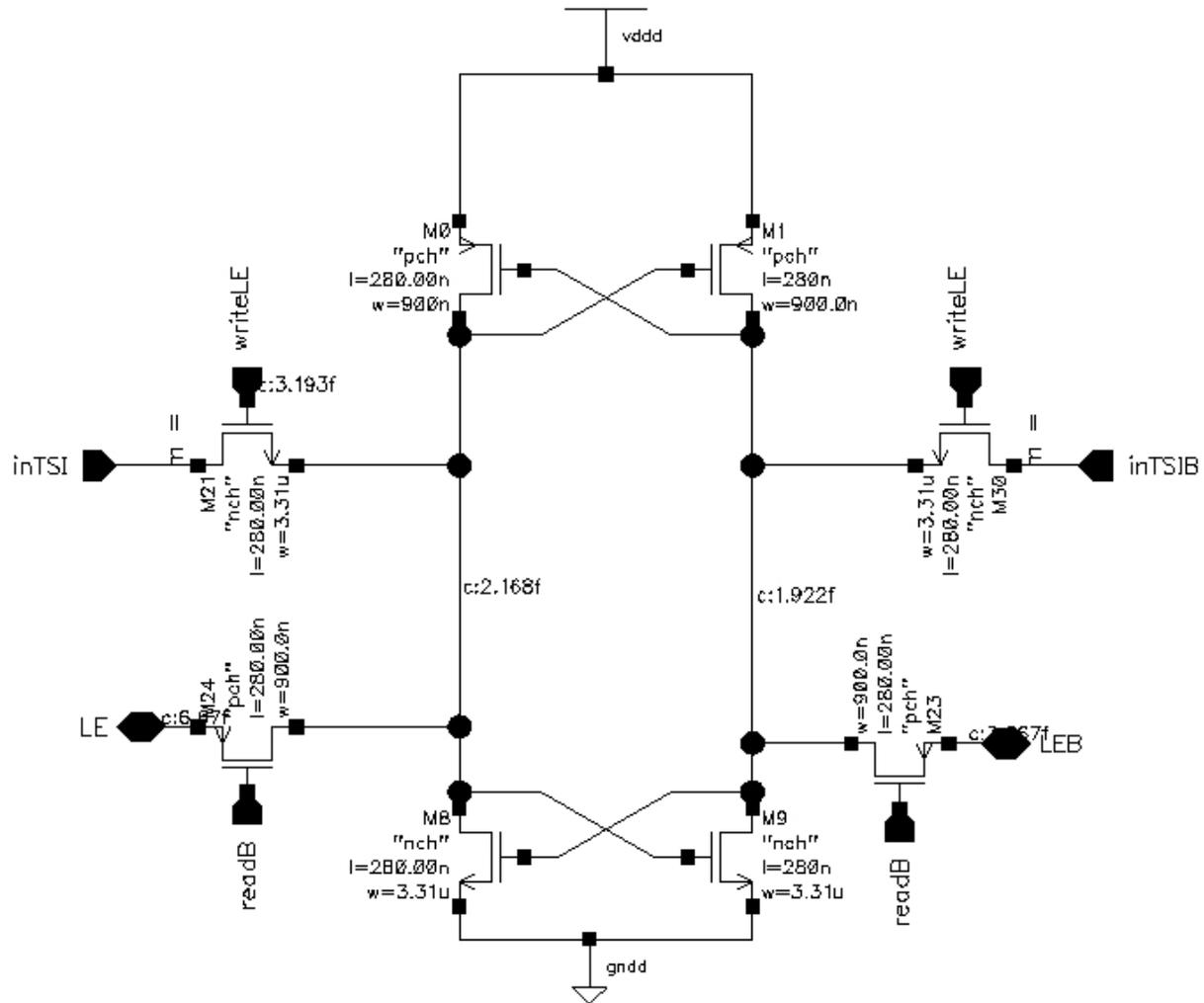
ReadpixelB

Discriminator Output

Global TSI Clock



Ram Cell Schematic



Changes

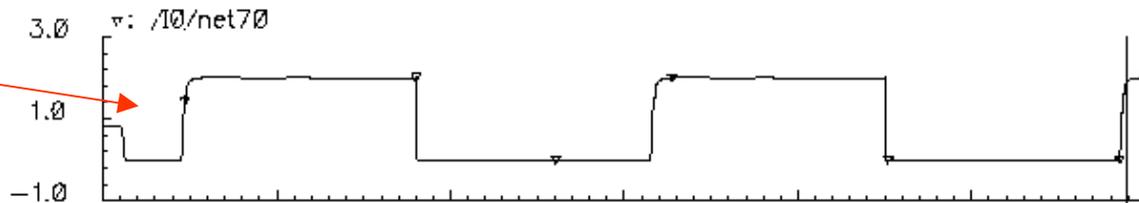
- RAM cell is static;
- RAM cell is differential;
- RAM cell write port is open only for a short time, when necessary, not to load the TSI bus;
- Layout is '*load compensated*' in order to reduce cross talk from TSI, LE, TE and ADD lines to the sensor;

RAM Cell Sim
slow models - 2V

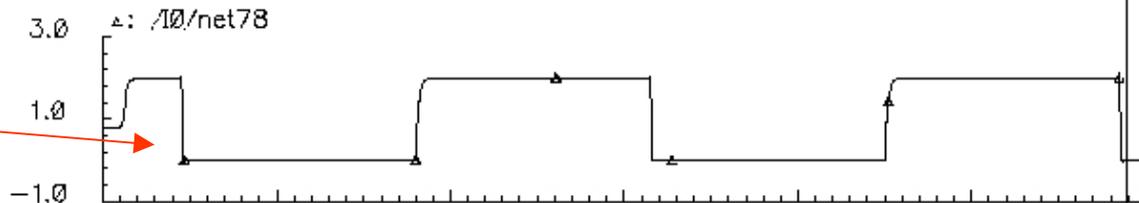
FEL_TEST SIMemRam_new_cell schematic : May 23 12:05:36 2001

Transient Response

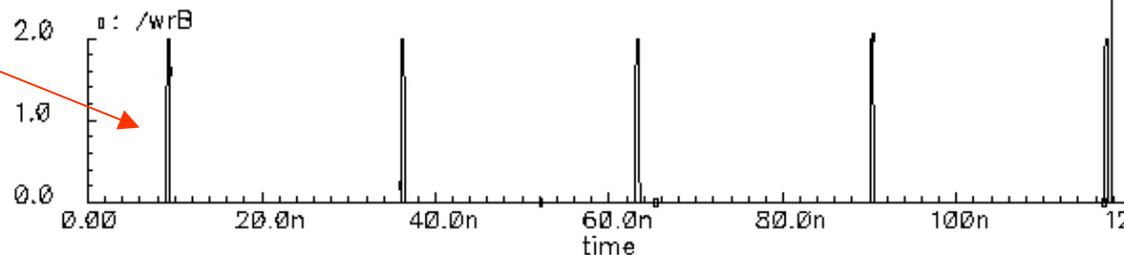
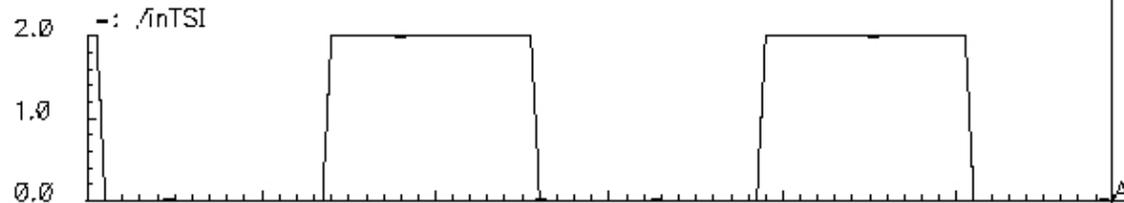
memnodeB



memnode

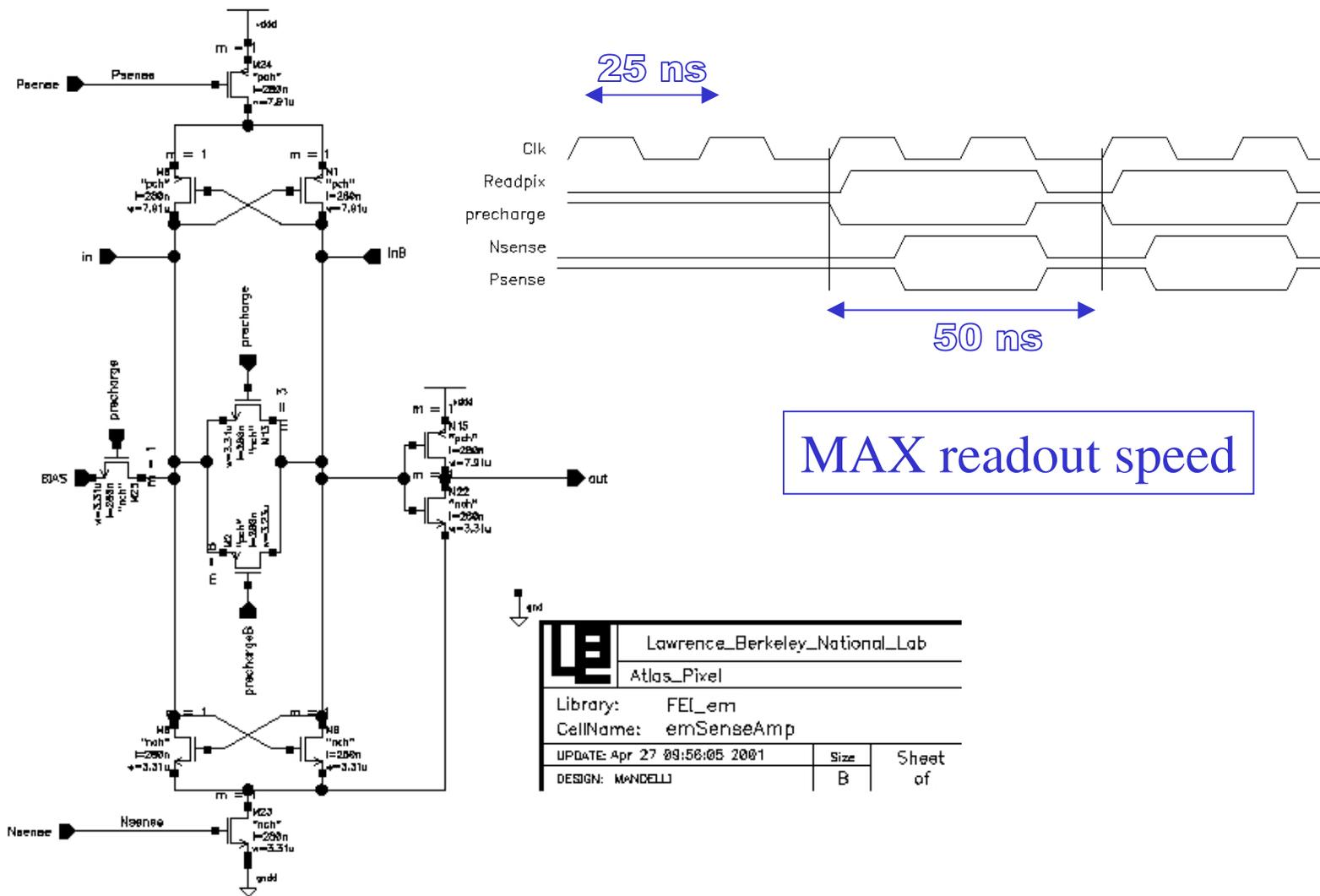


RAM write
pulse



A: (117.876n 0)

Sense Amp Schematic



Changes

- CMOS pre-charged differential design;
- Very fast and low DC power, but timing is critical (controlled by the CEU);
- A pre-charge voltage generator capable of driving the big TSI capacitive load is needed and it consumes DC power. (see later);

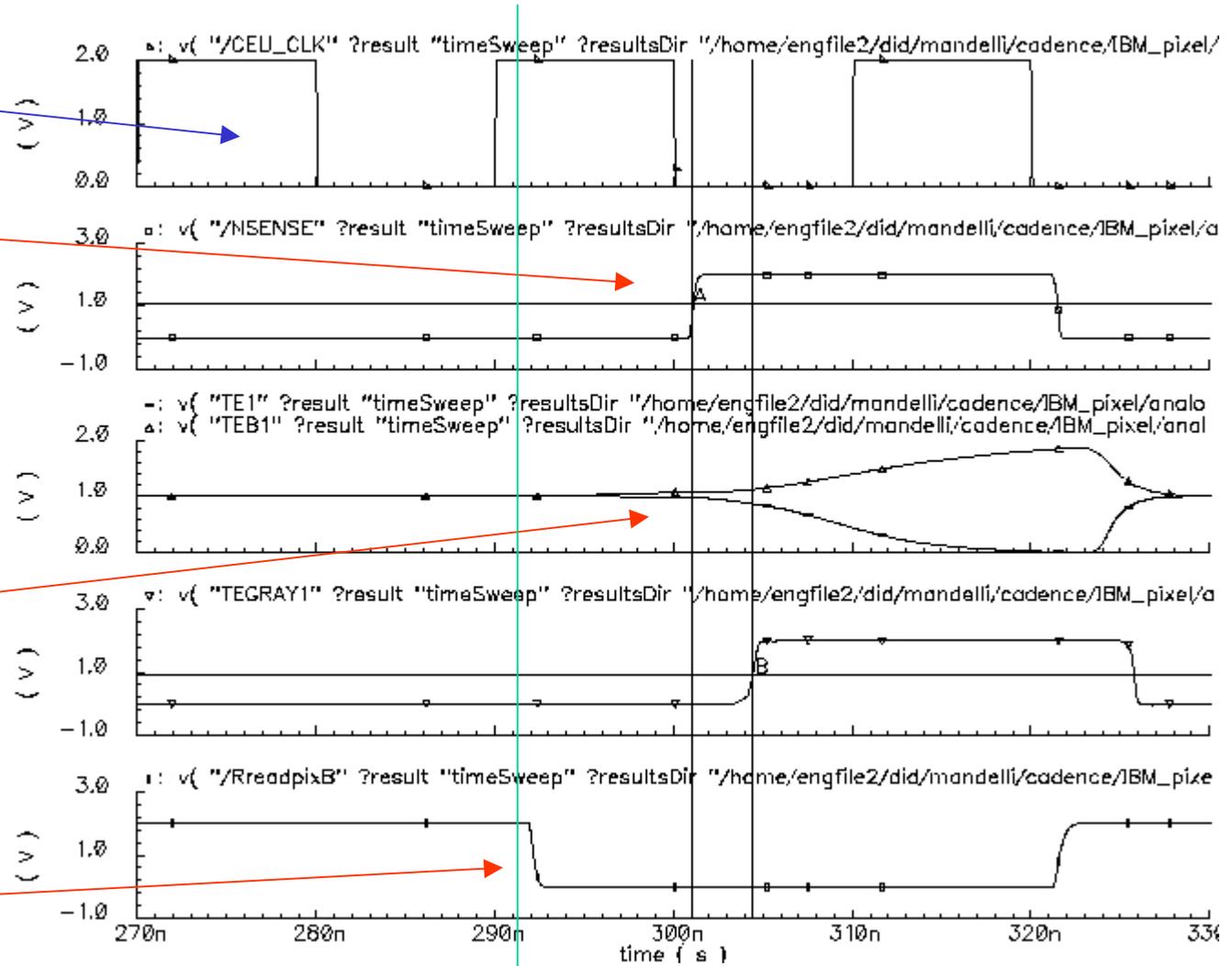
Sense Amplifier Simulations WC

40 MHz clk @ max readout speed

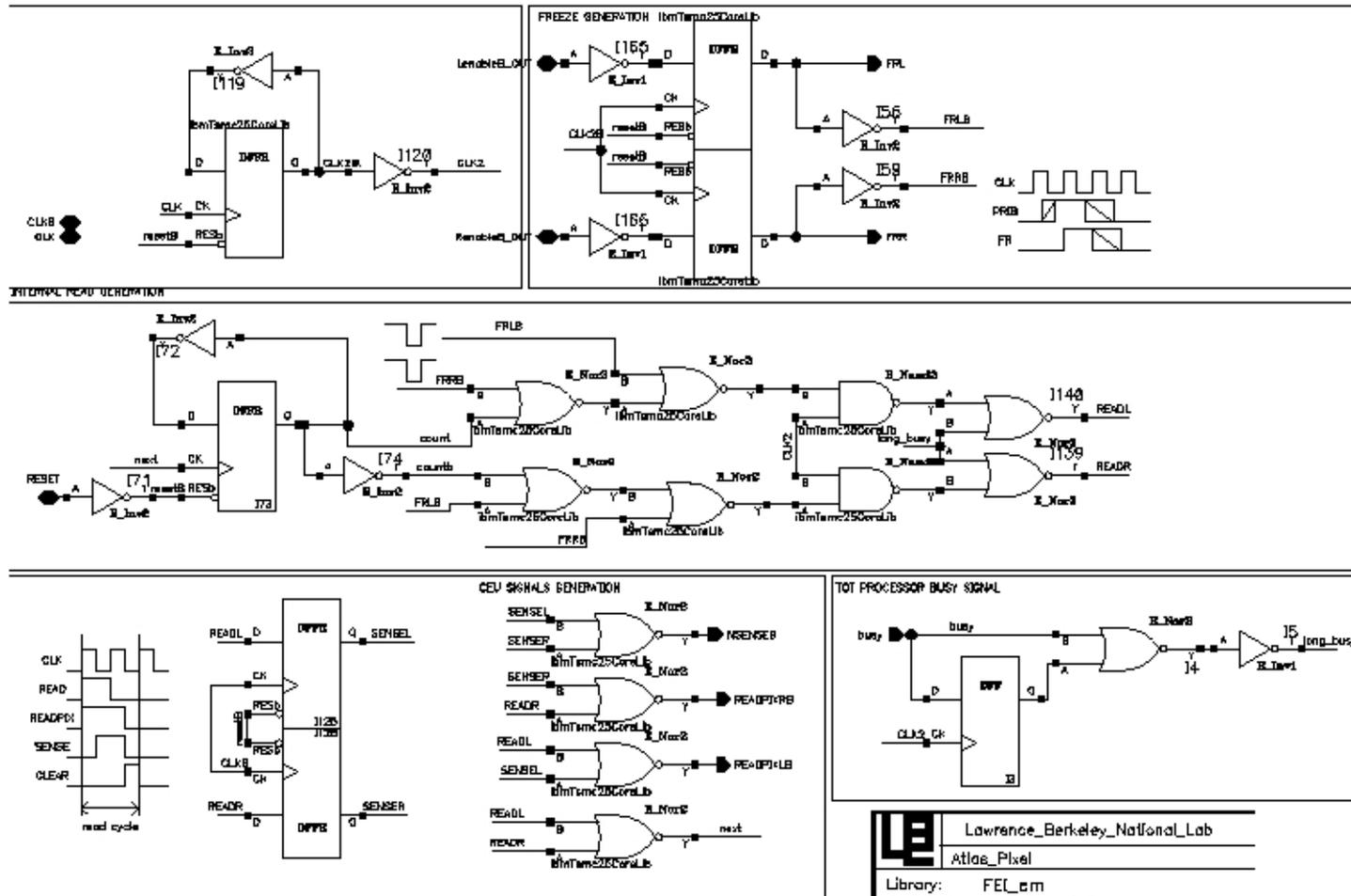
P_{sense} and N_{sense} are delayed by 1/2 clock cycle

The RAM cell moves the bus during the first half clock cycle

ReadB and prechargeB have the same phase



CEU Schematic Diagram

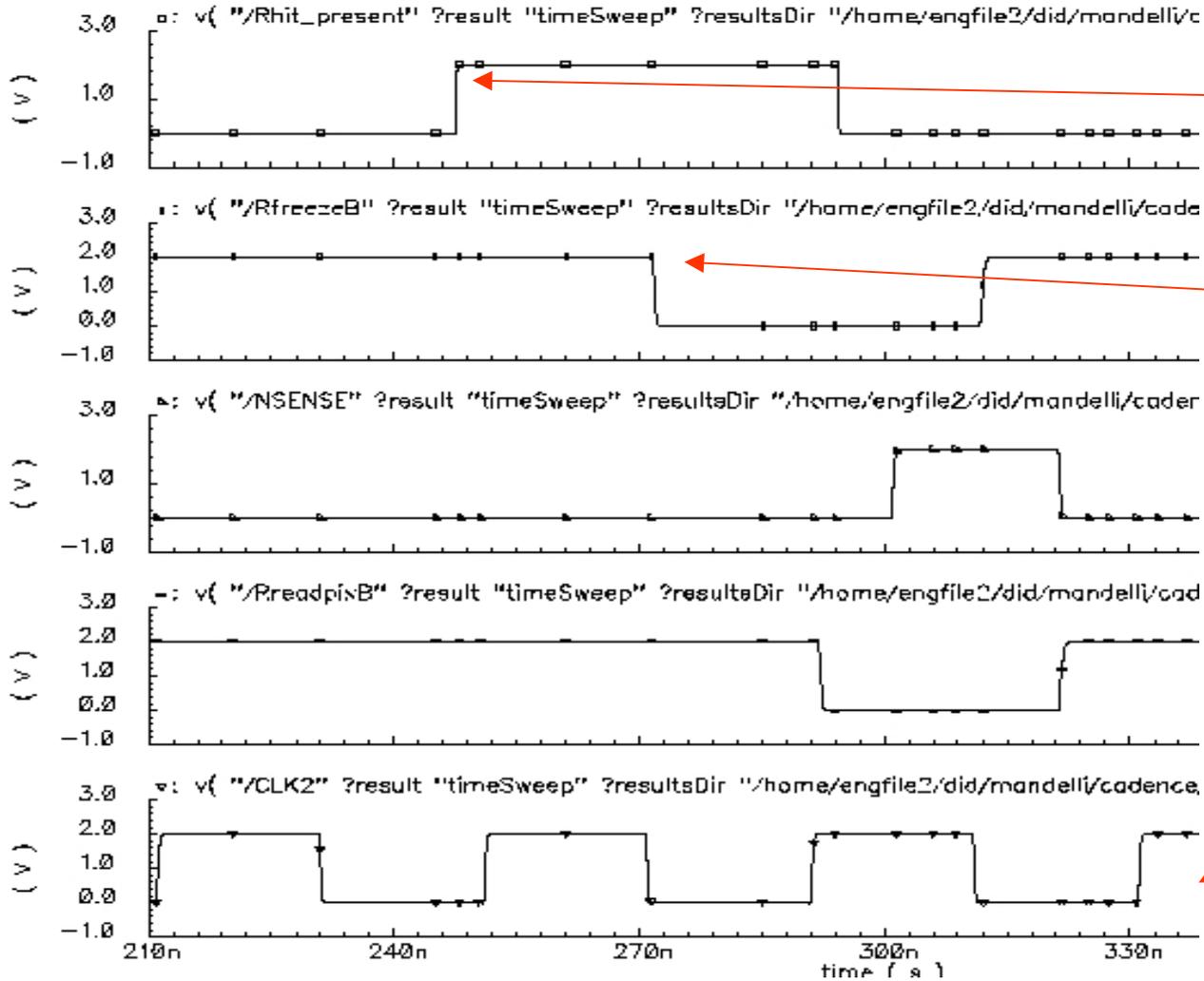


	Lawrence_Berkeley_National_Lab
	Atlas_Pixel
Library:	FEL_em
CellName:	amCeULogicPlus
UPDATE:	May 22 11:38:09 2001
DESIGN:	N=HOBLL
Size	Sheet
6	of

Changes

- The CEU works with one single phase clock;
- The readout speed is determined by the clock frequency;
- If no clock is present the CEU is off and does not consumes any power;
- The '*Freeze*' signal is synchronous;
- '*Clear*' signal is no longer needed by the pixel;
- A '*busy*' signal prevents the CEU from reading out data;
- The CEU synchronously generates the '*precharge-read-sense*' sequence needed by the sense amplifier;
- The CEU uses standard cells library only.

CEU Logic Sim



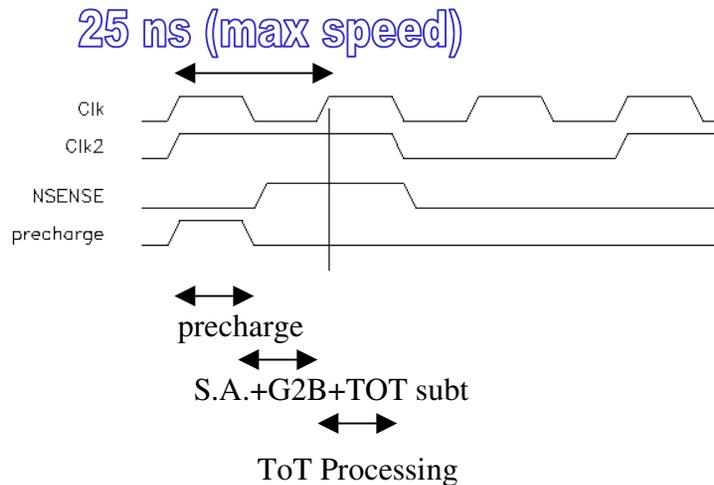
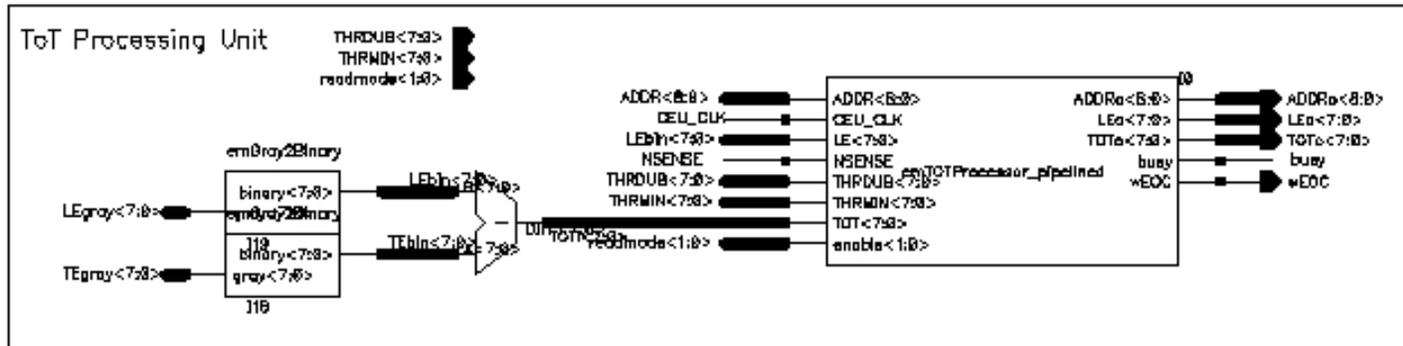
When this signal goes high, hits are present in the column

The column is frozen sync. With the clk

ReadPix is also used to precharge the Sense Amplifiers

This clock is generated in the CEU dividing the readout clock by 2

Tot Processor Functional Diagram



	Lawrence_Berkeley_National_Lab	
	Atlas_Pixel	
Library:	FEI_em	
CellName:	emColumnArbitrationUnit	
UPDATE: May 22 18:11:09 2001	Size	Sheet
DESIGN: MANDELLI	B	of

Gray 2 Bin Conversion

- LE and TE have to be converted from Gray to binary to be subtracted;
- the total time budget at maximum readout speed is 12.5ns, in which S.A., Gray2Bin and ToT subtraction have to provide valid data;
- The worst possible transition is 00000000 -> 10000000;

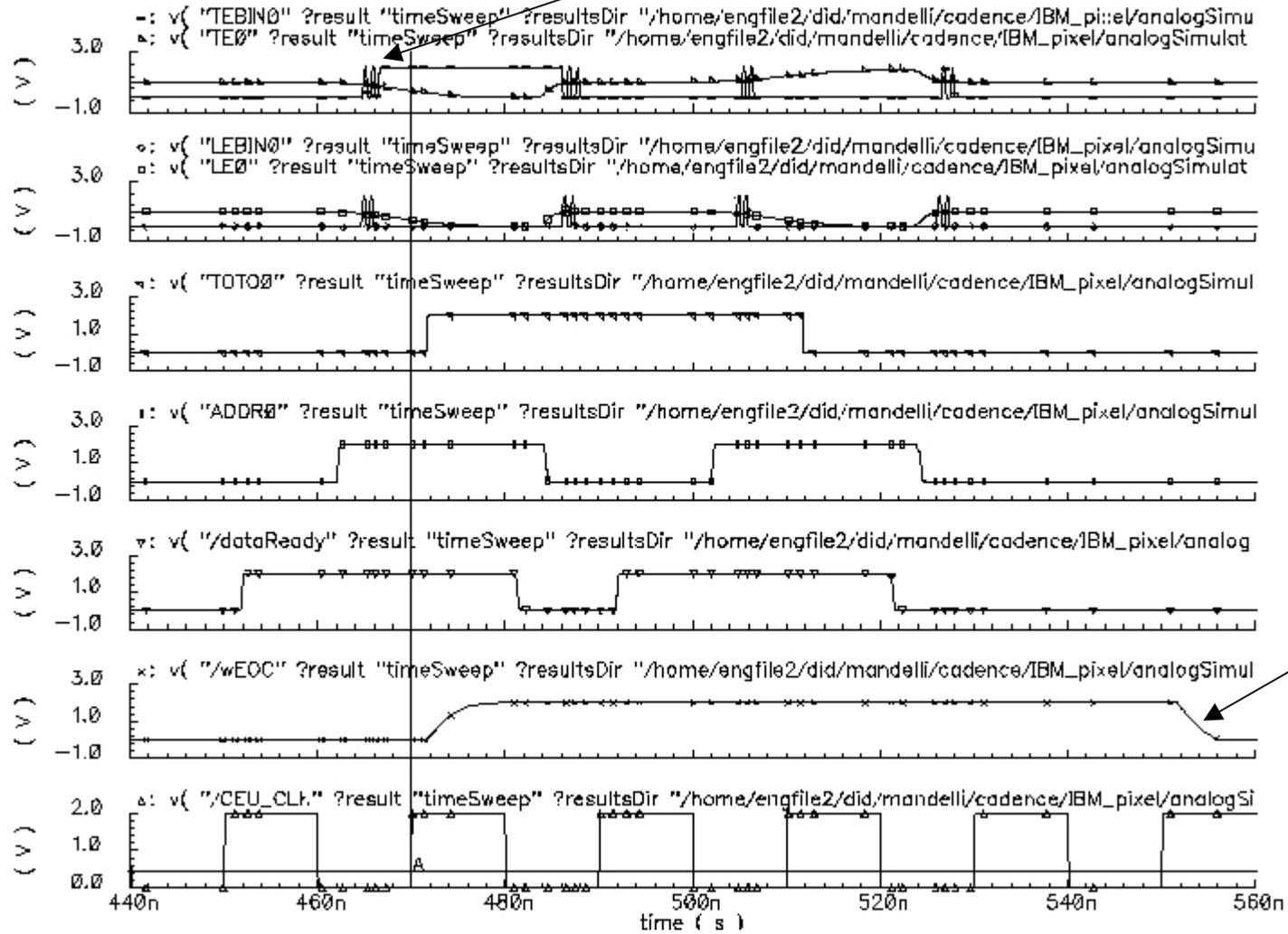
@2V	Gray2Bin	ToT Calc	SenseAmp Depends on C	TOTAL
Typ	2.5ns	1.4ns	(1.6ns)	5.5ns
Worst	4.3ns	2.7ns	(3.3ns)	11.3ns

ToT Processor

- ToT is calculated subtracting LEbin from TEbin at the column level;
- A ToT processing block latches the LE, ToT and ADDR values to be elaborated @CEU clock speed;
- Hits with small ToT can be discarded and/or duplicated;
- Four modes of operation:
 - Mode 00: All hits are written in the EOC buffers;
 - Mode 01: A hit with ToT below THRMIN is discarded;
 - Mode 10: A hit with ToT below THRDUB is written in two EOC buffers with leading edge equal to LE and to LE-1 in order to assign it to two subsequent bunch crossings;
 - Mode 11: Both thresholds are active (Filtering and Doubling);
- During hit doubling, the CEU is stopped and prevents new hits to be readout.

ToT Processor Sim

Conversion to binary takes a few ns

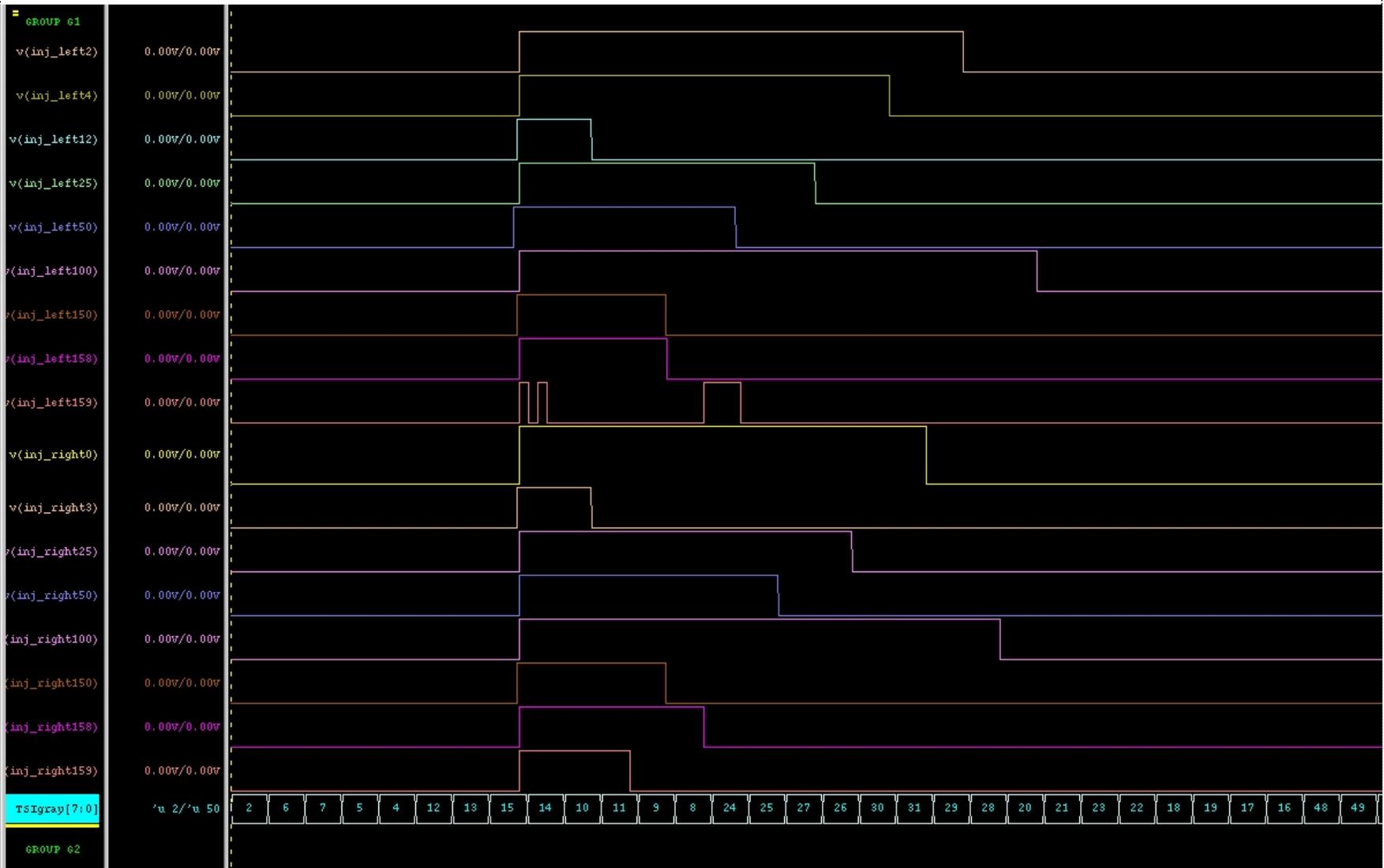


wEOC will no longer be loaded by the EOC buffers and will be much faster

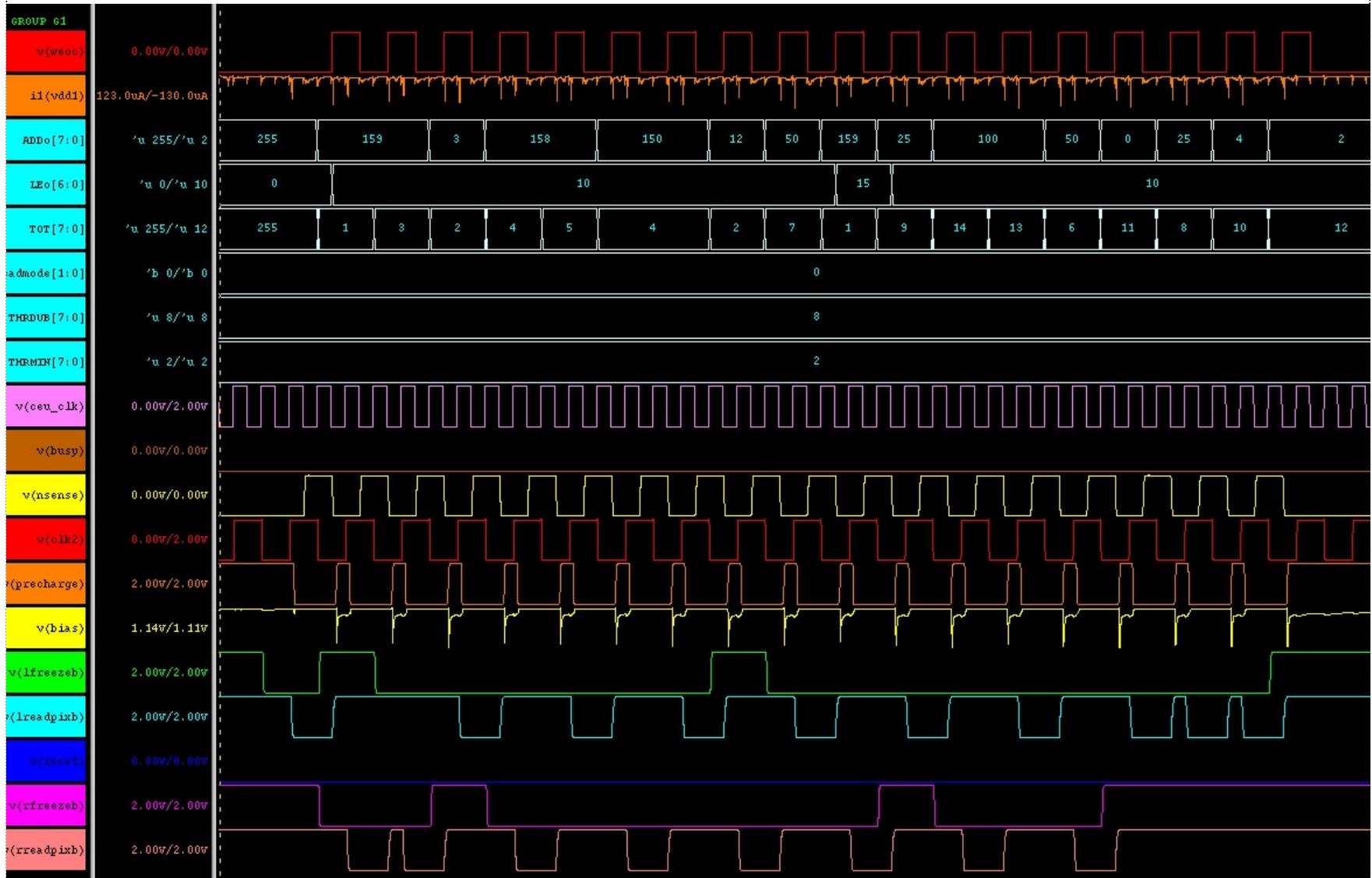
ToT Processor Sim 2



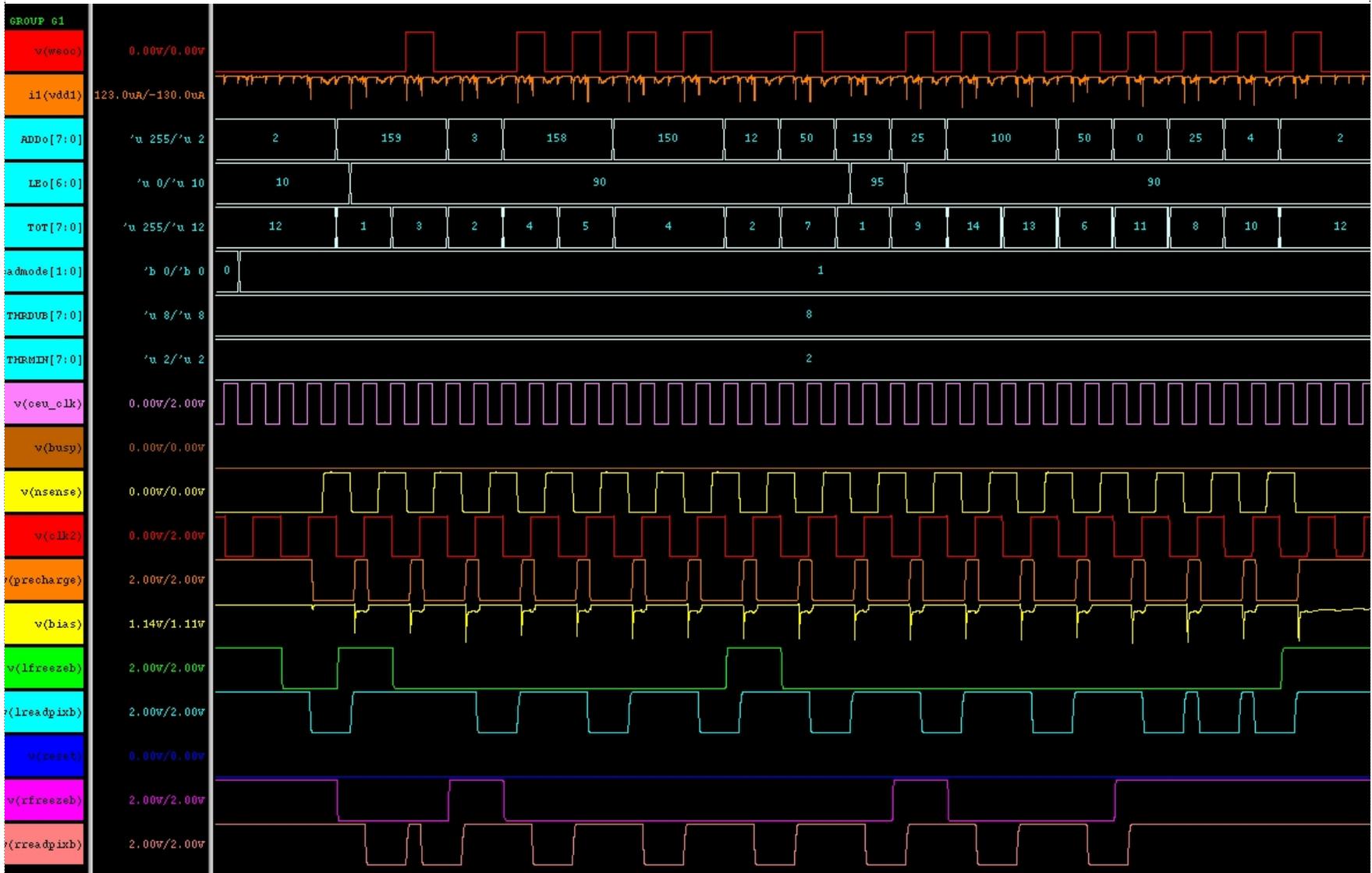
ToT Processor Inputs



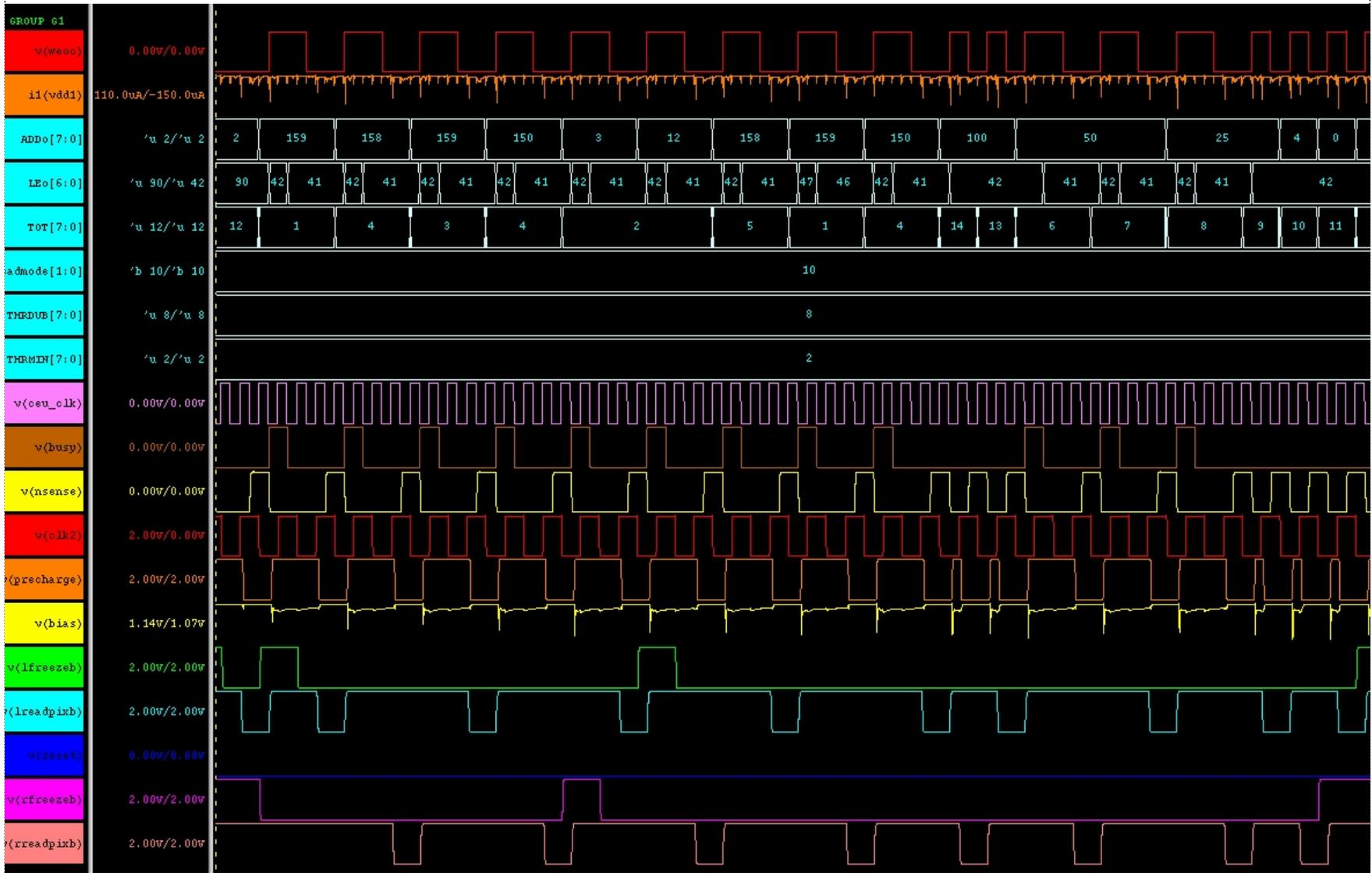
ToT Processor Sim3



ToT Processor Sim4



ToT Processor Sim5



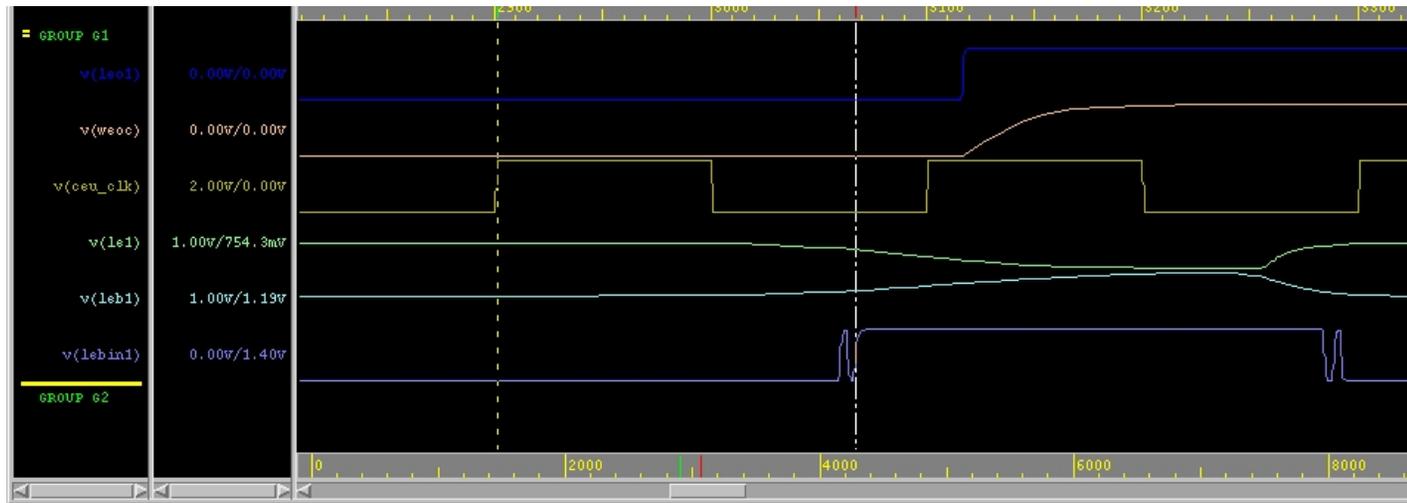
Simulation Results

- All simulations are done with a 50 MHz clk;
- BC, TC, WC has been simulated with verilog, eldo and PowerMill;
- Power supply is 2V;
- Power consumption: 1.1 mA per Column Pair idle;
- Consumption: 3.75 mA per Column Pair with the shown injection sequence averaged on 6us;
- Hot spots are TSI and TSIB lines 0;

Simulators Comparison

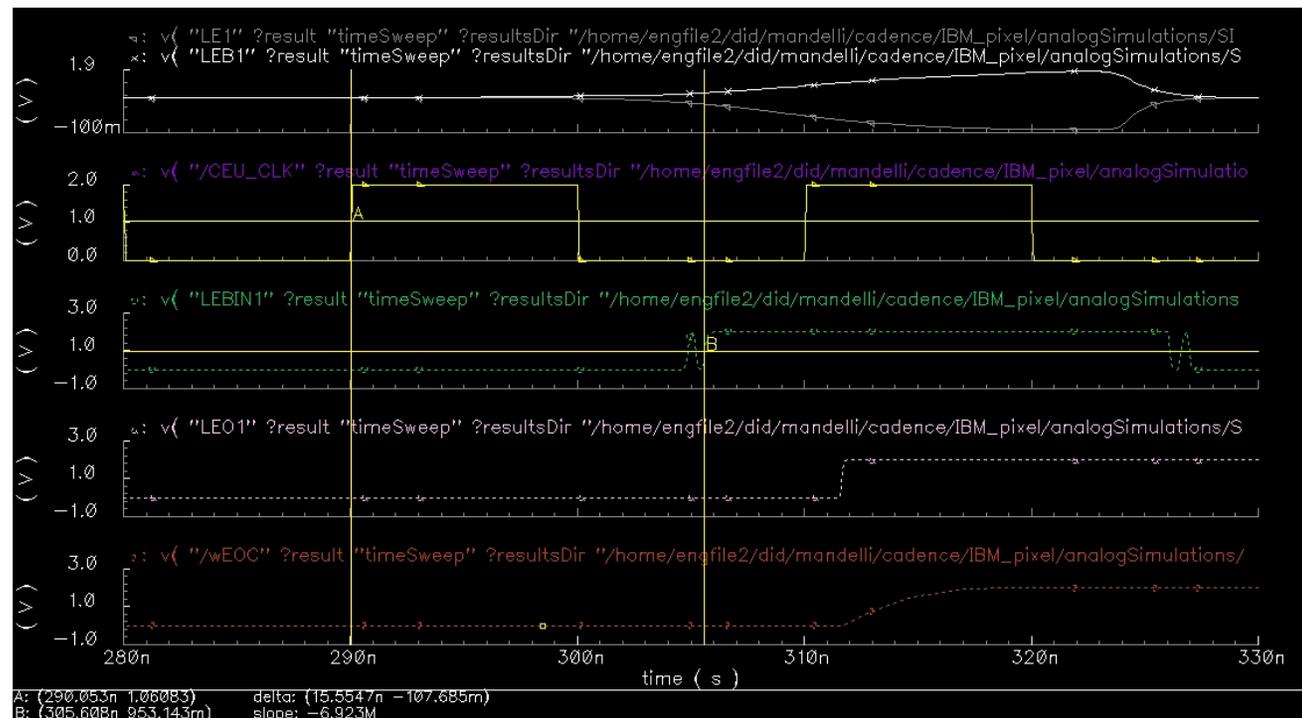
<i>Simulator</i>	<i>Error</i> <i>(delays, tr, tf)</i>	<i>Time</i> <i>15.000 dev</i> <i>1us .tran</i>	<i>Time</i> <i>150.000 dev</i> <i>6us .tran</i>	<i>Converging</i> <i>Devices</i>
Hspice	-		N.A.	1.000
Eldo	-	2h:30m	N.A.	15.000
PowerMill <i>(BSIM3)</i>	5-10 %	5m	18h:00m	>150.000 (?)
Verilog	< 10%	< 1m	~ 2m	>>150.000

Sim comp



Critical time example:

Verilog 16.1 ns
 PowerMill 16.6 ns
 Eldo 15.5 ns
 Diff < 10%



PowerMill Sim Out 1

```

xterm
-----
PowerMill Version 5.4
SN: P20000111(5.4)-SunOS_5
Copyright (c) 2000 Synopsys Inc., All Rights Reserved.
-----

Built by integ in " sun50111r54 " on Wed Jan 12 16:38:36 PST 2000
Fri Jun 1 16:04:51 2001

*****
RUN TIME POWER BUDGET VIOLATIONS
*****

*****
POWER BUDGET VIOLATION SUMMARY
*****

*****
BLOCK HIERARCHICAL POWER ANALYSIS
*****

BLOCK Col_power: AVERAGE SUPPLY CURRENT.

LEVEL          CURRENT          PERCENT OF          PERCENT OF          CHILD BLOCK NAME
              (uA)              PARENT              TOP
-----
*----- 0          -1059.2          100.00          100.00          Col_power
--*----- 1          -1023.5          96.63           96.63          kemcolarbunit.Col_power
---*----- 2          -485.19          47.41           45.81          kemcolarbunit.kem_ceu_top.Col_power
----*----- 3          -97.804          20.16           9.23           kemcolarbunit.kem_ceu_top.xi25_0.Col_power
-----*----- 3          -91.15           18.79           8.61           kemcolarbunit.kem_ceu_top.xbuf_0.Col_power
-----*----- 3          -78.809          16.24           7.44           kemcolarbunit.kem_ceu_top.xceu_logic.Col_power
-----*----- 3          -51.689          10.65           4.88           kemcolarbunit.kem_ceu_top.xi25_1.Col_power
-----*----- 3          -45.734          9.43            4.32           kemcolarbunit.kem_ceu_top.xbuf_1.Col_power
-----*----- 3          -22.861          4.71            2.16           kemcolarbunit.kem_ceu_top.xbuf_2.Col_power
-----*----- 3          -22.22           4.58            2.10           kemcolarbunit.kem_ceu_top.xi25_2.Col_power
-----*----- 3          -14.95           3.08            1.41           kemcolarbunit.kem_ceu_top.xi25_3.Col_power
-----*----- 3          -8.0017          1.65            0.76           kemcolarbunit.kem_ceu_top.xbuf_3.Col_power
-----*----- 3          -7.9547          1.64            0.75           kemcolarbunit.kem_ceu_top.xi1.Col_power
-----*----- 3          -7.8474          1.62            0.74           kemcolarbunit.kem_ceu_top.xi2.Col_power
:

```

PowerMill Sim Out 2

```

xterm
drwxr-xr-x  2 mandelli pixel      4096 May 29 14:25 .epicrun15725/
-rw-r--r--  1 mandelli pixel       608 May 29 14:29 emColExt2x160_noinj_unc
-rw-r--r--  1 mandelli pixel       273 May 29 14:29 emColExt2x160_noinj_ignore
-rw-r--r--  1 mandelli pixel     11219 May 29 14:29 emColExt2x160_noinj_fcapp
-rw-r--r--  1 mandelli pixel    245758 May 29 14:40 emColExt2x160_noinj_log
-rw-r--r--  1 mandelli pixel       578 May 29 14:40 emColExt2x160_noinj_err
-rw-r--r--  1 mandelli pixel   13981960 May 29 14:40 emColExt2x160_noinj_out
-rw-r--r--  1 mandelli pixel   1297524 May 29 14:40 emColExt2x160_noinj_cnt
-rw-r--r--  1 mandelli pixel     1200 May 29 14:40 emColExt2x160_noinj_sum
-rw-r--r--  1 mandelli pixel     2987 May 29 14:40 emColExt2x160_noinj_stat
-rw-r--r--  1 mandelli pixel    65816 May 29 14:40 emColExt2x160_noinj_power
-rw-r--r--  1 mandelli pixel     1324 May 29 14:40 emColExt2x160_noinj_nodealias
-rw-r--r--  1 mandelli pixel       541 May 29 14:40 emColExt2x160_noinj_hist
-rw-r--r--  1 mandelli pixel    739706 May 29 14:51 emColExt2x160_noinj_out.fsdb
drwxr-xr-x  5 mandelli pixel     8192 May 29 14:51 ./
engcad4:~/TimeMill/emColumnPlus/extracted_2x160 > less emColExt2x160_noinj.sum
-----
|                                     |
|               PowerMill Version 5.4 |
|               SN: P20000111(5.4)-SunOS 5 |
|   Copyright (c) 2000 Synopsys Inc., All Rights Reserved. |
|                                     |
|-----|
; Built by integ in " sun5011r54 " on Wed Jan 12 16:38:36 PST 2000
; Tue May 29 14:40:35 2001
;
;
; *****
; *** Hot Spot Statistics ***
; *****
;
Node Name          Cap(fF)      Toggle      Icin(uA)      Icout(uA)
-----
tsi_column0       3554.19      25          96.07         85.97
tsib_column0     3330.05      25          85.41         87.37
tsi_column1      3447.62      13          52.35         43.62
;
Total non-input nodes      :    31463
Total node toggles         :    15391
Total charging current      :    1274.53 uA
Total discharging current   :    1325.54 uA
emColExt2x160_noinj.sum (END)

```

Gray Code

0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101
10	1111
11	1110
12	1010
13	1011
14	1001
15	1000

COMMENTS:

- metastability in CEU hit-present -> freeze
- metastability in output inv of sense-amps
- power in precharged sense-amp?
- disconnect output BUS from sense amp during NSENSE phase