8 Pixel Demonstrator Programme

8.1 Introduction

Pixel detectors are currently used in several particle physics experiments [SLD, WA97, DELPHI, NA57] in much less demanding environments than the one foreseen at LHC. It was therefore felt necessary to develop a prototype which is close enough to the ATLAS requirements to give us confidence that we can build the detector we propose.

The demonstrator programme is subdivided into three steps of increasing complexity. In each step, detectors are integrated with electronics to form modules of different sizes. In all cases the front-end electronics should be able to operate according to the specifications described in Chapter 5, with the exception illustrated later in this section. The demonstrator programme is made of the following steps:

1. a single chip integrated on a ~0.6 cm^2 sensor (single chip module)
2. a set of 16 front-end chips on a ~10 cm^2 sensor with a Module Controller Circuit (MCC) integrated outside the module (16-chip module)
3. as in (2.), but with the MCC integrated on the module (ATLAS module).

The read out chain is the same for the three prototypes. Data transmission uses copper lines, rather than optical fibres. Results from (1.) are presented in Section 8.3.3; results from (2.) are expected during the summer of 1998, and results from (3.) should be available for the decision on module design, planned for November 1998.

The most important differences between the demonstrator and the final design are:

- the front-end chips and MCC have been designed in rad-soft technology
- the depth of the end-of-column buffers is limited (i.e. sufficient for the outer layers, but not for the B-layer at high luminosity)
- the pixel size is 50 µm x 400 µm

Some circuitry for diagnostic purposes is implemented in the demonstrator chips which should not be needed in the final design. We believe that this extra space reserve will allow us to implement, in the rad-hard optimized design with the nominal size pixel cell, the end-of-column buffer depth required for B-layer operation at full luminosity.

8.2 Description of the Demonstrator

One of the major goals of the demonstrator programme is to incorporate approximately the right level of functionality in each of the main chips. This implies serial transmission of configuration commands from the MCC chip to the front-end chips, and serial transmission of the data from the front-end chips, via a star topology, to the MCC chip. All digital signals which must be active during data-taking operations are transmitted using low-voltage swing differential drivers and receivers, and the pinout of each chip is simplified as much as possible. A number of parameter adjustments for the analog front-end circuitry are implemented using 8-bit current mode DACs to allow adjustment from the MCC without the transmission of large numbers of

analog signals to the module. The die area of the front end chips is approximately that expected for the final chips. The pixel size is 50 x 400 μm, in order to leave adequate room for diagnostic and control circuitry, and not constrain the design too severely before the details are worked out. This leads to a chip with eighteen columns of 160 pixels each. The total die size is 7.4 x 11.0 mm, including 0.1 mm between the chip active boundary and the scribe line on all sides of the die. This allows almost 3mm of space for the next generation of complete peripheral logic designs to be carried forward. Furthermore, these chips have the overall geometry required for ATLAS module construction, in which the active area of the pixels extends to within 0.1mm of the die edge on three sides of the chip, with all additional circuitry and I/O pads required to reside along the fourth ("bottom") edge of the chip. These chips will have 48 I/O pads, spaced 150 μm apart, on the "bottom" edge of the die.

This prototyping effort has been pursued with the aim of providing two front-end chip designs in rad-hard technologies using two different vendors, according to the official ATLAS policy for radhard electronics development. The two different vendors to be used are discussed in more detail in Chapter-5. Before making submissions to a rad-hard foundry, the basic designs have been prototyped using a similar process from a rad-soft vendor (AMS BiCMOS for the corresponding DMILL process, and HP CMOS for the corresponding Honeywell process). The two front-end designs will differ in many internal details, but are functionally "pin-to-pin compatible", so that modules can be easily built with either front-end chip and comparatively tested. To help achieve this level of compatibility, a specification was developed (described in Chapter-5), which also constrains the MCC protocol description.

The MCC chip uses standard cell CMOS design, apart from the FIFOs and LVDS drivers which are custom-designed. It is currently in fabrication at AMS. The die contains ~4 10^5 transistors over an area of 6.5 x 11.0 mm^2. There are 83 I/O pins.

For diagnostics, the MCC can also operate in a transparent mode; i.e. acting as a direct connection to a selectable front-end. In order to facilitate debugging and to cope with the submission delay of the MCC (see Chapter 5), an MCC substitute chip has been built which operates only in transparent mode.

Sensors have also been fabricated by two vendors. Some sensors have been directly bump-bonded onto the front-end electronics to produce the prototypes on which we report in Section 8.3.3. Some sensors are undergoing irradiation tests up to 10^{15} n_{ep}/cm^2 prior to bump bonding to rad-soft front-end chips. Studies of irradiated sensors should allow us to discriminate between the various design options which have been implemented in the single chip devices. First results are expected in Summer 1998.

The read-out chain for all prototypes consists of three elements, which are briefly described below:

- In the control room, a DSP interface: a VME module which provides 32 data lines and 12 address lines and controls the lower level boards described below;
- A Pixel Low Level Card (PLLC), which provides the interface to DSP for serial command processing in the front-end and module control chips and which performs:

  data decoding for the returned serial data stream,

  hardware histogramming capabilities for fast scans of thresholds, timewalk and charge gain,

  strobe/trigger generation and slow control capabilities;

- A Pixel Control Card (PCC), which provides:

  I/V supply and monitoring under external control,

  12-bit DAC for front-end chip control,

  differential drivers/receivers for digital signals from the PLLC and for LVDS from the support card,

  clock regeneration and re-synchronization of fast signals with the 40 MHz clock, including strobe delay fine adjustment;

A schematic of the read-out chain is shown in Figure 8-1.

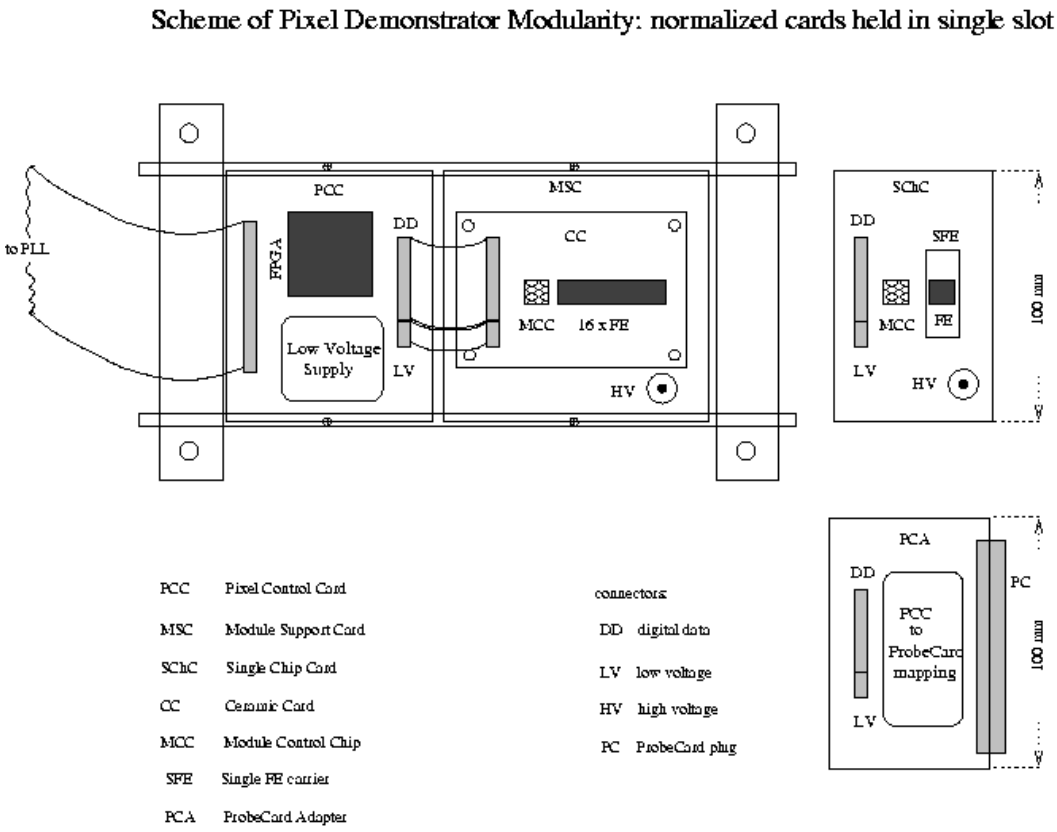

Figure 8-1 Layout of the read-out chain used to transfer data out of the demonstrator

The single-chip, 16-chip and ATLAS modules are mounted on different boards which have a common interface to the read-out system. These cards must also provide mechanical support and heat sinking for the modules, the bias voltage and power connections, the line decoupling capacitors, and load resistors. They also allow probing of signals selected with local jumpers.

The support for the ATLAS prototype has been designed (see Chapter 6) and will soon be available for the module tests aimed at a November 1998 decision on the module type.

8.3 Test Beam Measurements

Test results on electronics and on sensors alone are described in Chapters 4 and 5 of this TDR. In this section we mostly concentrate on test beam results of modules.

The demonstrator was built after several prototyping steps in which different single chip modules using p/n, n^+/p and n^+/n pixel sensors were built and measured. Test beam results on these prototypes are also reported in this section wherever relevant to the ATLAS pixel design.

8.3.1 The Test Beam Set-up

Tests were performed at the CERN H8 beam line. The test set-up, shown in Figure 8-2, consisted

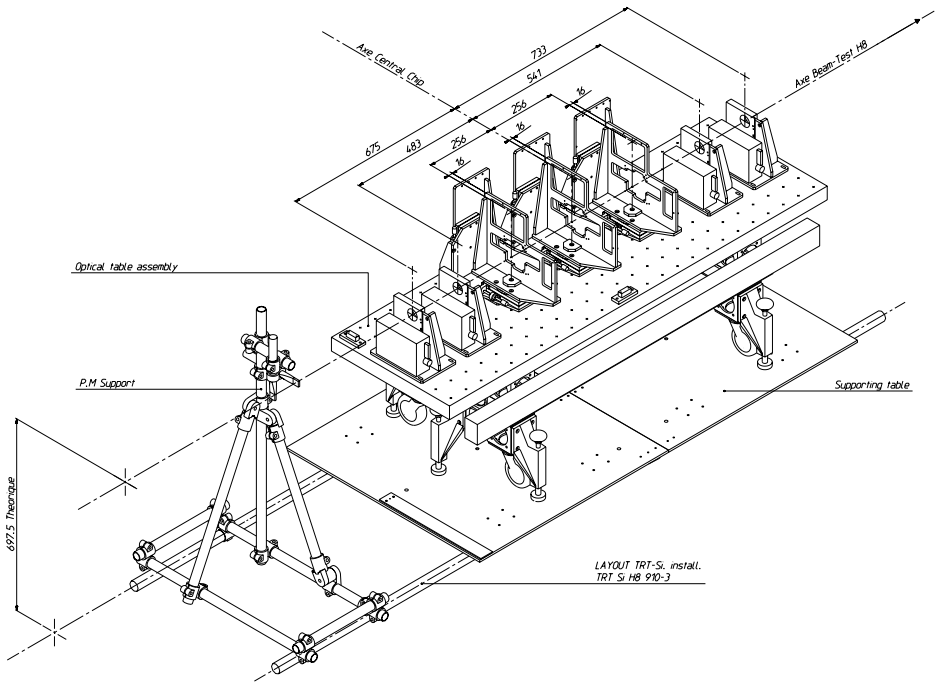

Figure 8-2 View pixel detector test set-up in the CERN H8 test. Two pairs of orthogonal microstrip detectors are each located upstream and downstream of a central location which can accommodate up to three pixel detectors under study.

of a telescope of four silicon microstrip detector doublets fixed to a marble table, with the central part reserved for the pixel detectors under study. Each microstrip doublet consisted of a pair of orthogonal planes of 384 strips with 50 μm pitch, with analogue read-out providing a resolution of **~3** μm.

Two scintillators and one silicon pin diode (5 mm x 5 mm active area) were used for triggering purposes. The beam passage time reference was given by the scintillator, while the diode signal selected tracks known to pass through the pixel array. Pixel detectors were mounted on a rotating platform allowing selectable ϕ and θ orientations, and which could be moved into a 1.56 T

magnetic field. The use of a pin diode (rather than a small scintillator) allowed the pixel trigger element to operate in the field.

A TDC measured the time difference between the trigger and a free-running 40 MHz clock. The TDC information was used to select those particles in time coincidence with the clock, and allows simulation of the LHC operating conditions, where all particles will be synchronized with the 40 MHz clock.

Most of the data were taken with a pion beam of 180 GeV/c momentum. The beam intensity was ~ $2x10^4$ cm^{-2} per burst (2 s out of 14 s). Several types of pixel detectors were tested in this setup. The rad-soft "Beer & Pastis" (B&P: Section 8.3.2.1) and LBL chips were tested in 1997. In 1998, data were collected with both the rad-soft demonstrator FE-A and a rad-hard chip (MAREBO). A second demonstrator chip FE-B will be tested in June. Several data sets were taken, with different detector thresholds and variation of the detector angle over a range +60° to -60° with respect to the beam, in either ϕ or θ. Data were taken with the same orientations in the magnetic field to measure Lorentz angle effects.

The reconstruction programme performed several tasks:

- the reconstruction of clusters in the microstrip detectors and calculation of the track position used a cluster centroid (3 strips around the maximum) algorithm.
- using an "η–algorithm", the response function of the strips was corrected by requiring a uniform distribution of the tracks across each strip.
- strip planes were aligned and tilt angles were taken into account with respect to the first strip plane, which served as a reference. The pixel chip was then aligned relative to that reference plane. The final uncertainty was the angle between the X and Y coordinates of the reference strip plane. This was solved using the pixel chip which by construction measures two orthogonal coordinates. Tracks were then fitted through the four strip planes and χ^2-selected.

8.3.2 Test Beam Results on the Demonstrator Predecessors

8.3.2.1 Results on the "Beer_and_Pastis" chip with digital ToT

The "Beer_and_Pastis" (B&P) pixel array was designed in 1996 at Bonn and CPPM, and was studied 1997 in beam tests at CERN and at the Bonn synchrotron (with 700 MeV electrons). The H8 telescope, described previously, was used as the reference system at CERN while the Bonn beam telescope with 4 planes of double sided strips (to reduce multiple scattering) was used in Bonn. Several B&P chips were bump bonded at LETI and IZM to p/n detectors with a pixel size of 50 µm x 432 µm.

The B&P chip uses the shift register readout described in Section 5.11.1.1 at a speed of 40 MHz. The digital output data of the readout shift register is fed into a Logic Cell Array which locally stores the information after a beam trigger has occurred. The data is then read out via VME. The chip offers the possibility of measuring the analog pulse height using the time over threshold (ToT) technique in which the width of the discriminator output is sampled in units of the bunch crossing clock (25 ns). This technique provides resolutions of 4-5 bits (see Chapter 5).

The threshold and noise of every pixel were determined from measurements of the fraction of hits seen as a function of the charge injected through an on-chip test capacitor. The 50% - point and the slope of the fitted error function give the threshold and noise values. The measurements were made a) using the shift register readout operated at 40 MHz, and b) by observing the discriminator outputs directly on a wired-OR of enabled pixels (the 'hitbus'). Both measurements give the same result, thus indicating no problem of pickup of the 40 MHz clock signal. The threshold homogeneity on a chip bonded to a p^+ in n pixel sensor is shown in Figure 8-3. At an average threshold of 3000 e, the dispersion is 110 e (without threshold tuning) with only small systematic variations from column to column (boundaries indicated in Figure 8-3 by the vertical lines). Some pixels with high thresholds at the edge of the array are due to a bad guard ring connection of the sensor. B&P offers the possibility of individual analog threshold fine-adjustment, but as the dispersion was already low, this feature was not used during the beam running. The pixel noise is homogeneously distributed across the array with an average value of 120 e.

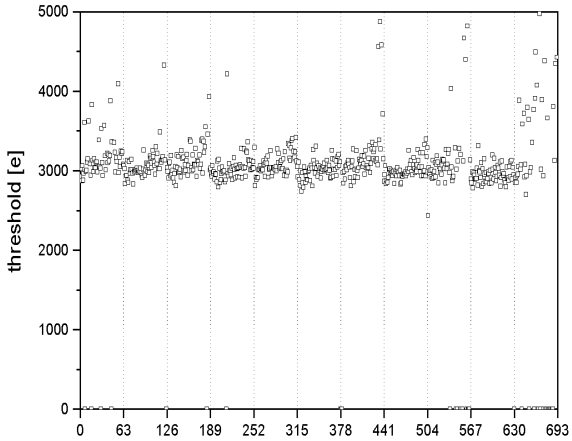

Figure 8-3 Threshold distribution of a B&P chip with sensor

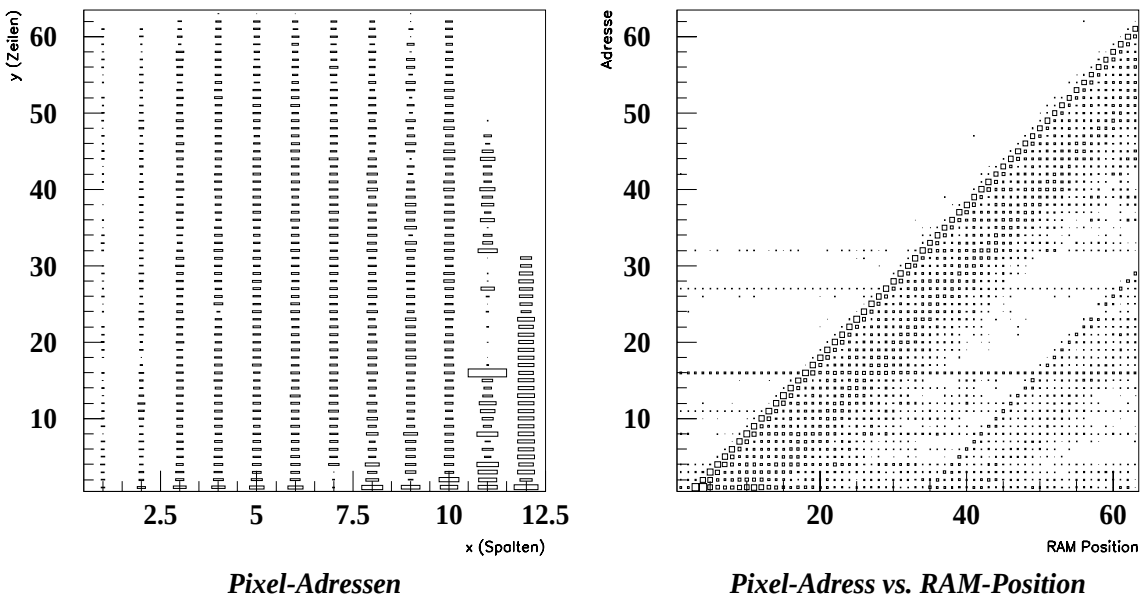

Figure 8-4 Left: hit map (rows versus columns) of the 12 columns and 63 rows of a B&P array. The right-most two columns had a bad guard-ring connection. Right: Correlation between hit information at the output of the chip (address of the pixel in a column) and the arrival time (position in a storage RAM).

Figure 8-4 (left) displays a hit map of the 12 x 63 pixels. The efficiency and homogeneity in the central region are clearly visible. Some inefficiencies or increased hit rate are seen at the edge due to the badly connected detector guard ring. Column 11 of this chip obviously has a readout problem while in the last column, the most significant data bit was temporarily lost due to a bad connector so that the upper half of the array is superimposed on the lower half. The right side of

Figure 8-4 shows the raw data of the shift register (vertical) vs. the buffer position inside the local memory, i.e. the time at which this address has left the shift register. The diagonal is expected for the rising in-time edges. The band below are the falling edges which are smeared according to the ToT pulse height distribution. Some noisy pixels (from column 11) produce the horizontal bands. The missing bit in column 12 created the 'ghost image' in the lower right corner.

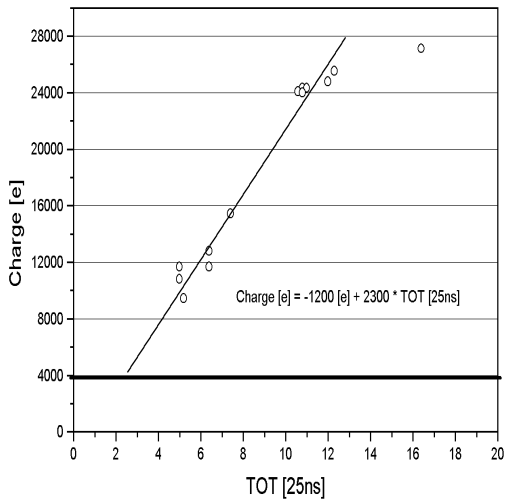

Figure 8-5 ToT calibration: The charge deposited in one pixel is calculated from the impact point and compared to the measured ToT value.

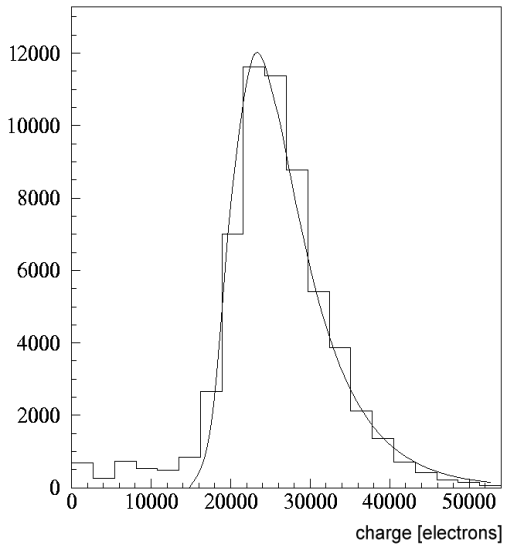

Figure 8-6 Cluster pulse height spectrum measured using the ToT amplitude information.

The charge deposited in one pixel has been calculated from the known impact point of the track (from the telescope) and the detector tilt angle. This value was then used to calibrate the ToT information (Figure 8-5). The extracted calibration constants agree well with the values found in the lab from the injection of known charges into the pixels. A global ToT calibration allowed the measurement of the deposited charges. This is illustrated in Figure 8-6, where the distribution of the total cluster charge (sum of all hit pixels) is plotted. The expected Landau distribution is superimposed to the histogram.

The spatial resolution is determined from the width of the residual distribution: i.e. the difference between the extrapolated impact and the reconstructed position from the pixel chip. This value has then to be corrected for the intrinsic resolution of the telescope which is about 5 µm in the CERN testbeam. Due to the increased multiple scattering of the low energy electrons at the Bonn synchrotron, precise resolution measurements are difficult. Figure 8-7 displays the residuals in the short and long pixel direction for a purely binary data analysis for perpendicular tracks. The resulting pixel resolutions are σ_{long} = 123 µm and σ_{short} = 12.7 µm for the long and short direction, respectively.

The spatial resolution should be best for tracks which deposit charge between two pixels and produce double hits. This is illustrated in Figure 8-8, where only double hits from perpendicular tracks are analyzed. Note that the distribution has a long tail with large reconstruction errors from tracks which are far away from the pixel edge. This is clearly visible on the right side where the extrapolated impact positions of the considered tracks inside the pixel are shown. Re-

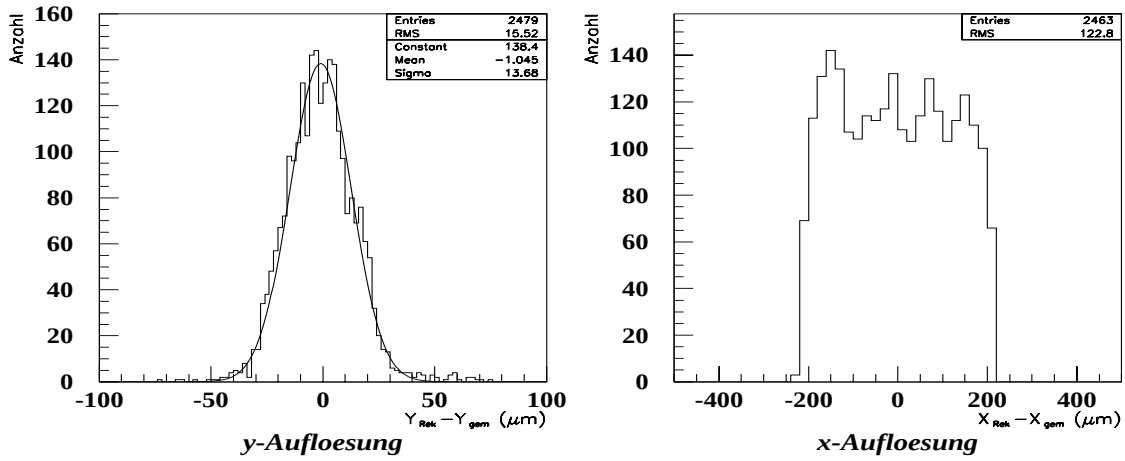

Figure 8-7 Residual distributions in the short (left) and long (right) pixel directions for perpendicular tracks using binary data analysis.

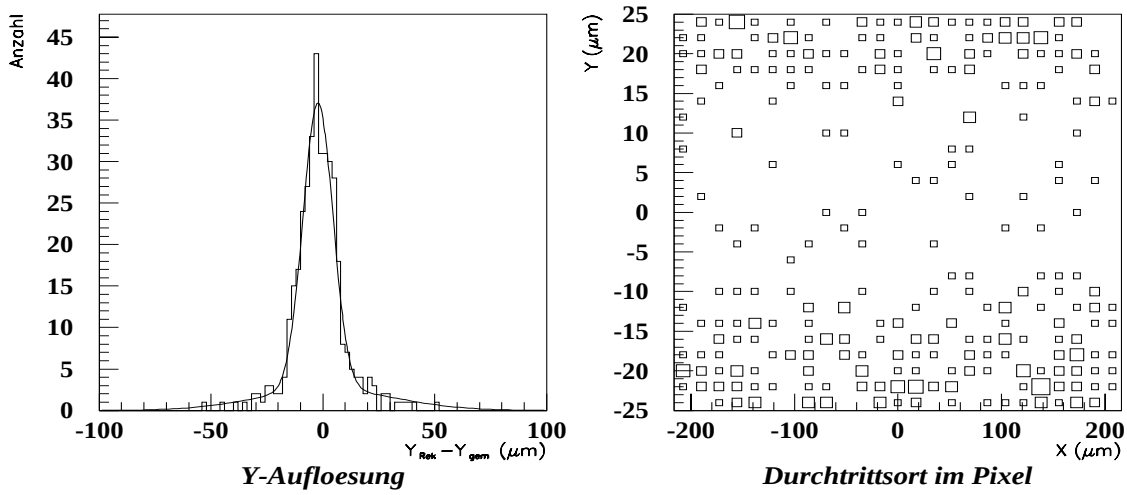

Figure 8-8 Residual distribution (left) and impact points (right) for double hits from perpendicular tracks (binary readout).

moving large charge depositions by means of a cut on the ToT pulse height removes these tails and increases the resolution significantly. This is demonstrated in Figure 8-9. The width of the residual distribution leads to a resolution of 4.2 μm after quadratic subtraction of the telescope resolution. A possible source of hits with large charge are δ-electrons, which are preferentially emitted perpendicular to the particle track and which can therefore deposit considerable energy at a position displaced from the track. This leads to an irrecoverable reconstruction error.

The spatial resolution can be improved by using the ToT amplitude information for clusters with two or more hits. This is illustrated in Figure 8-10 where the residuals for a sample of double hits at an impact angle of 10 ^{o} are shown for a binary data analysis (left) and an analysis using the ToT information (right). The spatial resolution (after deconvolution of the telescope resolution of 5 μm) improves from 11 μm to 5 μm. The improvement due to analog data analysis of the complete data sample is smaller, as single hits do not benefit from the ToT information. The fraction of multiple hits depends in particular on the impact angle of the tracks and on the Lorentz angle. While a fraction of 50% of single hits is the theoretical optimum for a binary

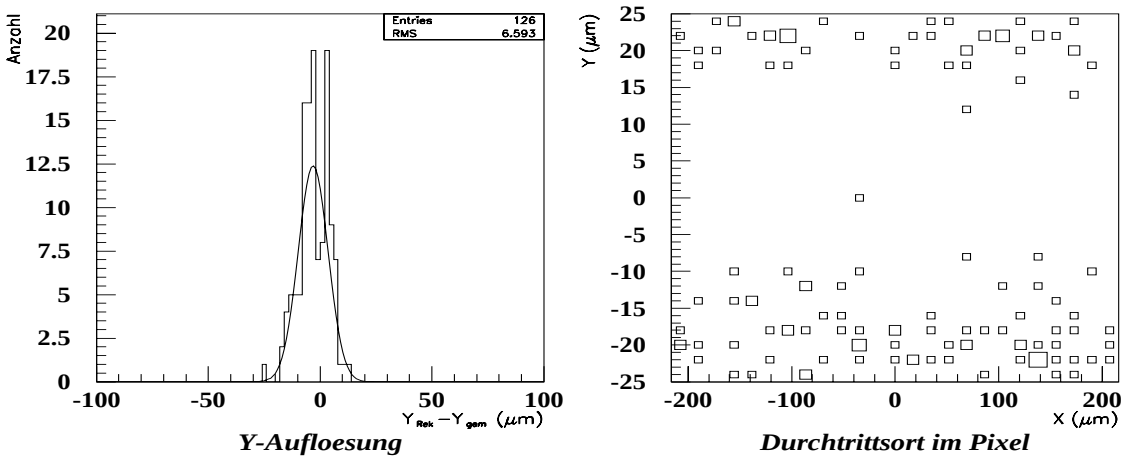

Figure 8-9 Residual distribution (left) and impact points (right) for double hits from perpendicular tracks with cut on ToT pulse height (binary readout).

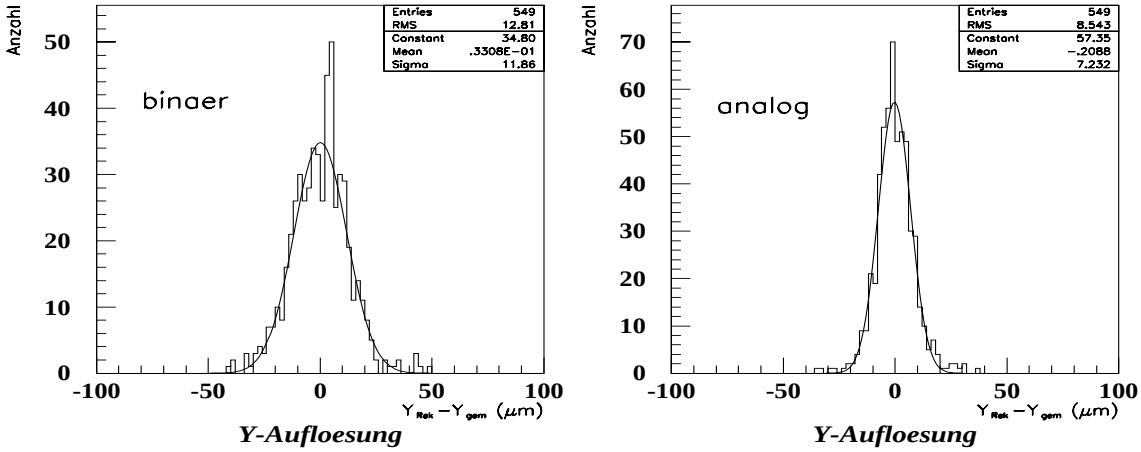

Figure 8-10 Residual distribution for double hits from 10º-tracks obtained by binary (left) and analog (right) data analysis.

readout (this doubles the resolution compared to 100% single hits), a greater fraction of double hits is beneficial for analog readout. On the other hand, the increased spread of the signals over several pixels reduces the signal amplitude which in turn can lead to larger reconstruction errors. Note that due to the particular geometry of the pixels, a vertical track deposits a charge in one pixel which corresponds to the full wafer thickness of 300 µm while a track traversing at 45º relative to the short pixel axis deposits only the charge from the traversal of 70 µm of silicon. The improvement in spatial resolution in the short pixel direction for binary and analog data analysis is summarized in Figure 8-11. The values for exclusive double hits are plotted on the left side as a function of the track angle. The total resolution is shown on the right side. The improvement in resolution for small tilt angles is clearly visible. The distributions are not exactly symmetric, a systematic effect which results most likely from the position of the pixel cells with respect to the shift direction of the column shift register. The effect is under study. The analog information improves the values by typically 1-2 µm.

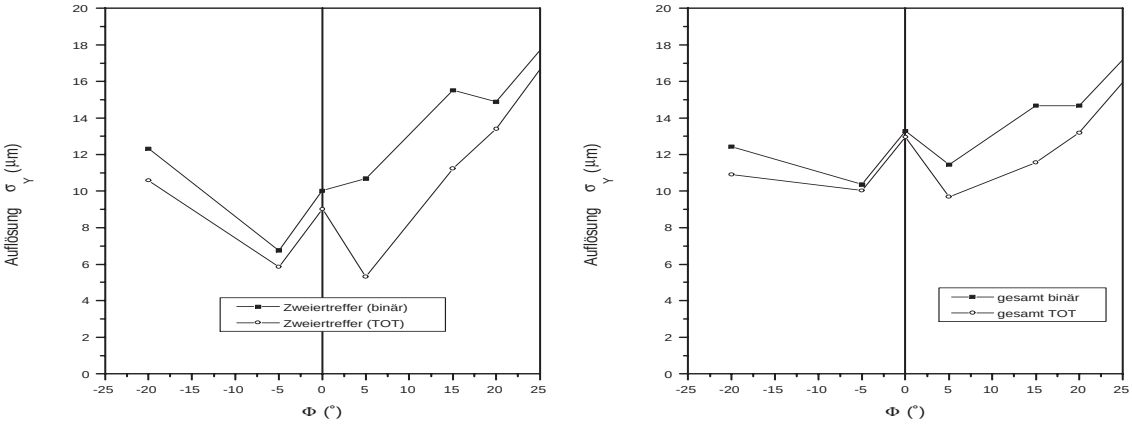

Figure 8-11 Resolutions in the short pixel direction for double hits (left) and all hits (right) as a function of the track impact angle. The impact point has been reconstructed using only binary information (solid) and using the analog ToT amplitude (open).

The situation for the resolution in the long (432 µm) pixel direction is summarized in

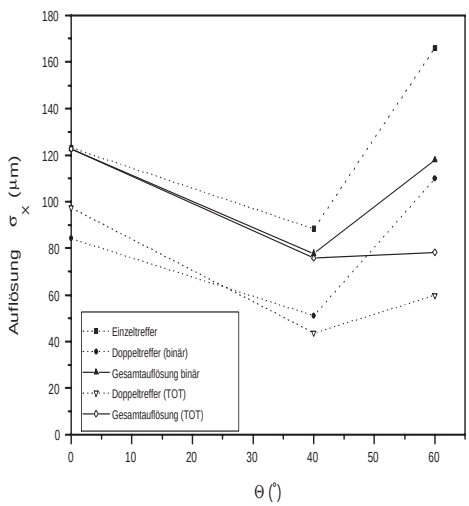

Figure 8-12 Spatial resolution in the long (432 µm) pixel direction for various impact angles. The solid curves are the total resolution for binary (triangle) and analog (diamond) analyses.

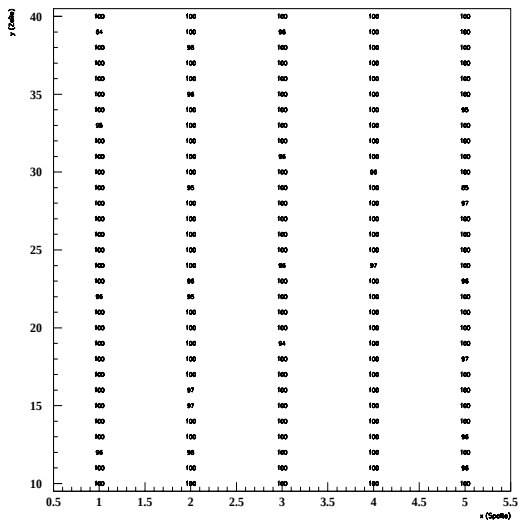

Figure 8-13 Efficiency of the central region of the B&P pixel chip.

Figure 8-19 as a function of the impact angle for various hit configurations and analysis methods. The solid curves are the total resolution for binary (triangle) and analog (diamond) analyses. At vertical impact with only few double hits in the long direction, the expected resolution of 432 µm / √12 = 124 µm is obtained. The resolution improves for inclined tracks due to the pres-

ence of more double hits. At very shallow track angles the analog ToT information can improve the resolution significantly.

The track reconstruction efficiency is estimated by searching for a cluster in a 5σ region around every track. The numbers obtained for typically 50 tracks per pixel are displayed in Figure 8-13: 83% of the pixels are fully efficient and the average efficiency is 99% including two less efficient pixels with 64% and 85%, respectively.

A fast response time of the preamplifier / discriminator system is crucial in order to correctly associate events to the 25 ns bunch crossing interval. The crossing clock on the pixel chips in ATLAS will be in phase with the interactions. This is not the case in beam tests where events can occur at an arbitrary time with respect to the free running pixel clock. A TDC is therefore used to measure the relative time difference between the interaction and the 40 MHz pixel clock. The efficiency of the hit reconstruction as a function of TDC time difference is shown in Figure 8-14 for various impact angles. Starting from a plateau at the correct interaction time, the efficiency drops as expected to zero when the particles arrive delays approaching one bunch spacing (25 ns). The plateau implies no problems with data loss due to a too slow response of the discriminator.

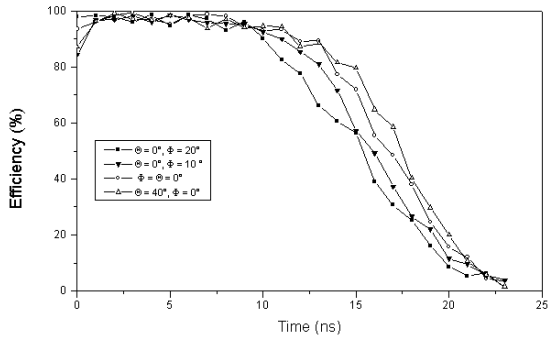

Figure 8-14 Efficiency of the readout as a function of the interaction time with respect to the pixel clock for various impact angles.

Due to the relatively low effective preamplifier input capacitance, a charge deposited in one pixel can capacitively cross-couple to the nearest neighbours through the inter-pixel capacitances. This effect could lead to wider clusters and to an increased data rate. The distribution of cluster sizes (all possible hit combinations) was therefore studied, and is shown in Figure 8-15. Only a small number of triple hits is observed despite the relatively low threshold setting (3000 e). Triple hits are expected if cross-coupling is present (we define here the cross-coupling as the fractional charge seen on one neighbour). In events where the deposited charge in one pixel exceeds (threshold / cross-coupling), hits in 3 adjacent pixels are expected. The triple clusters of Figure 8-15 can have different topologies - some may be due to δ-electrons - so that the rate of triple hits from cross-coupling is below the 6% rate of triple hits seen in Figure 8-15.

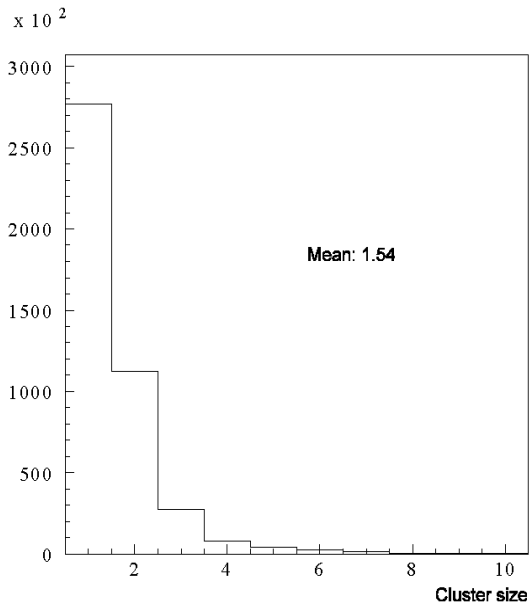

Figure 8-15 Distribution of cluster sizes.

8.3.2.2 Results on an LBL Prototype Array with Analog Readout

The first LBL prototype pixel array was produced in 1996 and extensively tested in 1997. The details of this design are described in Chapter 5. This array includes complete end-of-column logic, and provides hit information (time and address) as well as analog charge information (linear ToT) for each hit which is above a discriminator threshold and is in-time with a 40 MHz beam-crossing trigger. The chip is capable of storing up to eight events prior to a trigger coincidence, but only four events pending readout. It was typically operated with a trigger input which covered four consecutive 40 MHz beam-crossings, providing the readout of 100 ns of consecutive time, but with all hits labeled by 40 MHz beam-crossing number, allowing offline analysis of timing performance. This turned out to be quite useful, as the array with detectors required about 50 ns to account for timewalk of small input pulses. Furthermore, since the testbeam data is not synchronized with the 40 MHz clock on the pixel array, it is useful to read out one additional crossing to retain full efficiency for all arrival times of the beam particles relative to the 40 MHz crossing clock.

In Spring 1997, this electronics array was bump-bonded to detectors fabricated by LBL using n^+ implants in p-bulk material. This detector design is simple to fabricate, as it only involves single-sided processing with an un-patterned back side used to apply the negative bias voltage. The detector depletes from the n^+ implant side, and is partially depleted to a depth of about 50 μm, even in the absence of any applied bias, due to the presence of positive oxide charge. Such detectors can be readily operated in a partially depleted mode which simulates the behaviour of heavily irradiated n^+ on n-bulk detectors, without the presence of leakage current. With the detector mounted on the electronics, operation at thresholds of 3000 e to 5000 e was possible. The threshold for the testbeam results shown for the p-bulk detectors was measured to be about 3500 e.

Two detector assemblies of this type were tested in the CERN H8 testbeam telescope described previously. These detectors were bump-bonded by Boeing using an evaporated Indium process. The yield was excellent, as shown for one of the detector assemblies in Figure 8-16, where of the 703 channels expected to be functional, all channels do in fact work. The twelfth column is dead due to a layout error in the chip. The odd/even row modulation is due to the “bricked” detector geometry, where alternate rows are staggered in the long (z) direction by a half pixel. When combined with the square acceptance region of the 5x5 mm trigger diode, this produces odd-even variations in the hit occupancy near the edge of the trigger acceptance. The hits outside of the trigger acceptance arise from cases where a second particle accompanied the trigger particle. One of the “bricked” detectors is shown in a photomicrograph in Figure 8-17 to clarify the geometry. The virtue of this detector geometry is that for hits with adequate charge sharing in the $r\phi$ direction the z resolution is improved by up to a factor of two. This effect is displayed in Figure 8-19, where it can be seen that the resolution improves from roughly 120 μm for normal incidence (minimal charge sharing) to about 90 μm beyond about 10° in $R\phi$, where the charge sharing with neighboring pixels is significant.

These detectors were operated in a partially depleted mode, with a typical bias voltage of 40V, corresponding to slightly more than 200 μm depletion depth. The main consequence is a reduction in collected charge. Resolution studies were performed as a function of the angle of incidence of the charged particles by rotating the detector assembly on a stage on the telescope table. Resolutions were computed after clustering the hits in the pixel array using a nearest neighbour algorithm. For a binary resolution, a centroid was computed by including each hit with equal weight. An analog resolution was computed using an analog centroid calculation, after correcting the measured charge in each hit pixel for the calibrated response which converted ADC counts to equivalent input charge. Some sample results are shown in Figure 8-18. For

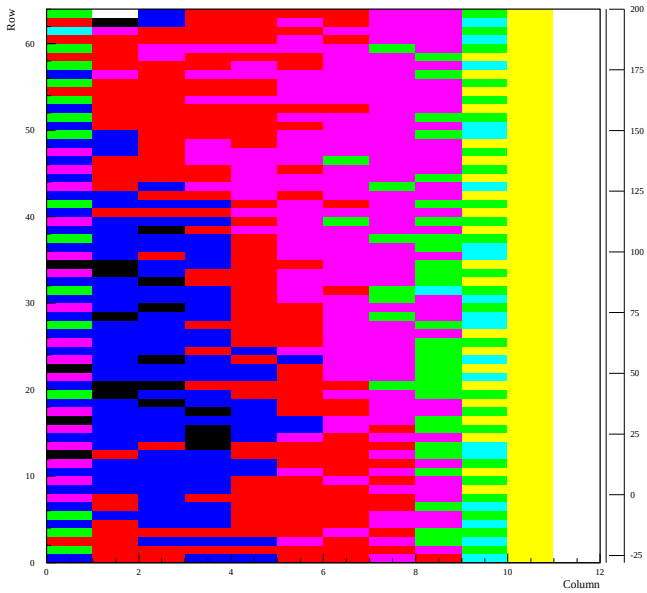

Figure 8-16 Hit map from a p-bulk detector bump-bonded to readout electronics using Indium bumps.

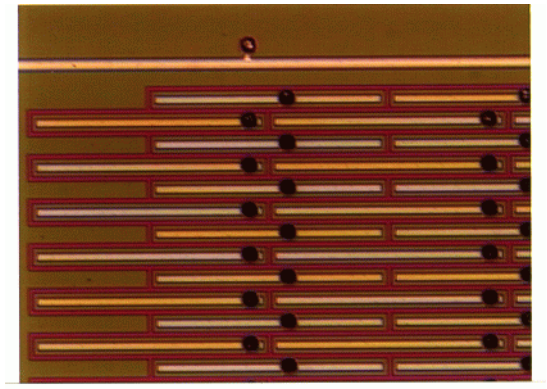

Figure 8-17 Implant configuration for LBL "bricked" detector design. The 20 µm diameter Indium bumps are clearly visible.

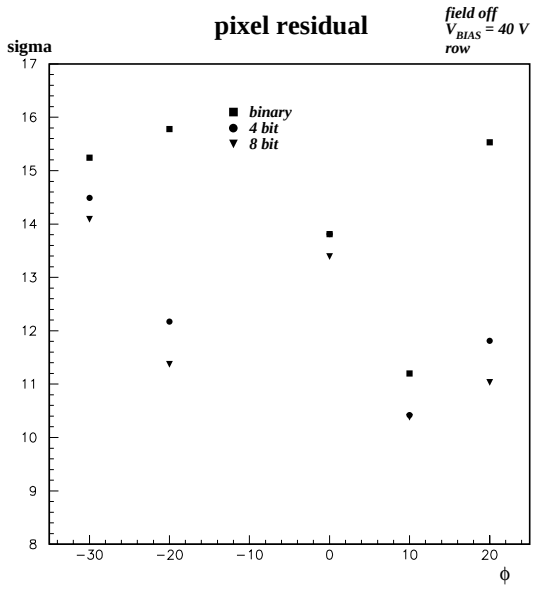

Figure 8-18 Resolution in narrow direction as a function of incident angle. Different techniques for computing the cluster position have been used.

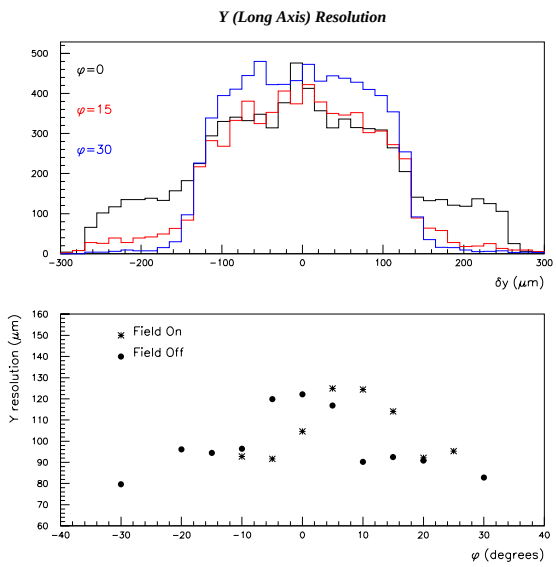

Figure 8-19 Resolution in the long direction of the pixels as a function of the angle of incidence in the narrow direction.

the applied bias voltage in this case, an incidence angle of 10° corresponds to a cluster size in the Rϕ direction which is roughly an equal mixture of single and double hits. For an angle of incidence of 20°, the clusters are approximately two pixels wide in Rϕ. These two cases correspond approximately to the best and worst situations for a binary centroid method. Thus, the best binary resolution is achieved at 10°, and the worst is achieved at 20°. The analog performance is more uniform, but not significantly better than the binary resolution. Note that these

resolutions represent the convolution of the true pixel resolution with the strip telescope resolution. Based on the covariance matrix from the telescope track fit, the extrapolation precision on the pixel array should be about 5 µm, but the presence of small amounts of material, not accounted for in the present telescope fitting procedure, degrades this to about 7-8 µm. Thus the analog resolution could be as good as 7-8 µm, but is more likely to be 8-9 µm after convolution. Further analysis of the testbeam telescope fitting is required to improve these estimates.

The detector assemblies using p-bulk detectors were operated at several bias voltages, in order to study the performance of the electronics and detector for different depletion depths. The observed charge distributions, after correction for the ToT calibration of the individual pixels, are shown in Figure 8-20. The detector should be fully depleted at the highest bias voltage, and so

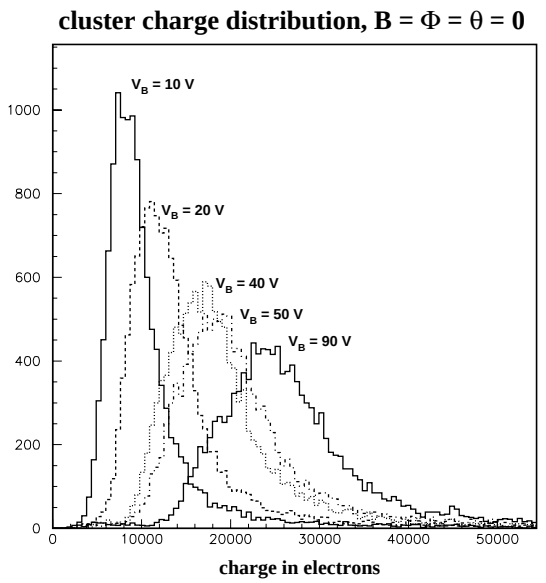

Figure 8-20 Charge distributions as a function of the bias voltage for the p-bulk detectors.

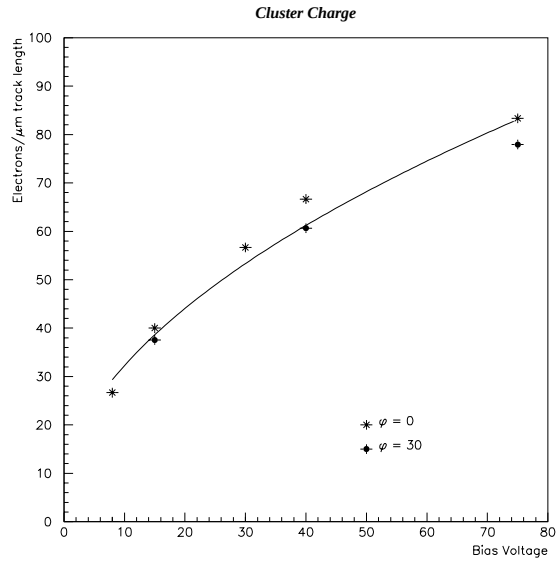

Figure 8-21 Observed most probable charge normalized to the total path length, and plotted as a function of the bias voltage.

an initial scale error of about 0.8 has been removed by normalizing the most probable charge to roughly the expected value of 24Ke for 300 µm of silicon. Although the initial calibration depends on the value of a small charge injection capacitor with a value of approximately 5 fF, this deviation was larger than expected, and is not understood. At the lowest bias voltage of 10 V, the detector was expected to be depleted to a depth of only about 100 µm. The variation of the observed most-probable charge versus bias voltage is displayed in Figure 8-21, with a fitted curve proportional to the square-root of the bias voltage superimposed. The observed charge, which should be proportional to the depletion depth, does indeed follow the expected behaviour, and indicates a depletion at zero bias of about 50 µm, which was expected based on the detector doping. The charge follows the expected behaviour for both normal incidence and 30° angle of incidence in the Rϕ direction.

Careful studies of the efficiency for reconstructing a cluster in the pixel array were also performed. For these studies, it is essential to have very high quality telescope tracks to ensure that no inefficiencies develop because of poor reconstruction of tracks in the strip planes. This is done by requiring one and only one cluster in each of the strip planes, and making tight χ^2 cuts

on the quality of the strip track fit. The matching between the extrapolated strip telescope track and the pixel array was allowed to be fairly loose to account for resolutions, and a fiducial region was defined, far from the edges of the pixel array. The matching in the narrow direction

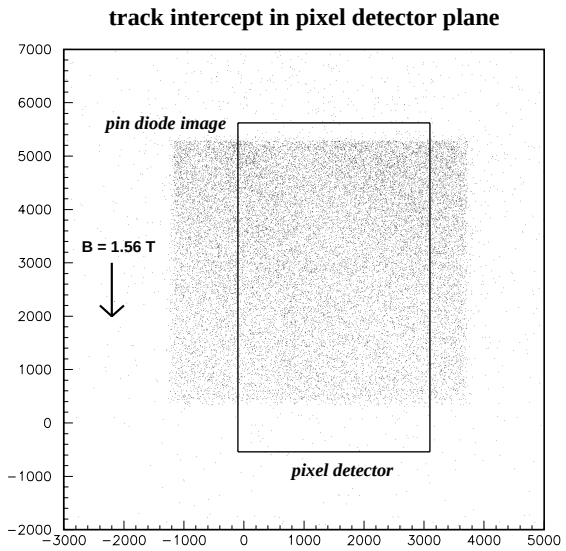

Figure 8-22 Observed extrapolated track positions on the pixel array. The active region of the array is indicated by the rectangular outline, with the narrow direction corresponding to the narrow direction of the pixels themselves. The outline of the trigger diode is apparent.

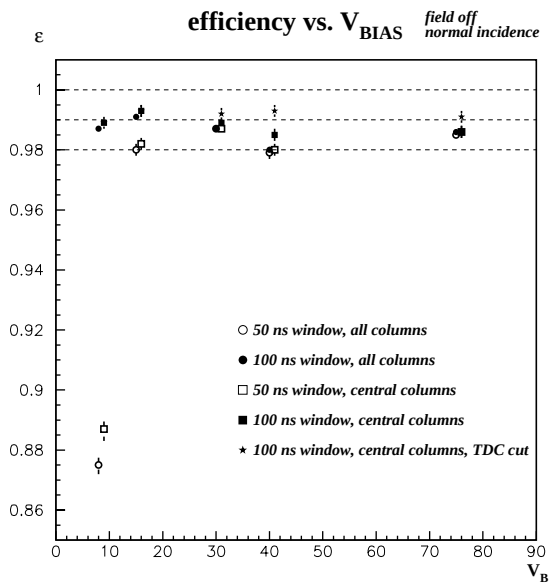

Figure 8-23 The measured efficiency of track matching to a cluster in the pixel array for the p-bulk detectors. The detector bias was varied, changing the depletion depth and reducing the observed charge.

was 150 µm, and in the long direction was 1000 µm. The test beam configuration is indicated in Figure 8-22, showing the active area of the pixel array and the trigger region defined by the PIN diode. In this arrangement, tracks were required to intercept the pixel array more than 100µm away from the edge of the active region to avoid possible matching problems near the edge of the array. The results are shown in Figure 8-23, where two different sensitive times have been plotted. The 100 ns points use all four crossings worth of hit information from the pixel array, and correspond to a true sensitive time of about 85 ns, due to the random arrival time of the beam relative to the 40 MHz clock. The 50 ns point is closer to the true LHC operation, although this pixel array does not yet fully meet the 25 ns LHC timewalk requirement. The array operated efficiently down to bias voltages of 10V for the longer sensitive time, providing an efficiency of about 99% (statistical errors are shown on the plot). This data was recorded at normal incidence, where the pixel cluster size is very close to 1 hit pixel, particularly for the smaller depletion voltages, so the cluster efficiency and the hit efficiency are almost identical.

A total of five assemblies were bump-bonded using pixel detectors of the same geometry, fabricated by Hamamatsu. These detectors used n^+ implants on n-bulk material, with a single window-frame of 5 µm wide p-stops to isolate the pixel implants. This geometry was virtually identical to that of the LBL p-bulk detectors. The backside was patterned with a simple guard structure. The depletion voltage of these detectors was typically about 75 V, and they were operated at bias voltages of 100-200 V with very low bias currents. The nominal thresholds were chosen to be in the range of 4-5 ke range, since these detectors can only be operated fully depleted, and hence there is no need to go lower in threshold. The thresholds and noise behaviour for

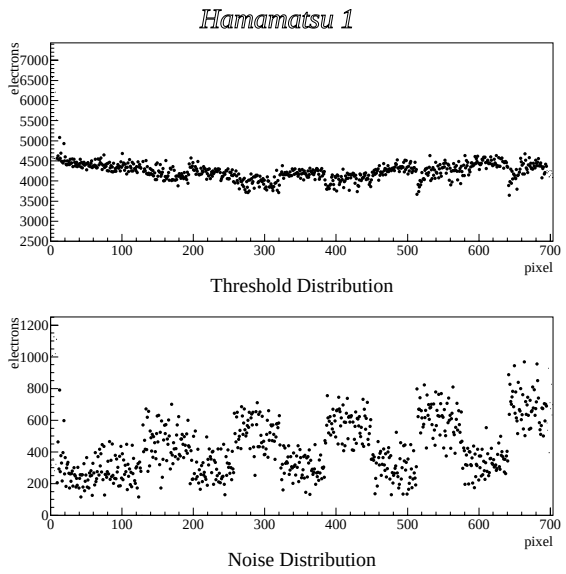

Figure 8-24 The results of fitting the threshold curves for a pixel array bonded to the first Hamamatsu detector. The upper plot has the fitted threshold for each pixel in the array, and the lower plot is the fitted noise.

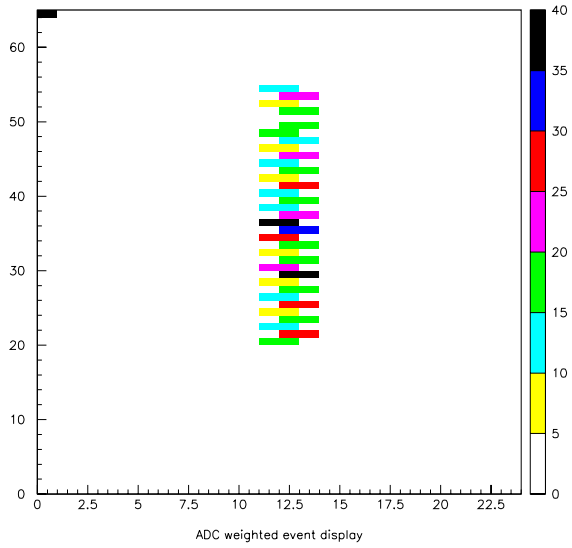

Figure 8-25 Single event display for a run at grazing incidence (80°) showing the very long clusters observed.

each pixel were measured by injecting charge into the internal calibration capacitors, and scanning this charge value across the pixel discriminator thresholds. The resulting curves were fit to error functions to extract the threshold (50% probability for pixel to fire) and the noise (width of the threshold turn-on curve). The results are displayed in Figure 8-24. In this generation of pixel array, there was a grounding connection missing in all pixels in even columns except the first column. This resulted in rather poor ground referencing between the preamplifier and the discriminator, and caused many significant effects in the array performance. The threshold variations in this particular assembly were not large, but a very significant degradation of the noise performance can be seen. The noise in the “good” columns is roughly the expected 350e, but the noise in the defective columns is typically a factor of two higher. Since the charge measurement is based on ToT information, it is also somewhat compromised by the same defect.

Studies were performed at a variety of different angles of incidence, from 0° (normal incidence) up to almost grazing incidence of 80°. A typical event display is shown in Figure 8-25. Note that at this angle of incidence, the charge deposited in each pixel corresponds to a track length of only about 50 µm of silicon, since the pixel is traversed from the side. Thus, the observation of such a high efficiency (most pixels traversed appear as hit) indicates that the threshold must be less than or equal to about 4 ke. Note also that the storage of the hit information in the pixels themselves provides an unlimited ability to visualize single events with this readout architecture.

Efficiencies were also studied for the n^+ on n-bulk detectors, using the same selection criteria as before. The efficiency averaged either over a column or over a row of pixels is displayed in Figure 8-26. The average efficiency is again about 99%, and shows no signs of large variations across the array. Cluster positions were calculated using both binary centroids and analog centroids, as before. An example of the residuals between the strip telescope track and the pixel cluster, for an angle of incidence of 0°, are shown in Figure 8-27. The distribution in the Rϕ direction is very clean and Gaussian. Gaussian fits were used to extract the resolution in this pro-

jection. The results for different algorithms and angles of incidence are shown in Figure 8-28.

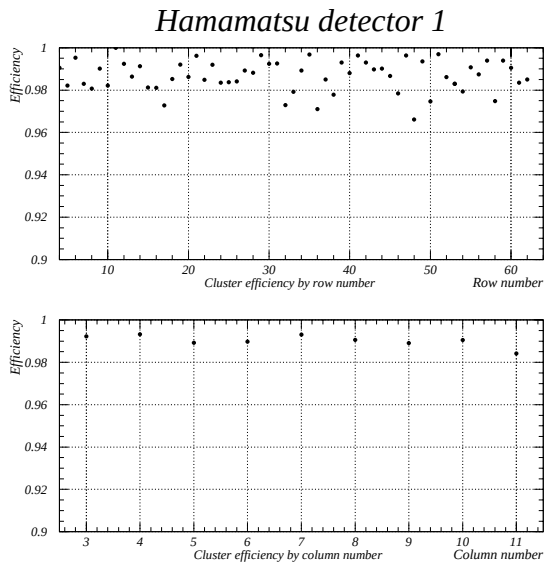

Figure 8-26 Efficiency extracted as a function of the row number or the column number for the first Hamamatsu detector.

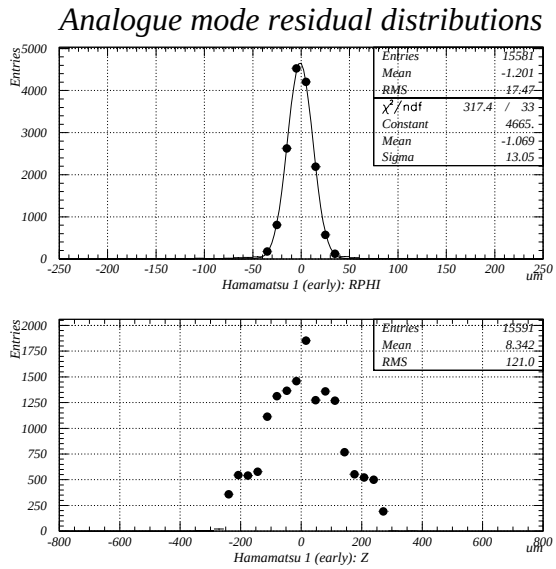

Figure 8-27 Residual distribution for matching between a strip track and a pixel cluster for the first Hamamatsu detector.

Note that in this case, resolutions with and without magnetic field are shown. The extrapolated strip track precision is estimated to be about 5μm for field off, and 7 μm for field on.

Finally, an analysis of the width of clusters in the pixel array was performed at different angles of incidence, with and without the magnetic field. Due to the magnetic field, the drifting charge cloud will follow a displaced trajectory, and will appear shifted. Since detectors with n^+ implants collect electrons, and their mobility is rather high, the expected effect is relatively large. For a field of 2 T, we expect about 16° for the Lorentz angle. In H8, the field in the center of the dipole is about 1.5 T, and so we should expect a Lorentz angle of around 12°. The data has been analyzed in two different ways. First, the large angle of incidence data, which is dominated by purely geometric effects, can be extrapolated using straight lines to small incidence angle. These fits give a result of about 9.1° for the Lorentz angle. An alternate method, which depends on the details of the charge sharing effects at small angles of incidence, has also been used. In this case, a quadratic curve is fit to the cluster width data for small incidence angles, and the minimum of this fit determines the Lorentz angle. This method gives a consistent result of 8.9°. Both of these results are somewhat smaller than the mobility of electrons themselves would suggest, so perhaps the explanation is that for the slower shaping times of the present chip, there is some sensitivity to the holes as well, and their mobility is much smaller. The data on cluster width, and the results of the two fits, are shown in Figure 8-29.

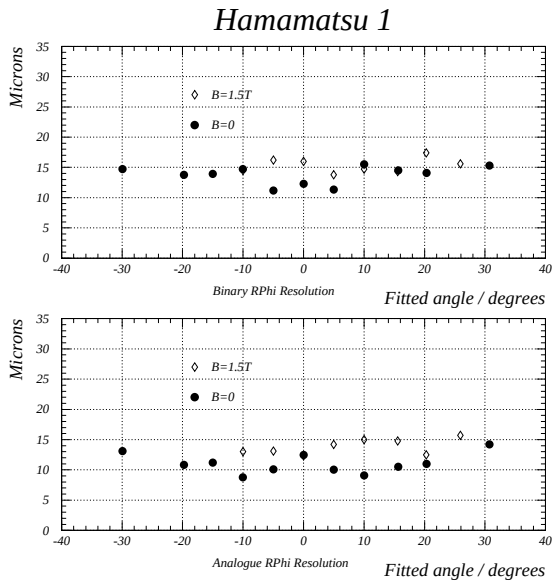

Figure 8-28 Binary and analog resolutions calculated by performing Gaussian fits to the residual distributions for different track incidence angles.

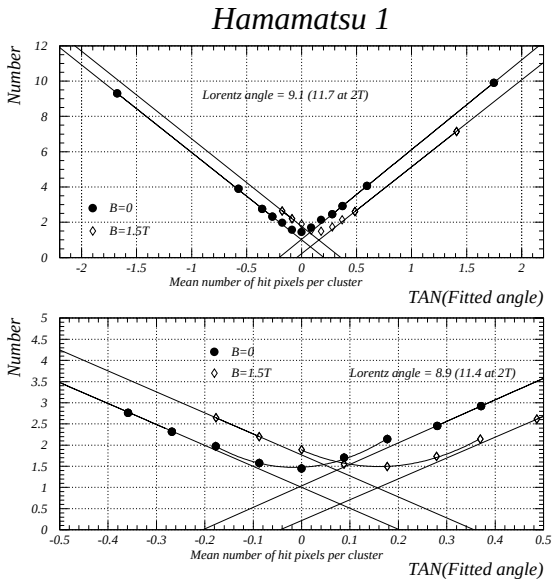

Figure 8-29 Variation of the cluster width as a function of angle of incidence, with and without magnetic field. The fits for the Lorentz angle are shown.

8.3.2.3 Results on MAREBO (rad-hard)

The rad-hard MAREBO chip was tested in the April 1998 testbeam at CERN. Therefore only preliminary results are presented here.

MAREBO is to a large extent the radhard DMILL version of the B&P chip successfully tested in the lab and the test beam in 1997 (Section 5.11.1). It also has the same front end architecture (e^- collection for n^+/n sensors) as the FE-A (PIRATE) chip and fully meets the analog functionality requirements of ATLAS. MAREBO consists of an array of 12 x 63 cells, each cell facing a pixel of 50 µm x 432 µm area. The readout architecture shifts each column into an external memory, where the selection of any of the 128 BCOs following the pixel hit is performed (Section 5.11.1.2). MAREBO has been operated with a threshold of about 3500 e^- with a detector depleted at -150 V. The analog test beam performance of the MAREBO chip bonded to a sensor is considered a bench mark test of the rad-hard DMILL chip technology under true ATLAS conditions.

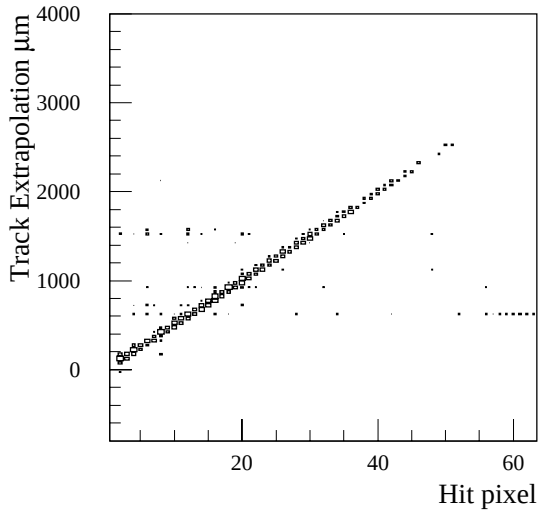

Figure 8-30 Correlation between the track extrapolation and the hit pixel seen in the MAREBO pixel readout chip.

The pixel readout worked as expected. When selecting the optimal BCO, a clear correlation between hit pixels in one BCO and the strip extrapolation is seen, as shown in Figure 8-30. The chip was tilted at a θ angle of 60 degrees. The efficiency of finding a pixel hit within the correct BCO and inside a box of 3x3 pixels is shown in Figure 8-31. Efficiency above 98% was measured over most of the channels, giving a mean efficiency of 80% taking account of several channels which did not work properly due to processing problems on the bipolar part of the circuit[1]. Hits are missing on the upper part of the plot as the beam did not illuminate the whole pixel detector active area during this run.

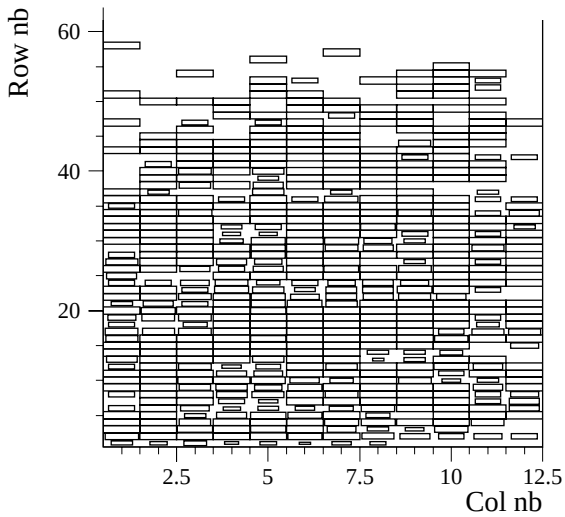

Figure 8-31 Scatter plot of the in-time efficiency for a pixel detector read out with the MAREBO chip. Each rectangle represents a pixel whose area is proportional to its efficiency

The significance of these results is limited by the poor statistics; only 13000 events were recorded at the end of the April run. More data will be taken in June 1998.

8.3.3 Test beam results with the demonstrator

The single chip module using a FE-A (PIRATE) chip on a n^+/n sensor was tested in April 1998. It was routinely operated at a threshold of 3000 e^- on a detector depleted at -150 V. The results shown here are preliminary and refer to normal incidence beam with no magnetic field.

The FE-A chip contains the complete read-out architecture needed for LHC operation, including time stamping to a precision of one BCO, and serialization of the data output. The **threshold performance** of the sensor/chip assembly is shown in Figure 8-32 showing the individual threshold settings measured by threshold scans before threshold tuning. Figure 8-33 shows the same measurement after threshold adjust and Figure 8-34 and Figure 8-35 show the respective projections. The entries with larger threshold values largely belong to pixel Front End cells which are connected to two sensor pixels in the overlap region between chips and are therefore exposed to a double capacitance.

In the testbeam, the pixel readout worked as expected, as can be seen from the correlation between hit pixels in one BCO and the extrapolation of the track as measured by the telescope, shown in Figure 8-36. This figure also illustrates that the noise (i.e. the number of hits outside the correlation region) is very low.

The **noise probability** was measured from the number of hits outside the correlation region. This measurement includes the particle correlated noise (including δ-rays and cross-coupling) and hits generated by upstream interactions not vetoed by the beam trigger condition. The result is a spurious hit probability of $7\ 10^{-6}$ per pixel per BCO.

1. These problems can be traced to layout details of the design and are now understood.

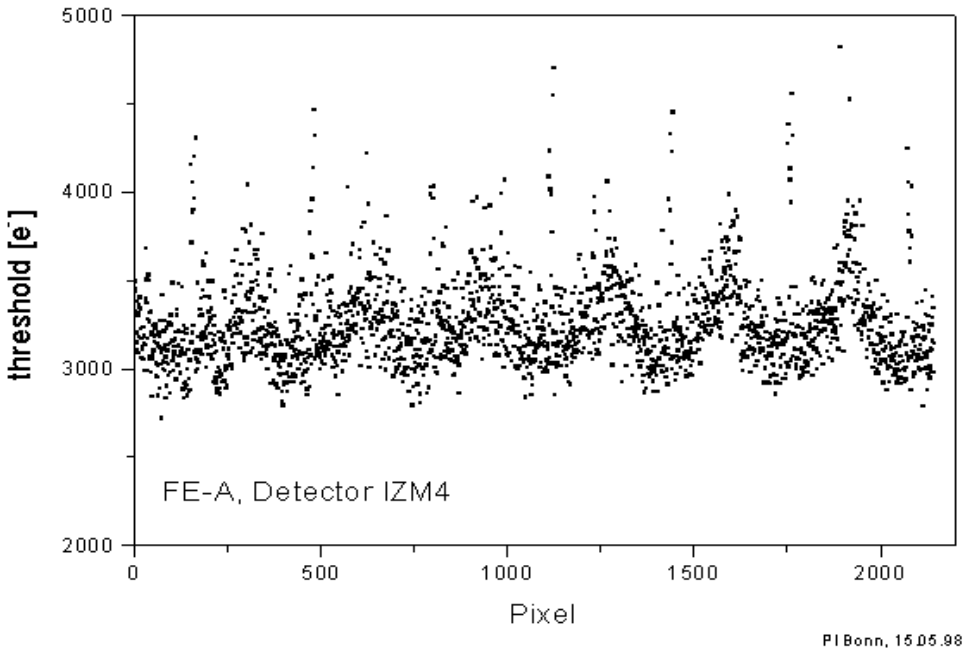

Figure 8-32 FE-A: Threshold scan of the FE-A demonstrator chip connected to a tile-2 type sensor (ST2) before individual threshold adjust. Note that the y-scale has a suppressed zero running from 2000 e to 5000 e. The nominal threshold was set to 3200 e. The overall rms is 184 e.

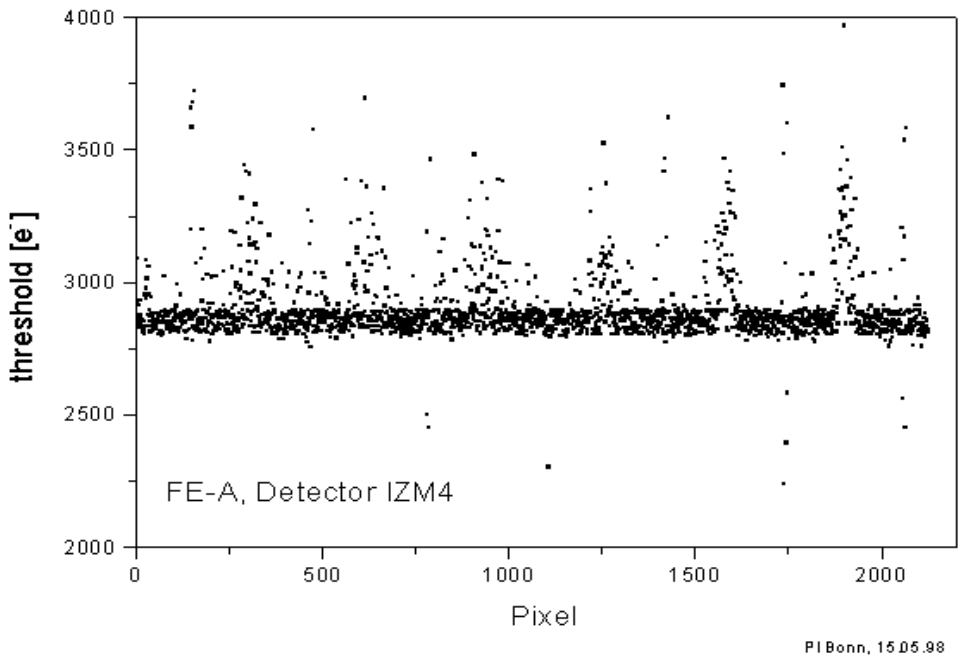

Figure 8-33 FE-A: Same as Figure 8-32, but the thresholds are now tuned to 2850 e.

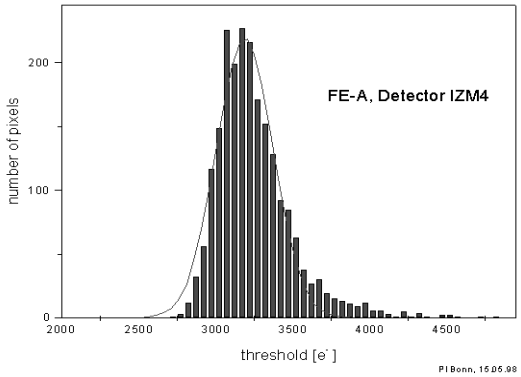

Figure 8-34 Threshold distribution of FE-A/ST2 assembly before threshold adjust. The measured rms is 184e at a nominal threshold setting of 3200 e.

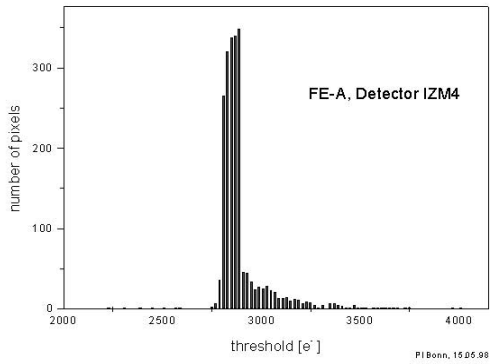

Figure 8-35 Threshold distribution of FE-A/ST2 assembly after threshold adjust. The measured rms (ignoring the tails) is 36 e at a tuned threshold setting of 2850 e.

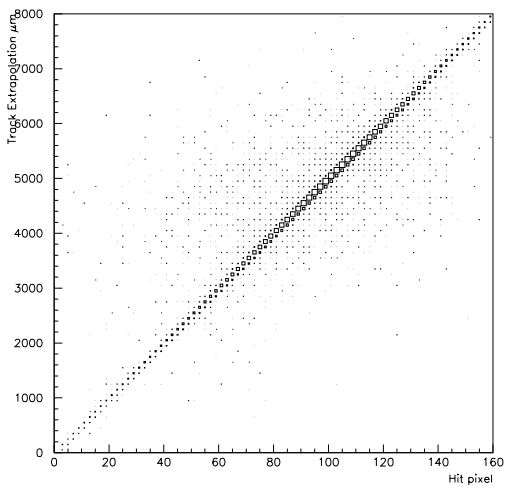

Figure 8-36 Correlation between the track extrapolation and the hit pixel as seen by the FE-A chip.

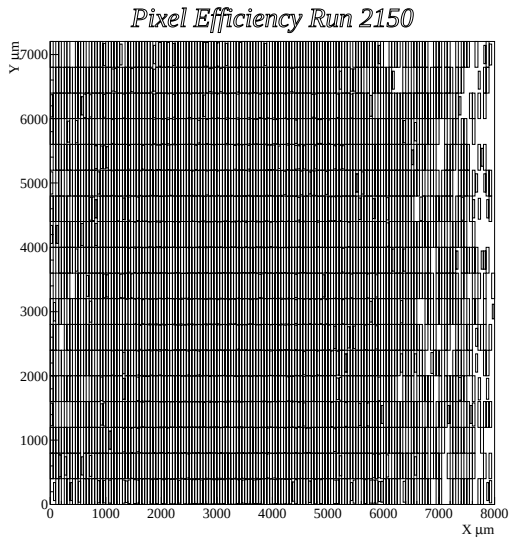

Figure 8-37 Scatter plot of the efficiency over the active area of the FE-A pixel module. Each rectangle represents a pixel whose area is proportional to its efficiency.

There are no noisy pixels, except the “double” pixels (#153, 155, 157 and 159 in each column) which, because of the larger capacitance, cannot work at 3000 e^- threshold and have therefore been masked in these data sets.

The **efficiency for finding a pixel hit** in the correct BCO within a box of 3x3 pixels is 97%. This is obtained as the maximal efficiency in a single 25 ns TDC bucket, thus reflecting the expected efficiency at LHC. With integration over three buckets (3 simulated BCOs), the efficiency increases to 99%. To evaluate the detector as well as the bump bonding efficiency, a 3 BCO integration was used. The uniformity of the response over the whole chip is very good, as shown in Figure 8-37.

The missing hits along the right edge of the plot can be traced to the poor beam illumination of this part of the detector and are not due to inefficiencies.

The **spatial resolution** in the narrow direction (x) has been measured by computing the residuals between the hit position predicted with the silicon strip telescope and that from the pixel detector. The cases of single and double hits have been studied separately. In Figure 8-38 the

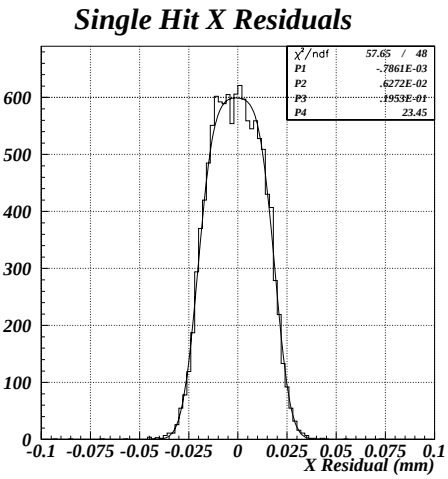

Figure 8-38 Residuals between the track reconstructed by the telescope and the single hits in the pixel plane.

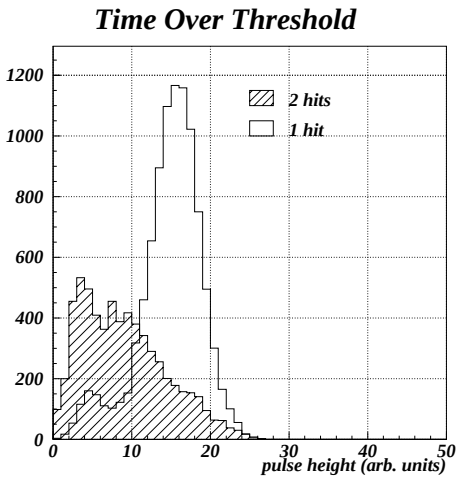

Figure 8-39 Pulse height distributions (measured through the ToT) for single hits and double hits in the pixel plane.

residual distribution for the single hits is shown. The pixel detector and the silicon telescope resolutions have been parametrized with a uniform distribution between L and a Gaussian, respectively. The fitted curve is the convolution of the two resolution functions where the widths, the overall normalization and the mean value have been left as free parameters. We find that the single hit events occur in a region of L = 19.5 µm around the centre of the pixel while the silicon telescope resolution at the pixel plane is 6.3 µm. From studies of the correlation between the

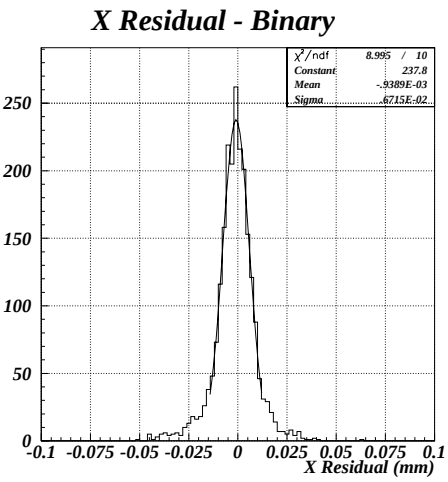

Figure 8-40 Residuals between the track and the cluster center for pixel double hits using the digital algorithm.

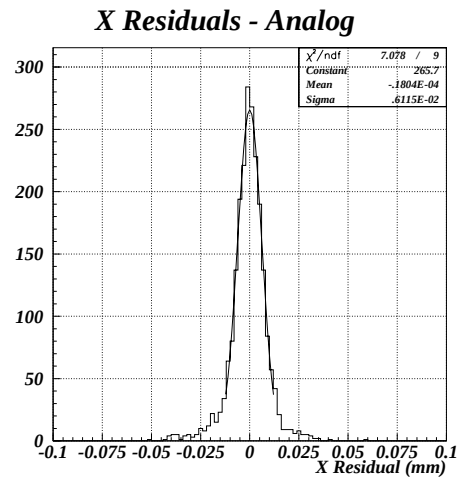

Figure 8-41 Residuals between the track and the cluster center for pixel double hits using the analog algorithm.

charge and the position we find that the double hits are concentrated in a region of 5 µm around the edge between the two pixels (in agreement with what we obtain from the fit to Figure 8-38). The double hit resolution has been studied using both a binary algorithm (measured coordinate taken at the centre of the two hit pixels) and an analog algorithm (position interpolated from the charge collected on the two pixels using the ToT measurements). Figure 8-39 shows the ToT distribution for single hit and double hit events respectively). Figure 8-40 and Figure 8-41 show the residual distributions for the two algorithms. We do not yet completely understand the tails in the distributions. From a Gaussian fit to the central part of the distributions we find resolutions of 6.7 µm and 6.1 µm for the binary and analog algorithms, respectively. For the double hits we expect the residual distributions to be dominated by the silicon telescope resolution: what we measure in the analog case (6.1 µm) is in very good agreement with what we find from the fit to Figure 8-38. The small difference between the analog and binary read-out is as expected from the width of the uniform distribution (5 µm) of the double hits.

Finally, in Figure 8-42, the residual distributions of the single and double hits (treated with the analog algorithm) are shown together. The shapes of the distributions are complicated, and we do not learn much by fitting an adequate parametrization. The r.m.s of the distribution (12.6 µm) includes also the telescope error. Once the latter is subtracted we end up with the **pixel detector resolution** of about 11 µm, in agreement with the assumptions made in Section 3.2.3.

In Chapter 5, **cross-coupling** measurements on the demonstrator chip bonded to a detector have been obtained from lab measurements using various methods (Section 5.11.1.3), with the conclusion that it is about 5% for a tile-2 type sensor. Here we report on an attempt to confront the lab measurements with testbeam data. In Figure 8-43 histograms of double plus triple hit clusters for the long pixel direction (top) and the short pixel direction (bottom) are shown. Cross-coupling nominally produces triple hits symmetric on both sides, while charge sharing, δ - electrons and other physics related effects generally produce double hits. The shape of the histograms clearly displays the contributions from all of these effects. Closer to the pixel boundaries the amount of charge sharing and δ – electrons is enhanced, while in the centre of a pixel it is reduced. In the long (z) direction almost no entries are found in the centre, because charge sharing is non-existent over distances exceeding 50 µm, while the cross coupling via the short pixel sides is also much reduced. We use the bottom histogram to place an upper limit on the fraction of cross-talk hits, ignoring the fact that double hits are most likely not induced by electronic cross-coupling. Taking a region of 5 µm in the centre and normalizing to the total number of hits results in an upper limit of 10%, when scaling to a 300 µm long pixel cell as in the ATLAS pixel sensors. This number then includes cross-coupling as well as contributions from charge sharing, δ electrons and other possible effects. The direct measurement of triple hits is shown in Figure 8-44. The total number of triple hits normalized to the total number of events leads to a hit cross-talk rate of 0.5%

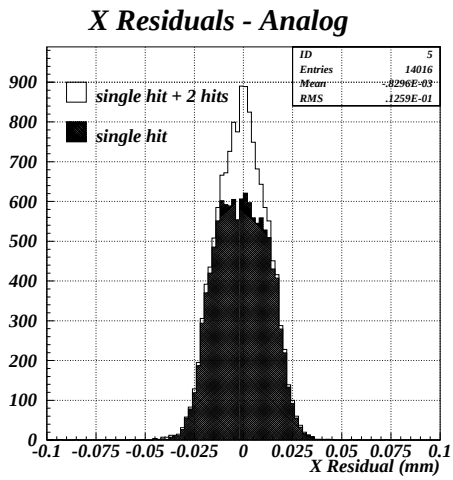

Figure 8-42 Residual distribution between tracks and the centers of the single and of the double hits in the pixel plane.

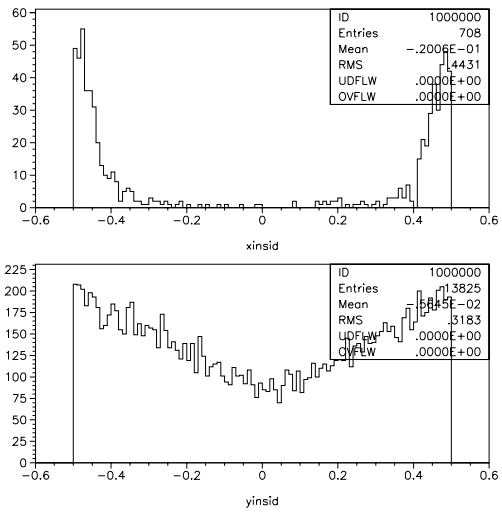

Figure 8-43 Histograms of double and triple hit clusters for the long pixel direction (top) and the short pixel direction (bottom) in fractional cell length units.

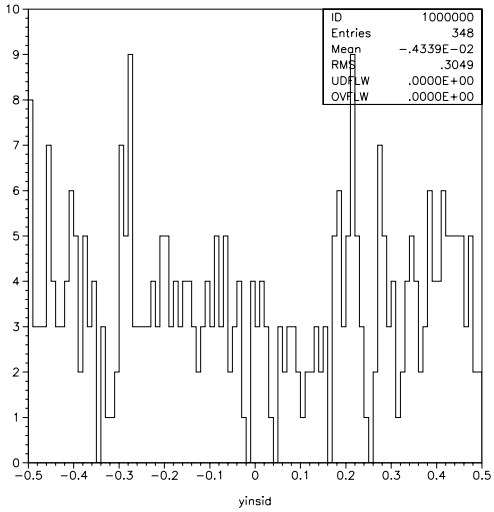

Figure 8-44 Histograms of triple hit clusters for the short pixel direction fractional cell length units.

A 16-chip module, shown in Figure 8-45, has been fabricated and is currently under test in the laboratory. This module has not been produced with fully qualified known-good-dies and can therefore only give partial results on the operation of a 16-chip module. Sixteen chip modules with known-good-dies are currently in fabrication and will be available for tests during the summer of 1998

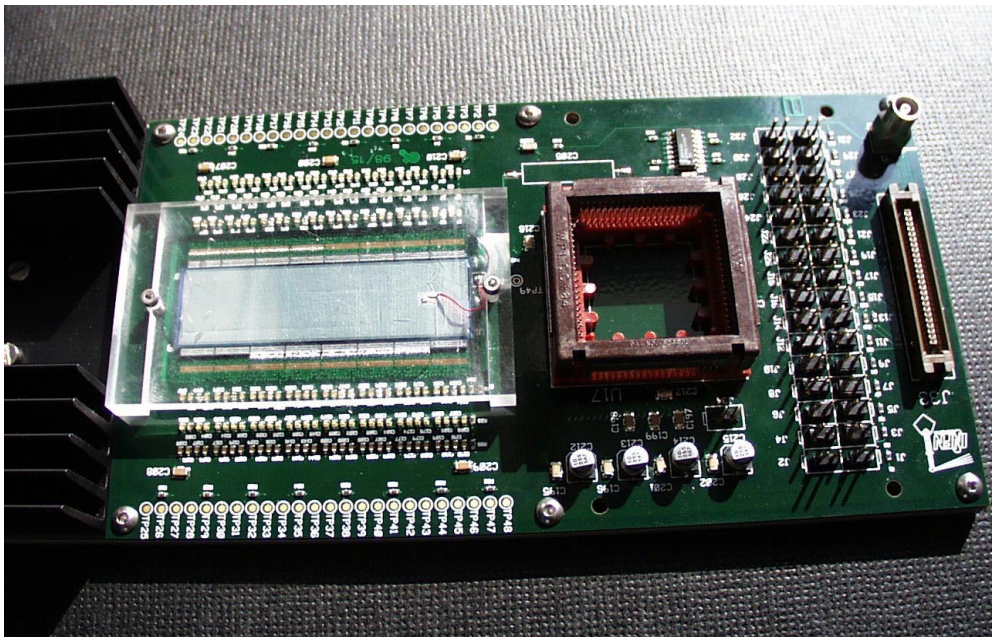

Figure 8-45 Picture of a 16-chip module on the module support card

8.4 References

8-1 http://www.ge.infn.it/ATLAS/Electronics/MCMSpec.ps.