Floorplan, overall layout, global circuit blocks

1 Overall geometry

2 IO Pads and signals

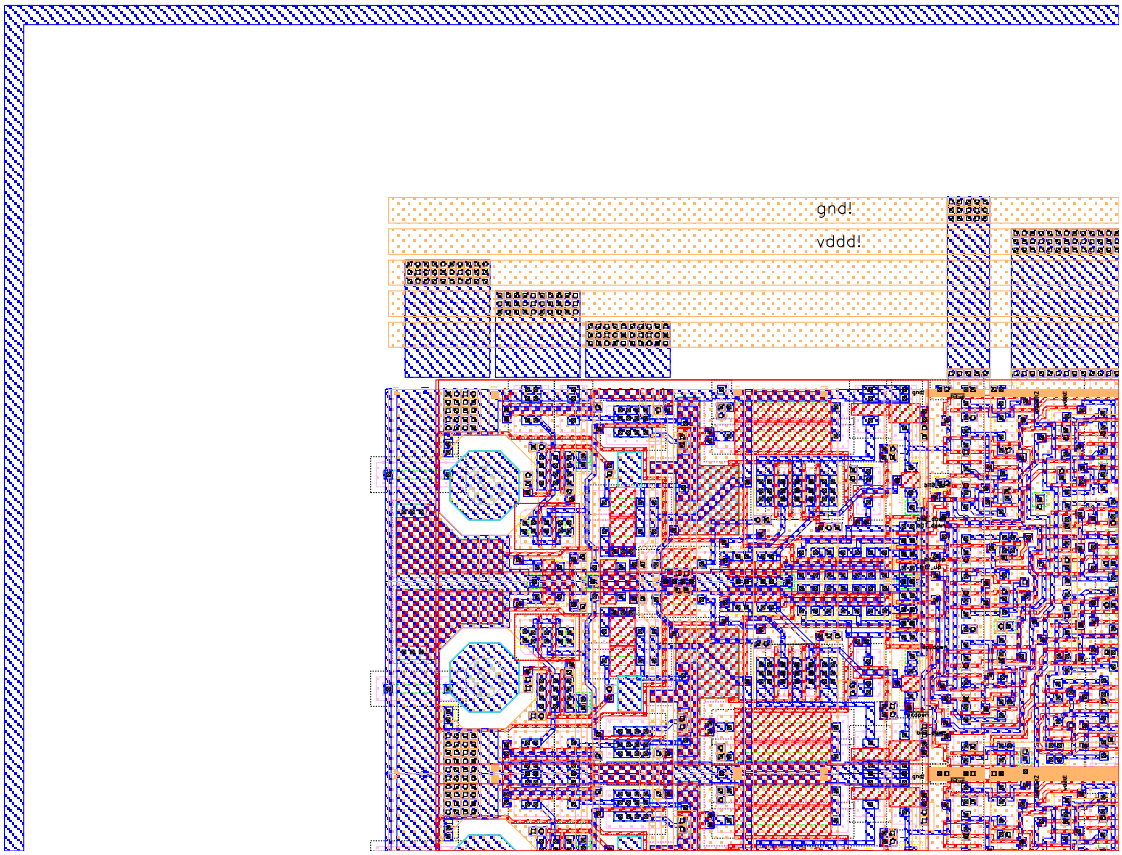
3 Power distribution

4 Circuit blocks

- Command decoder
- Pixel control logic
- Hitbus and column masking
- Current mode DACs
- VTH and VCCD voltage generators
- Charge injection circuit
- Some more blocks are presented in talk of M. Ackers

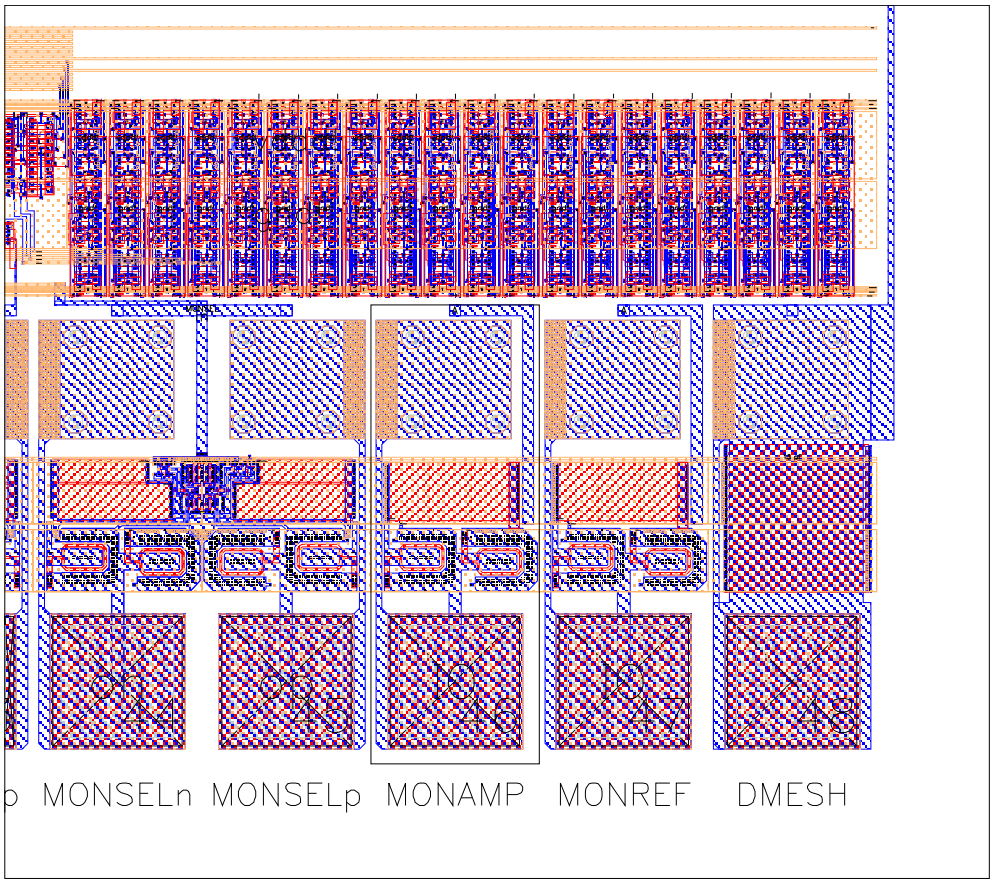
1 Geometry

- Chip size is 7.4 x 11 mm^2 with 18 x 160 pixels of 50 x 400 μm^2
- This chip size leaves a gap of 200 µm between two adjacent chips on the module -> no flipchip problems
- No active components are placed within 100 µm from the scribe line
- The pixels are arranged in 9 ‘column pairs’ with pairs of pixels
- pixels are mirrored horizontally within columnpair
- layout of upper left chip corner:



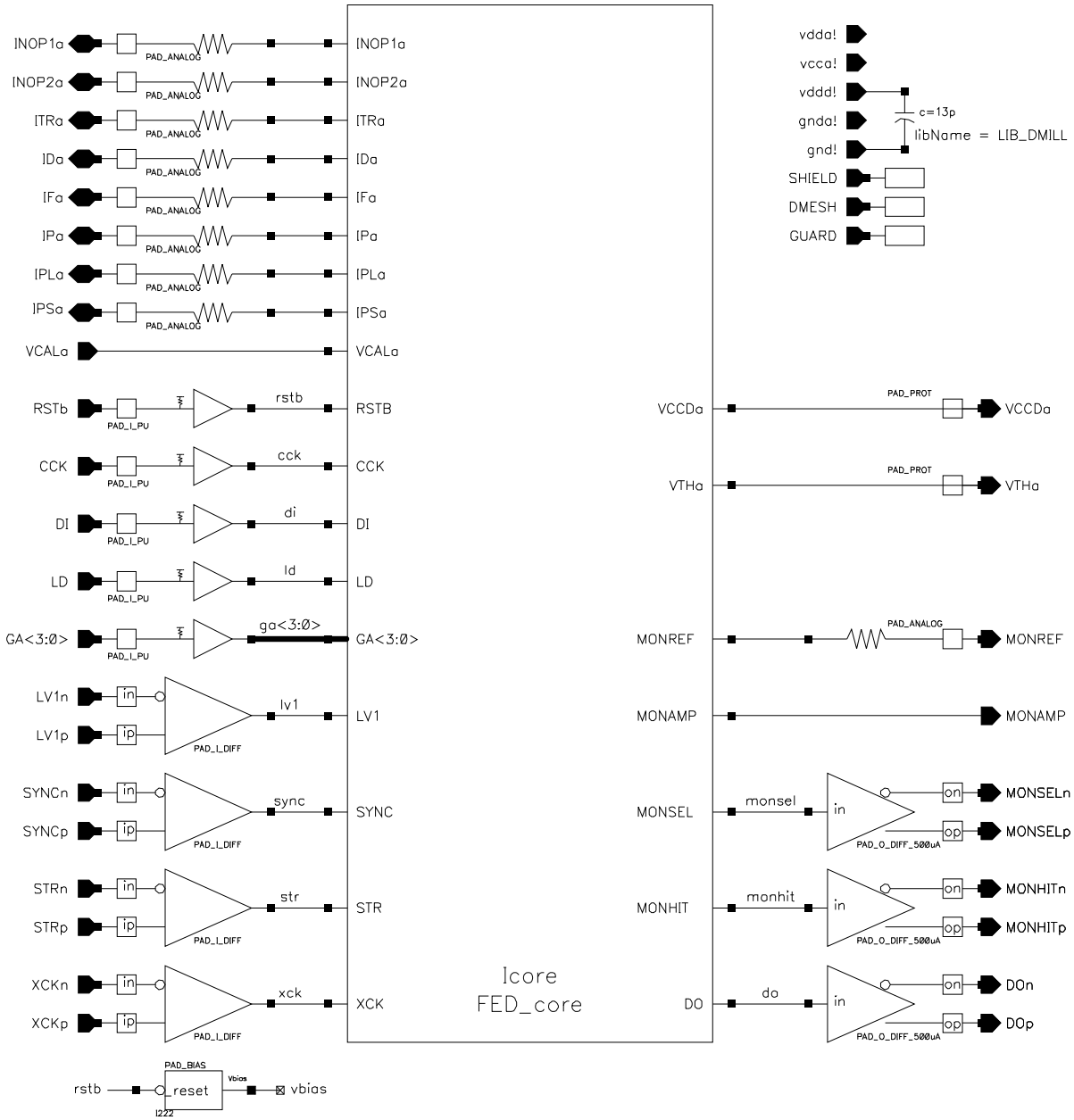
2 IO pads

- All 48 IO pads are located at the bottom with a pitch of 150 µm
- Every IO pad has also 4 bumps in a pitch of 75 µm for use in MCMD assemblies
- layout shows lower right corner of chip:



- All IO pads have protection circuits as recommended by CEA (NMOS diodes to VDDD and GNDD)
- 4 different types of IO pads are used:
  - Analog pad (current bias IOs, reference monitoring)
  - CMOS input with pullup (slow control)
  - ‘LVDS‘ input (40 MHz XCK, LV1, SYNC, STROBE)
  - ‘LVDS’ output with 500uA output current (Data out, Hitbus)

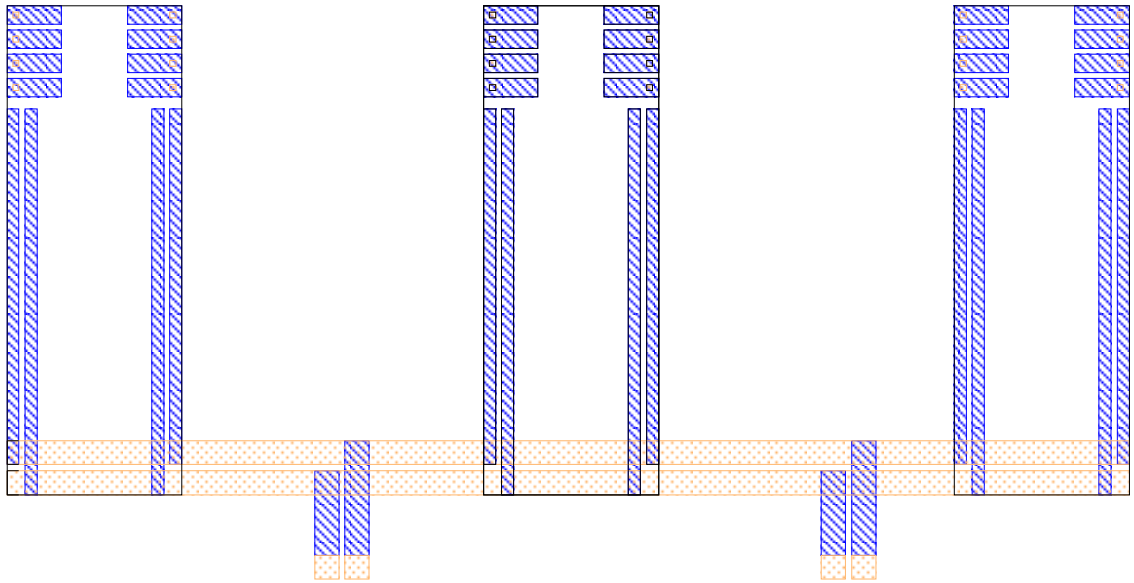
Chip pins



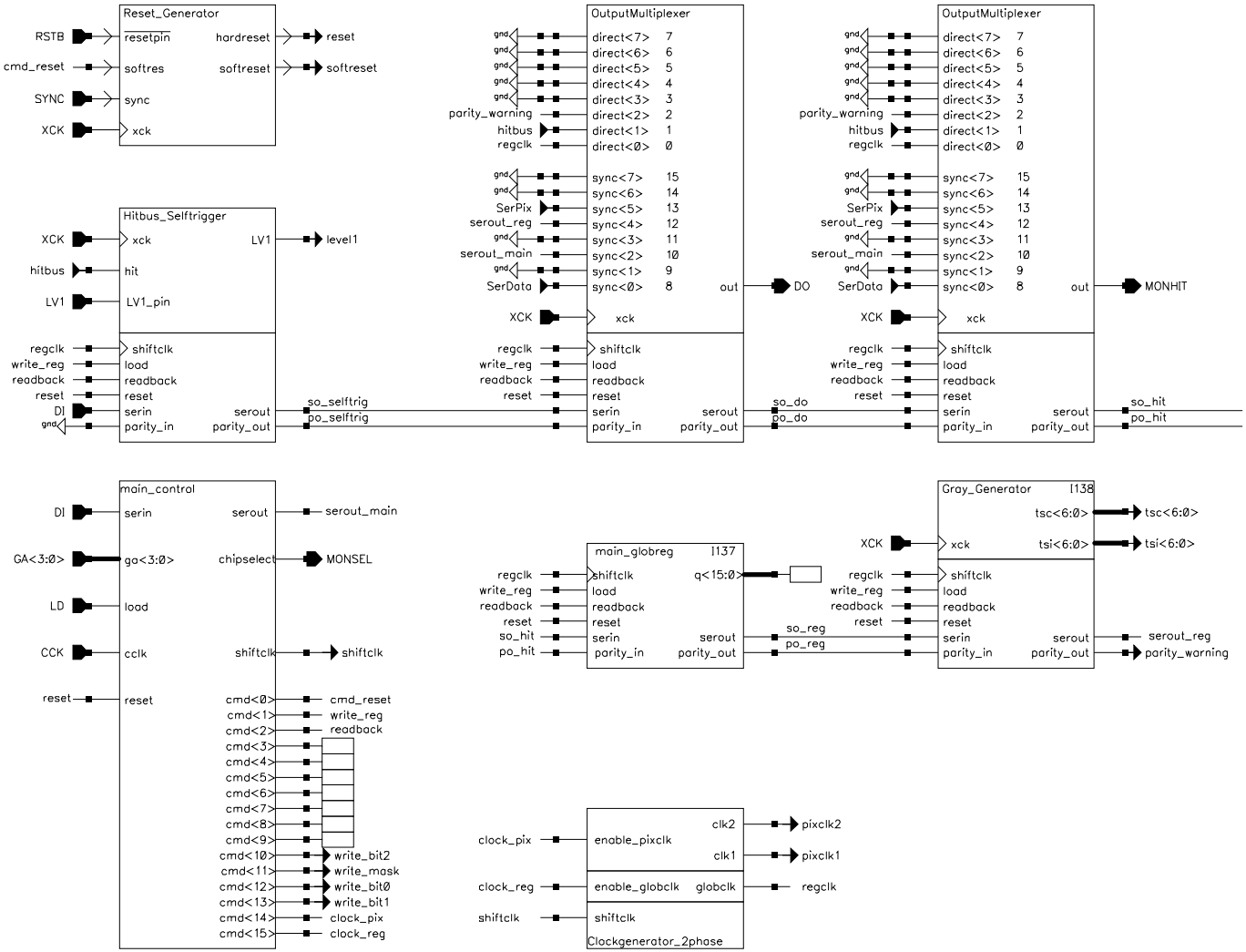
- All chip pins are shown here
- The 5 global supplies have 2 pins each
- Many of these pins are for chip testing and are not connected on the pixel module
- 20 Signals should be enough needed in final module

3 Power distribution

- Chip has 5 power supplies:
  - Digital VDD (vddd! = 3V), Digital Ground (gnd!)
  - Analog VDD (vdda! = 3V), VCC (vcca! = 1.5V), Analog Ground (gnda!)
- Every supply has 2 bond pads at 1/4 and 3/4 of chip to minimize IR - drops in horizontal busses
- Horizontal bus uses M2 (lower sheet resistance)
- Vertical bus uses M1 and M2 up to pixels, M2 (M1) in pixel matrix ->
  - Analog supply voltage drop in pixel matrix =15 mV (increasing drop for top pixels)
  - Voltage drop in vertical bus = 10 mV (same for all pixels)
  - Voltage drop in horizontal bus < 5 mV (most for outer columns)



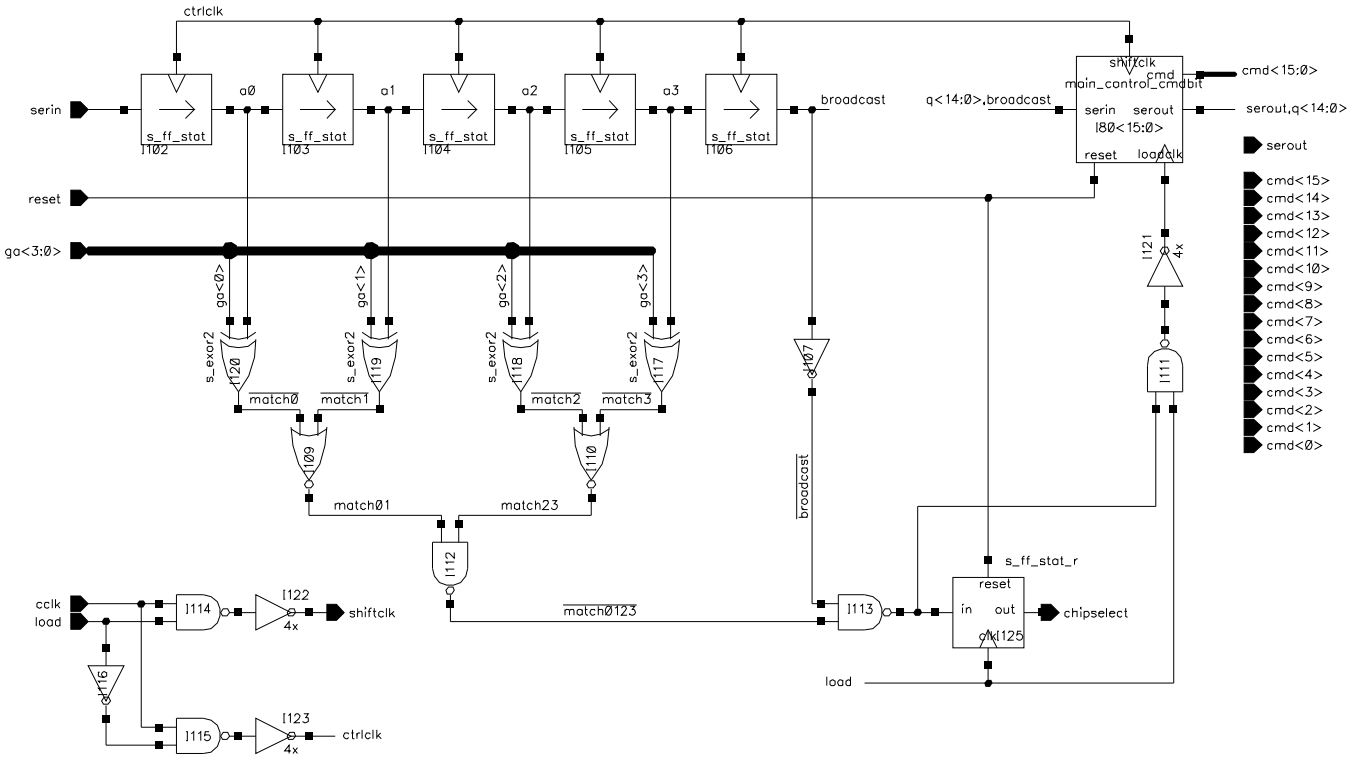
Main command schematics



4 Global command structures

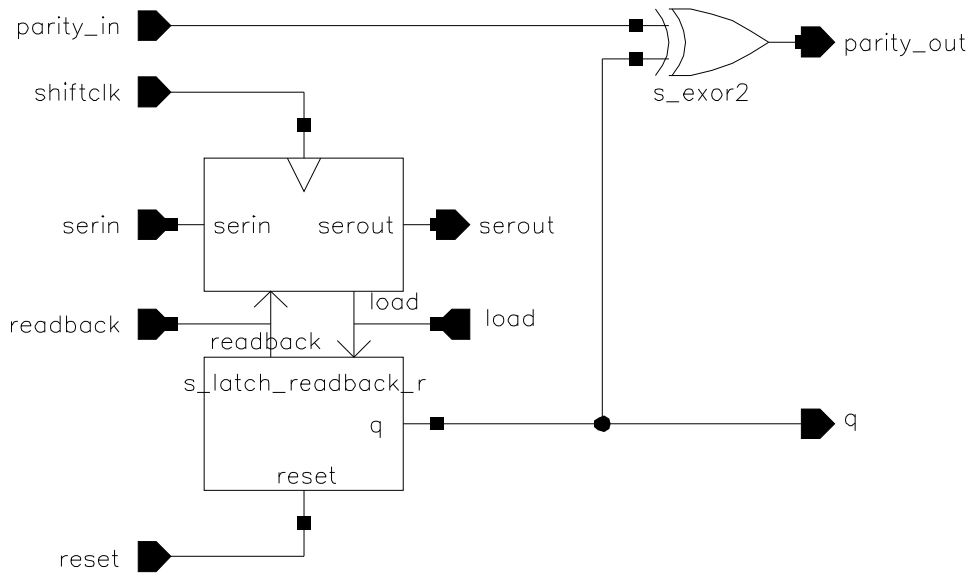
- Command decoder receives slow control commands and passes data to registers and pixel matrix
- global register chain contains control bits, latency, DAC values, selects output MUXes etc.
- All global register bits have a parity check bit which is sent in the serial data stream as a parity warning
- Resets can be generated by reset pin, soft reset or by a long SYNC signal (eliminate reset pin...)
- Level 1 trigger can be auto-generated (selftrigger) from Hitbus signal
- The signals passed to the output of the chip can be selected with MUXes. Standard settings are serial data and hitbus, many other signals can be accessed for debugging.

Schematic of command decoder



- Command bits are sent serially through DI when LD = 0
- One broadcast bit is sent, 4 Address bits are sent
- LD is pulled high -> Address is compared to geographical chip address and command is transferred to registers is chip is selected or broadcast is sent
- Data can be sent as long as LD is high

One bit of global register chain



global register bit with parity bit

- This circuit is used to store DAC values, latency, control bits etc.
- Data is first written in a shift register and transferred to the storage latch wit a seperate command. No ‘junk’ values are therefore present in the register
- All register bits are chained with XORs to generate a parity bit to detect bit flips (SEU). The parity bit is included in the serial data stream as an error bit

Pixel control logic

1 Purpose, specification

- logic in every pixel to control injection, masking and 3 tune bits (5 bits total)
- provide fast OR of pixel hits by pulling low vertical ‘hitbus’
- use Metal 2 for shielding -> layout must be done in Metal 1 only

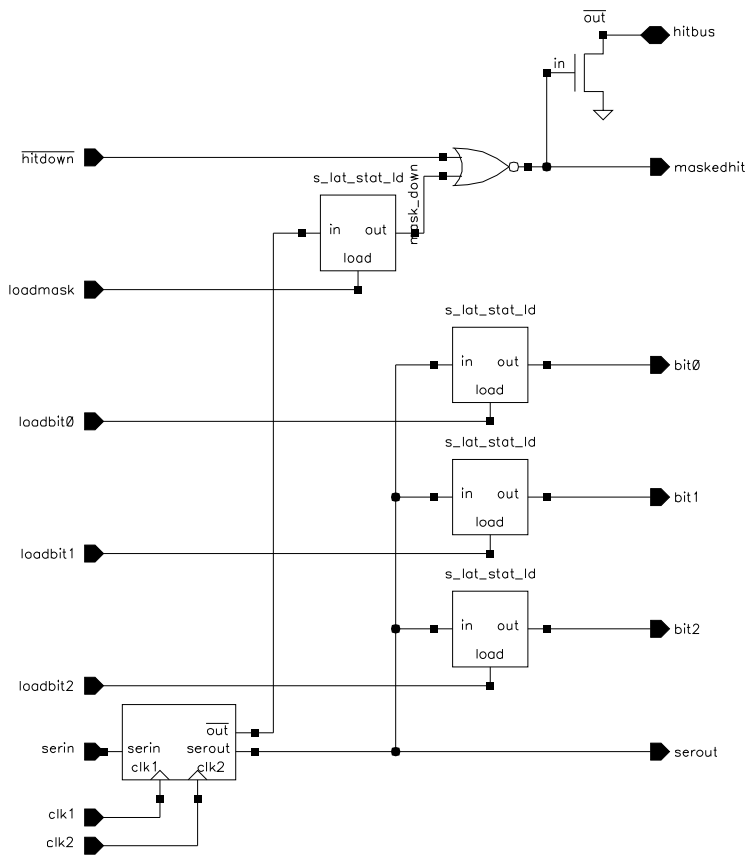
2 Implementation

- use conservative two phase shift register chain to select pixel
- use 4 static latches to load mask bit and 3 tune bits
- use annular NMOS with low C_{gd} to pull down hitbus

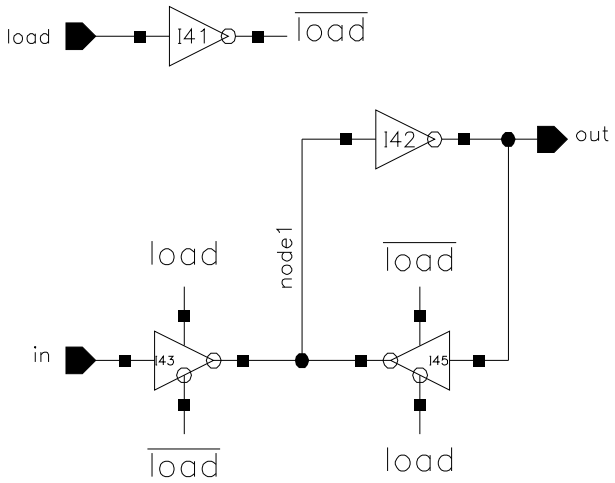
3 Performance

- identical schematic works in FEA and FEC

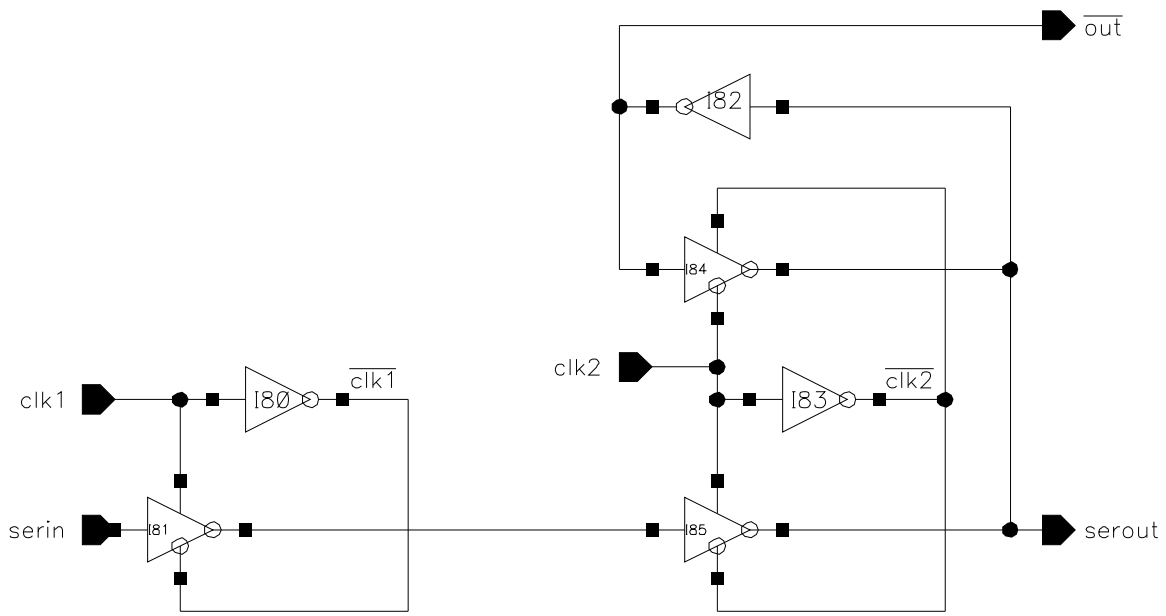
Schematic of pixel control section:



Latch in pixel control section:



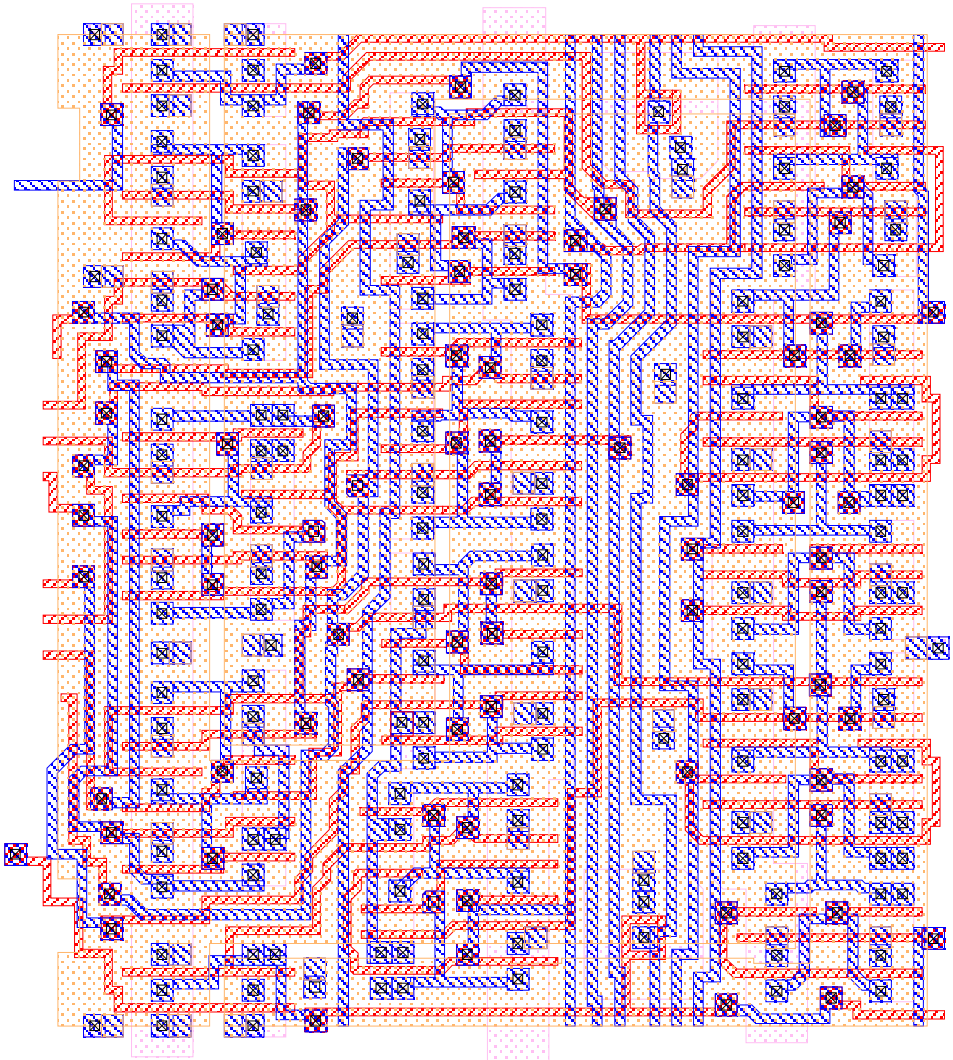
Shift register in pixel control section:



Control Shiftregister in Pixel (2 phase)
(in static mode if clk1 = 1 and clk2 = Ø)

- uncomplete first stage to save area -> register is dynamic during half clock period. Clock speed is 5 MHz. The two phase clock generator guarantees that the static position is default.
- inverse clocks are generated in pixel to reduce bussing

Layout of control section for 2 pixels



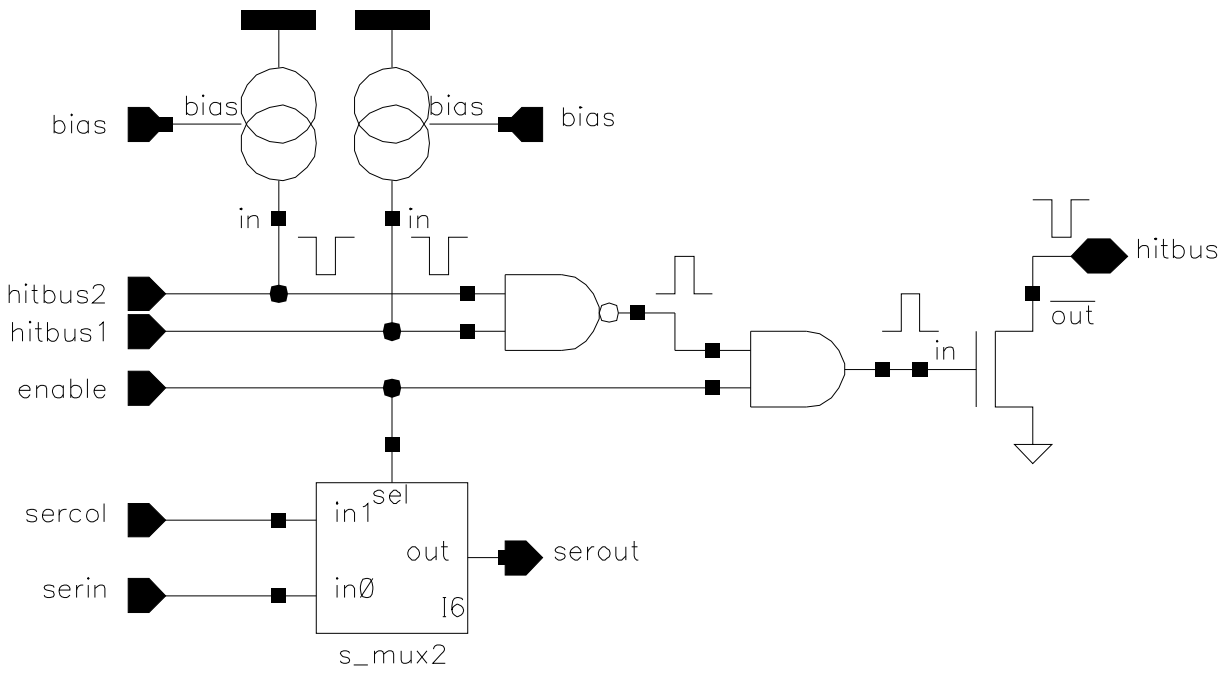
- height: 100 µm, width: 90 µm
- metal 2 is used only for supplies
- 10 lines go to analog part (left): 2 x (hit_in, inject, trim<2:0>)
- 2 lines to readout part (right): (2 x hit_out)
- anular NMOS is used for hitbus

Hitbus and column masking

1 Purpose, specification

- regenerate signal of vertical hitbus in every column and pass signal to horizontal hitbus (reduce capacitive load of net)
- provide possibility to switch off hitbus in columnpair (in case it is stuck in that pair)
- provide possibility to bypass to control shift register in the columnpair (in case it is interupted)
- Use same enable signal for both functions and use this signal also to remove this columnpair form data readout

2 Circuit realization



3 Verification

- circuit is checked in global simulation

Current mode DACs

1 Purpose, specifications

- Supply biasing currents for preamplifier, discriminator, trim DAC and Injection chopper
- 7 DACs are needed
- Required precision is >= 7 bit (default current / 16 -> 8 x Default current) for bias DACs, 8 bit for injection DAC. This allows 25e injection step @ 6400e full scale or 250e steps @ 3 mip full scale
- Aim for good integral linearity to avoid calibration errors @ injection
- Radhard design requires current source transistors to be always on
- No detailed matching data of irradiated transistors available
- Space is available under analog / digital M2 power busses at bottom of column -> use only M1

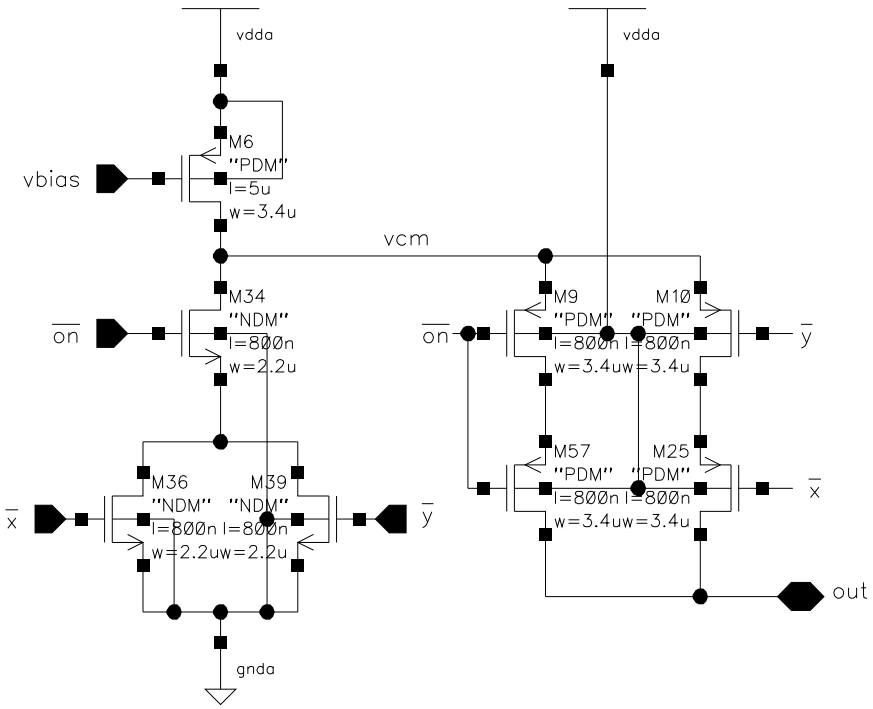
2 Inplementation

- Use individually switched current sources for 6 MSBs, use scaled transistors for 2 LSBs
- Make sure V_{ds} of current source transistors is stable (independant of load) -> ‘cascode’
- Size current source transistors for 8 bit precision (using ‘typical’ matching data) -> A < 20 μm^2
- Unit cell layout is 20 µm x 30 µm, block of 8x8 cells is 160 µm x 240 µm + control + LSB + Regs

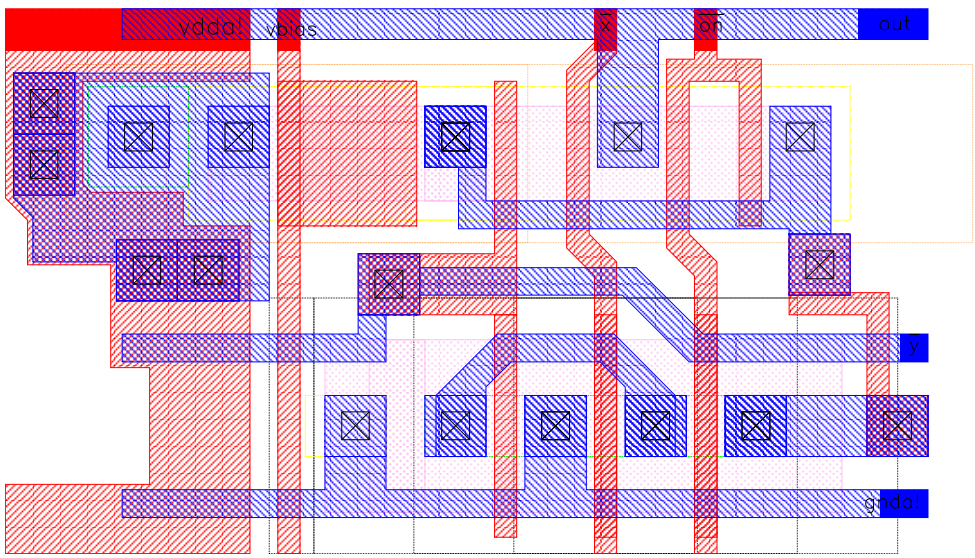
3 Performance

- Simulation shows no systematic effect for MSBs, 10% error on LSB

Schematic of one bit cell

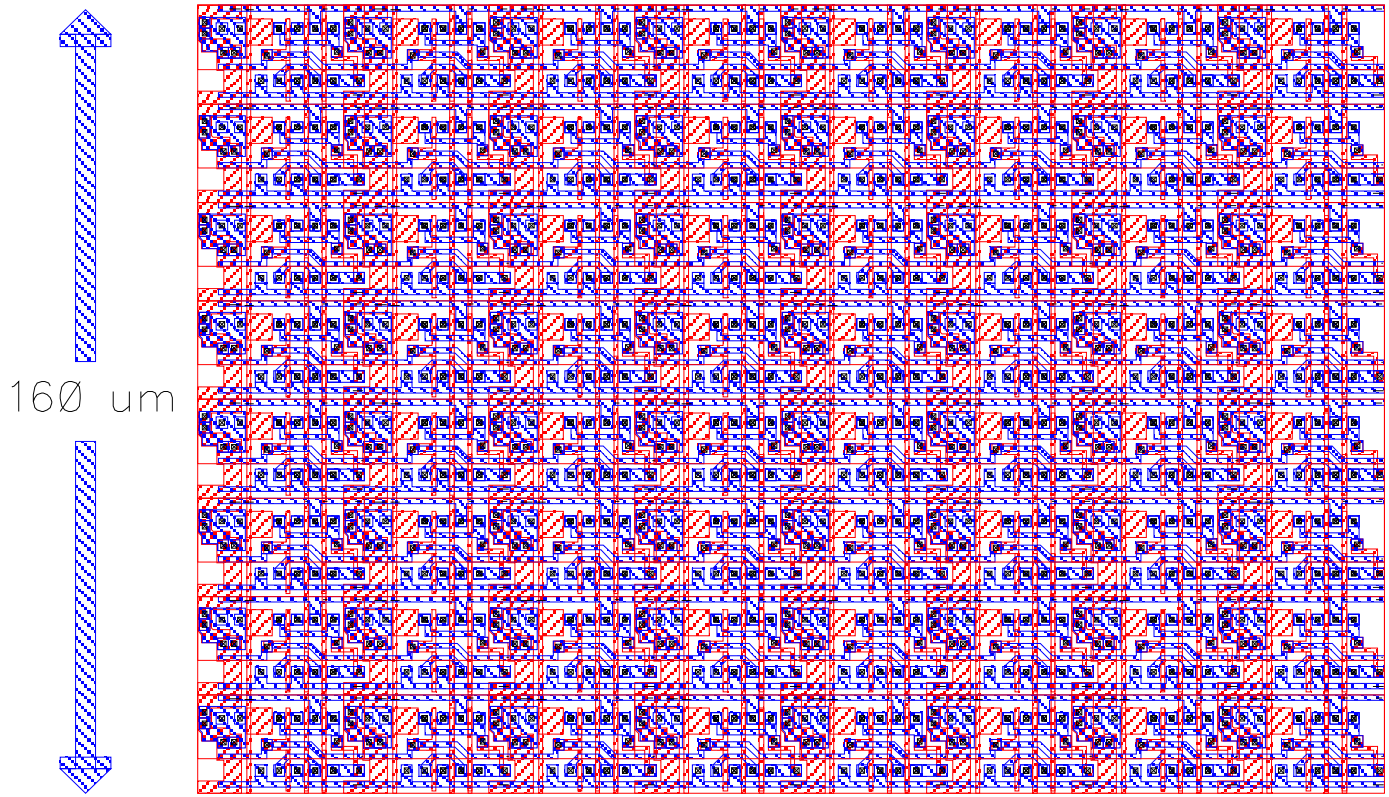


Layout of one bit cell

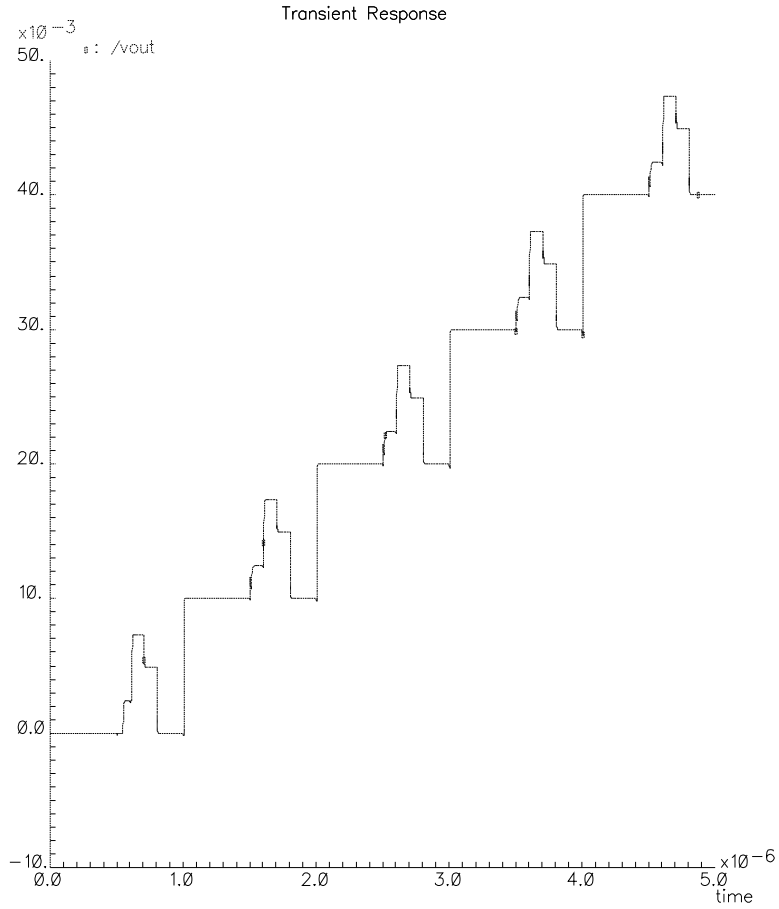


- uses only metal 1
- size is 20 µm x 30 µm

Layout of bit matrix



Simulation result using 4 bit cells and 2 LSBs (0-1-3-2)



- No systematic effect for MSBs (2 µV for10 mV steps)
- 10 % systematic effect on LSBs (transistor models ?)

VCCD & VTH voltage generators

1 Purpose, specification

- generate 2 programmable voltages (vth, vccd) to control bias points in discriminator
- Only one buffer of each type required on chip
- current required is up to 5 mA for worst case threshold settings
- voltage ranges are 0.5V -1.9V and 1V - 2V in 16 - 32 steps

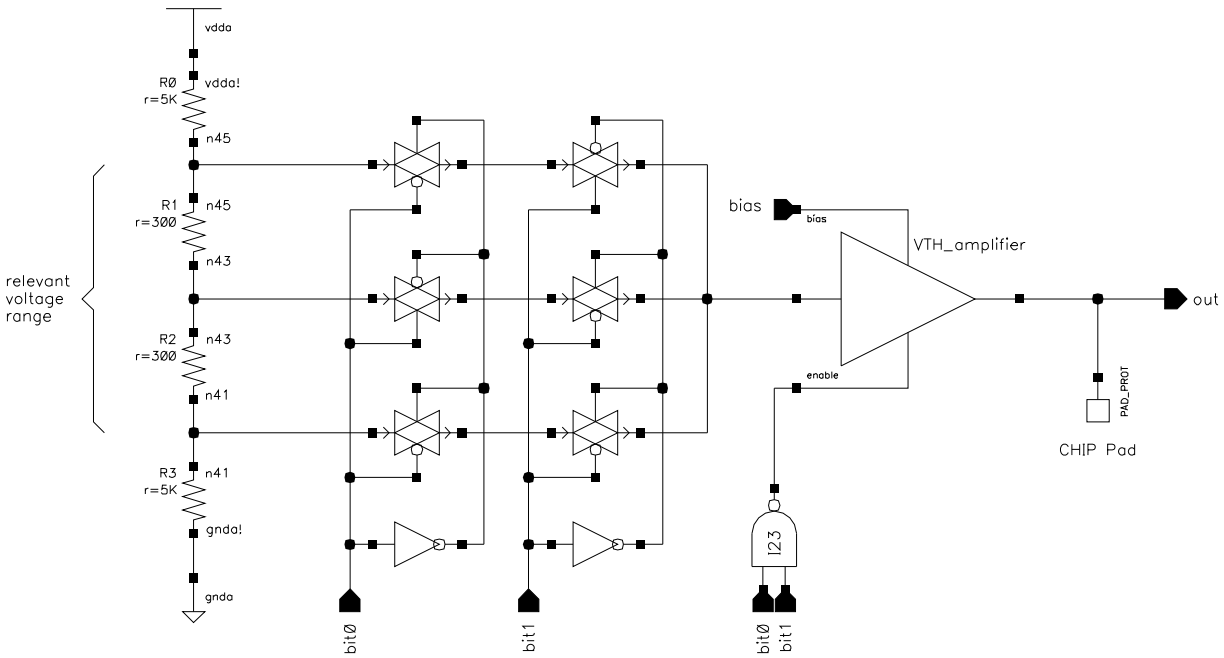
2 Implementation

- Use resistor string to provide possible voltage
- Use pass transistors to select one of the voltages
- Use 4 (5) register bits to control switches
- Analog buffer can go close to rails and supply required current (see L. Blanquart)
- Voltage is available on chip pin for monitoring
- Buffer can be disabled and voltage supplied externally

3 Performance

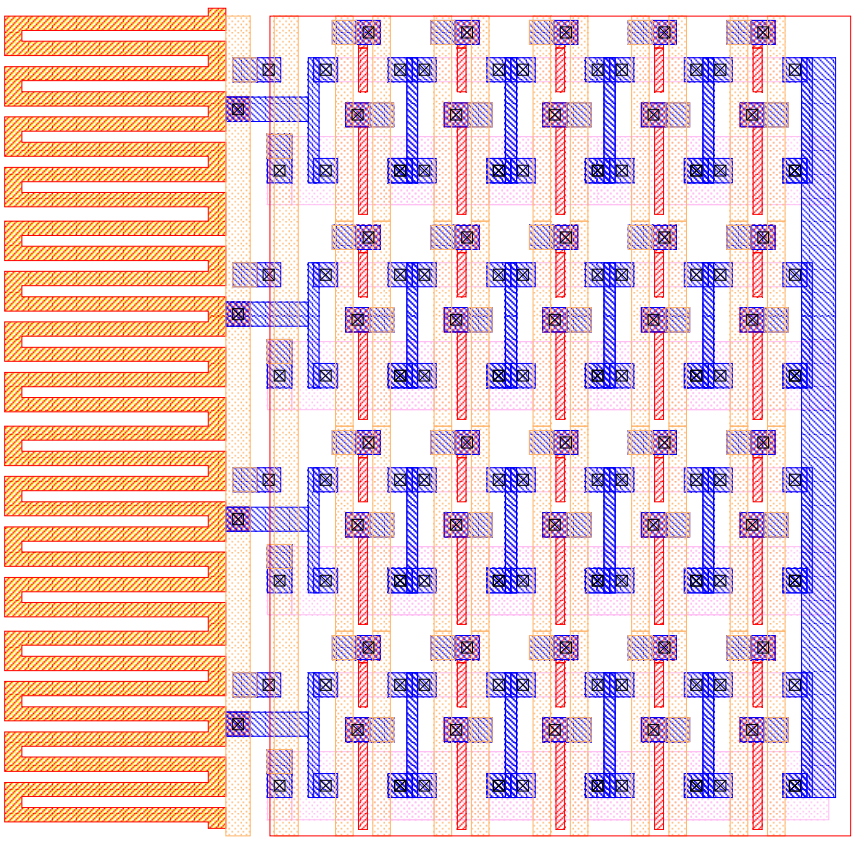
- See L. Blanquart

Principle of voltage generation

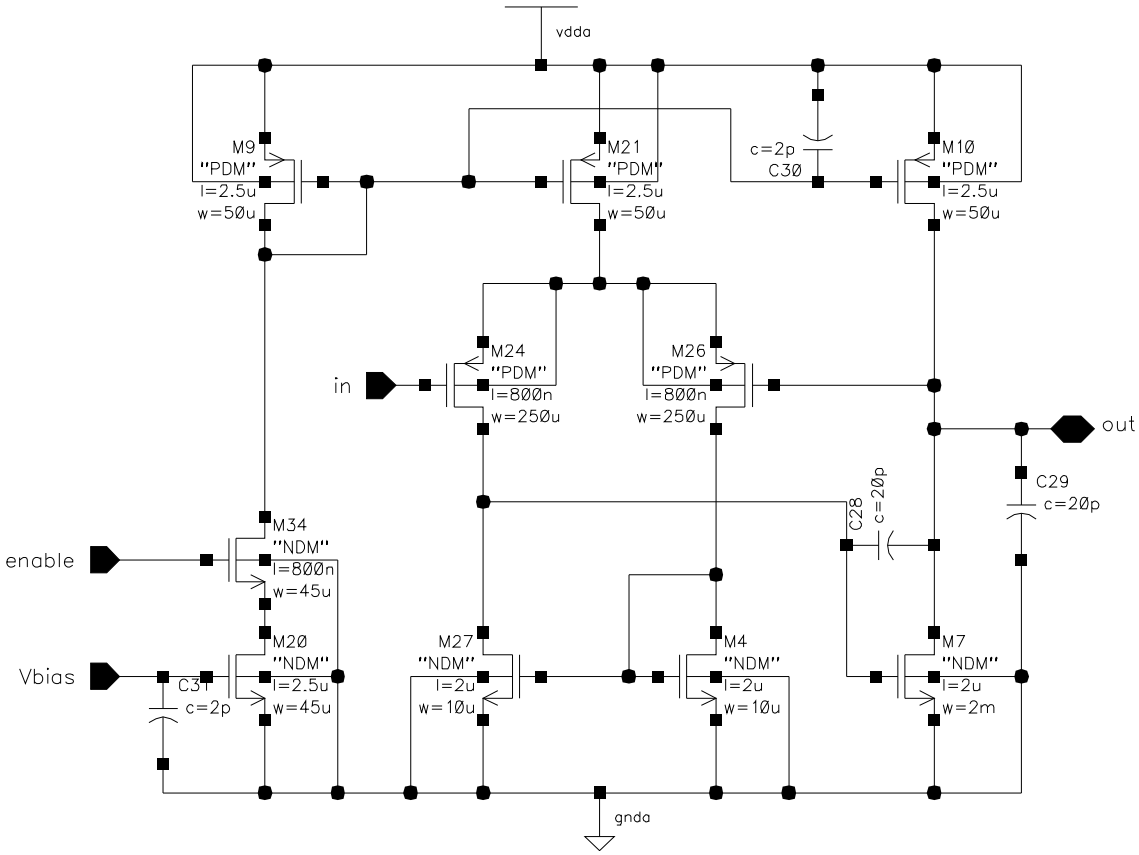


- Output voltage is referenced to analog supply

Layout of resistor string and pass gates



Schematic of analog buffer



- Output can swing close to ground, circuit sinks current
- buffer can be disabled to supply voltage externally

Charge injection circuit

1 Purpose, requirements

- Provide negative voltage step on VCAL line to inject charge into preamplifier via 10 fF injection capacitors (M1-M2 under bump pad)
- Range should be 0 ... 1 fC = 0 ... 6300 e = 0 ... 0.1 V in 256 steps of 25 e for standard threshold measurements and noise scans
- A second range of 0 ... 10 fC = 0 ... 3 mip = 0 ... 1 V allows generation of mip signals and above (crosstalk studies etc.)
- Must be able to operate in stand alone mode (internal circuit) OR using external voltage VCAL (as a backup solution and to cross check)
- Injection step must not change with supply voltage and after irradiation

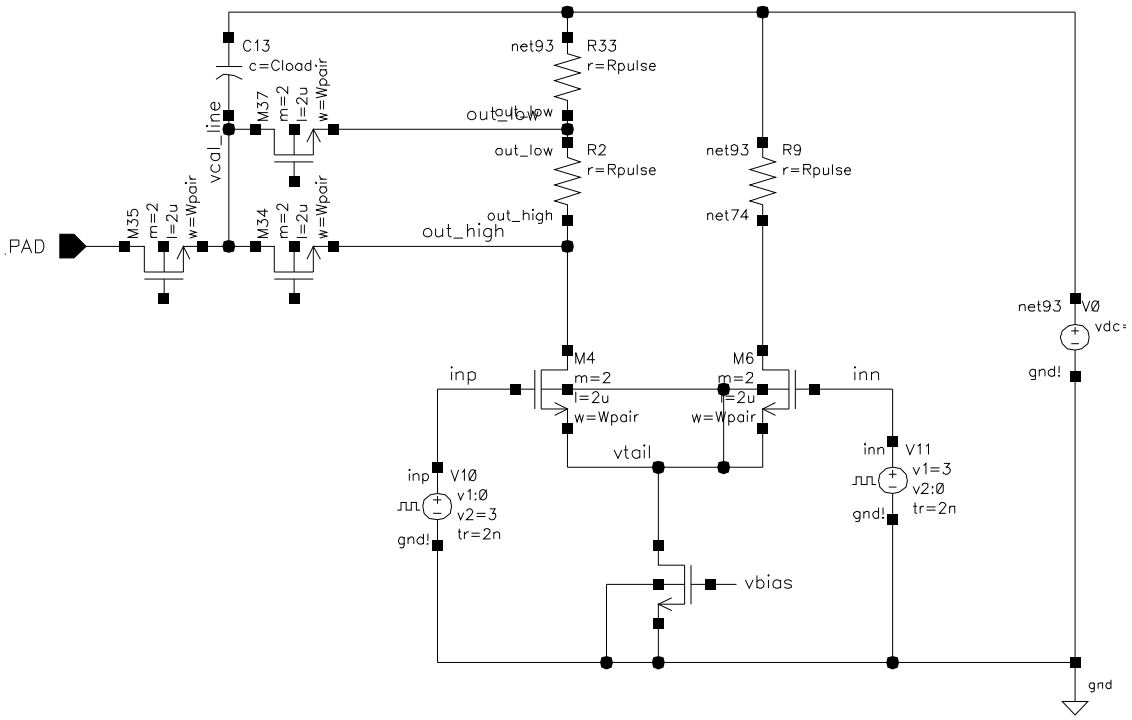
2 Circuit realization

- Use current switched with differential pair into resistive load (-> $\Delta U \sim R_{load} \times I$)
- Current is generated in V_{BE} reference ($I \sim R_{ref}^{-1}$)
- -> ΔU depends only on ratio R_{load} / R_{ref} . Same types of resistors (Poly) are used.

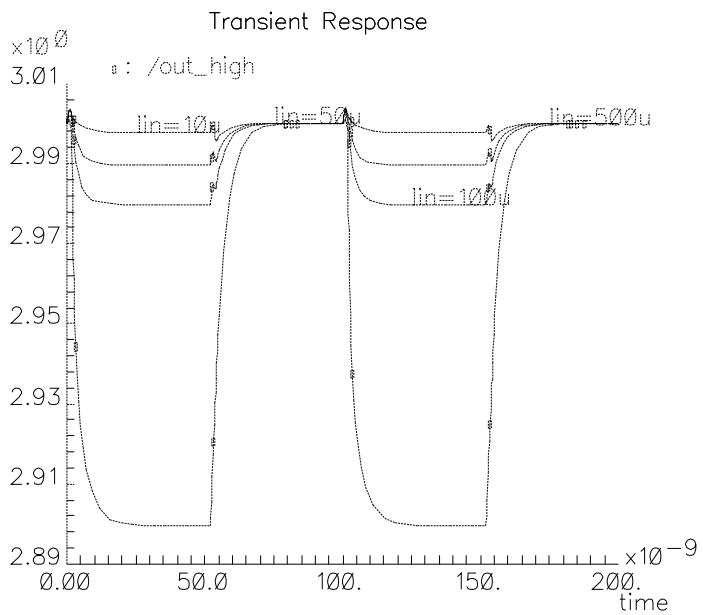
3 Performance

- Still under study
- Insensitivity to absolute value of Rs has been verified

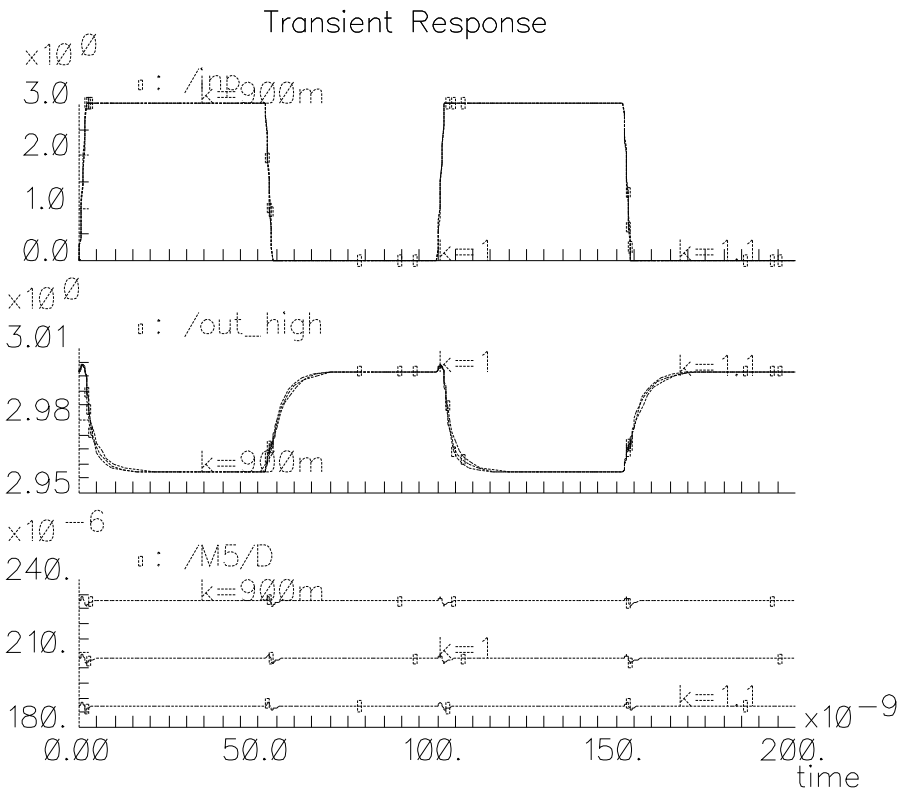
Schematic of injection circuit



Voltage output for various currents



Variation of absolut values of resistors in injection and reference:



Status

- Most global control blocks are ready: Schematics are simulated and layout is done
- ‘Rail’ system ist used to easily rearrange blocks in final floorplan
- Floorplanning is done and layout pieces are filled in.
- Macro LVS simplifies verification in final layout phase (see talk G. Comes)
- Some blocks still need layout (Hitbus, DAC, VTH & VCCD generators, ...)
- Injection circuit still needs analog simulation

- For Verilog simulation strategy and results see talk of M. Ackers