Introduction and Overview for FE-D Design Review

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Overview of system specifications and design of module

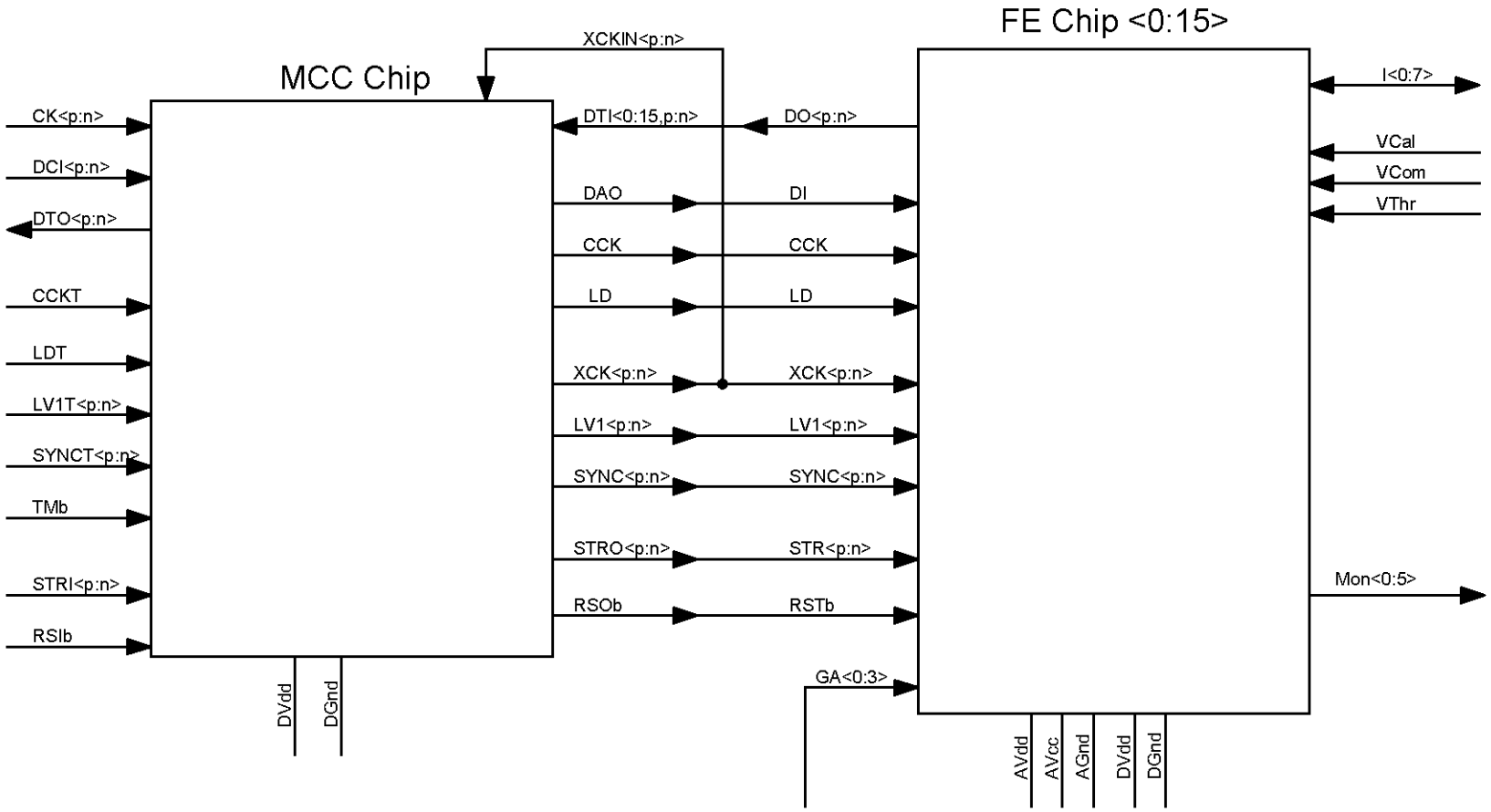
Summary of previous submissions and relevant results

Overview of FE-D specifications and design at the top level

Introduction to verification issues: SPICE models

System Design of Pixel Module

First requirements analysis and discussions led to module system design in 96:



- Two chip design, including a single controller and event-builder chip (MCC) and 16 front-end chips bumped to a single silicon substrate.

Features:

- Basic interface to the outside uses a 3-wire protocol (SerialIn, SerialOut, XCK), which maps onto the SCT opto-link protocol
- Provide a “transparent mode” interface through MCC to FE chips for simplified testing.
- Basic interconnections between FE and MCC use bussed signals. Slow control will not operate when recording events, so it uses full-swing CMOS. All fast signals use low-swing differential “LVDS-like” signaling. Point-point signals use 0.5 mA drivers (FE chips only), external or bussed signals use 3 mA drivers.
- To provide enhanced speed and robust module design, the serial output lines are connected from the FE to the MCC in a star topology (16 parallel inputs on MCC).
- Only analog signal between MCC and FE at this time is VCal calibration signal. All FE chips have internal current references and adjustment DACs to control analog operating points.
- Architecture is “data-push” style: each crossing for which LV1 accept is present causes all FE chips to autonomously transmit back hit information for the given crossing. LV1 signal may remain set for many contiguous crossings to allow readout of longer time intervals. MCC merges such events together.
- Synchronization signal available to ensure FE chips label LV1 properly.
- System uses two analog supplies to reduce power dissipation.

Requirements Summary

Power budget:

- Total for module is based on 0.6W/cm^2 power density, including all power dissipation in services within the pixel tracker volume. This includes MCC and FE chips, sensor leakage, opto-link, and power transmission.
- Within this budget, MCC is allocated roughly 300 mW, and each FE chip roughly 250 mW (150mW analog, 100mW digital). The analog budget is further specified to be 40μW/pixel

Geometry:

- The active die area for the FE chip is 7.2 x 10.8 mm, of which 7.2 x 8.0mm is sensitive area for particle detection. The sensitive area of the FE chips must extend to the edge of the die along 3 sides, with all additional logic and I/O concentrated on the remaining side.
- Physics studies indicate that the pixels should be as narrow as possible in one dimension, and a 50μ pitch has been chosen as reasonably achievable. In the long direction, adequate resolution is obtained with a dimension of 300μ - 400μ. The present prototyping program has frozen the length at 400μ.

Demonstrator Program

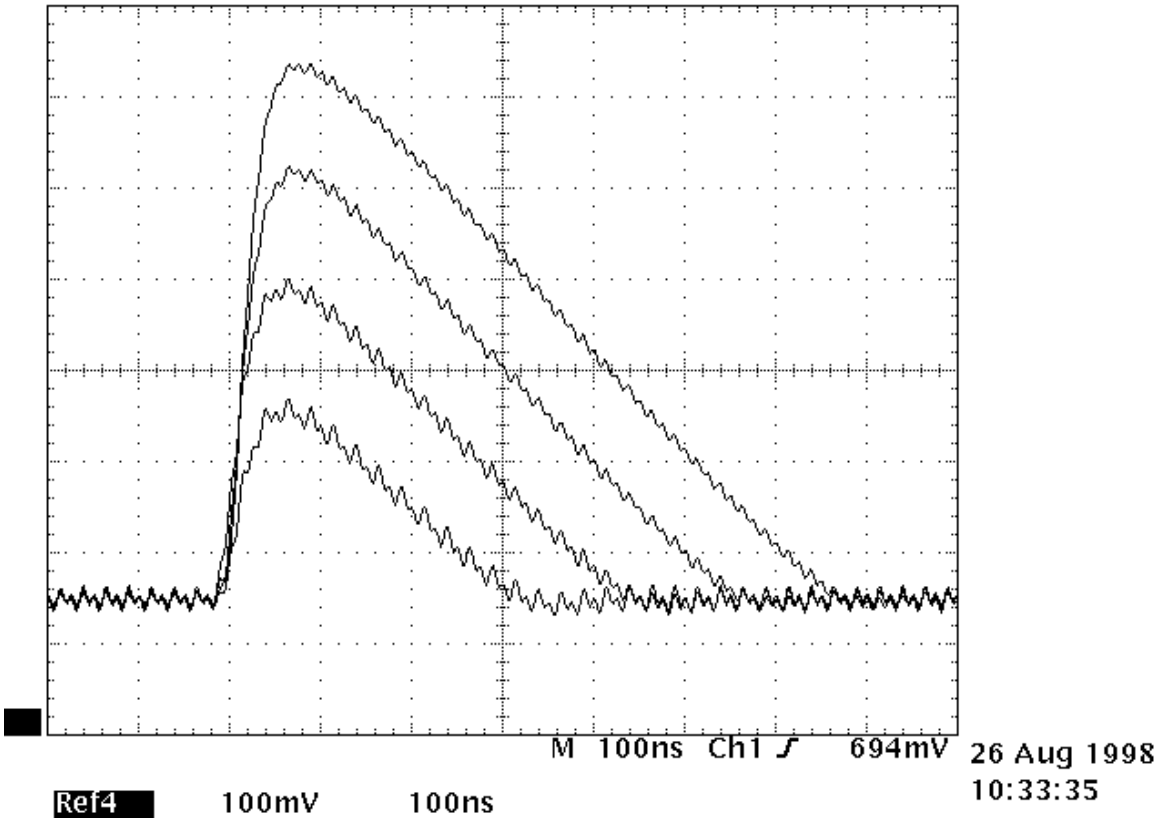
- In 1997, we agreed on overall design specifications for the FE and MCC chips necessary to implement this module design in a prototype form. We decided to pursue two prototypes for the FE chip. This was based partly on history and partly on the goal of submitting designs to two rad-hard vendors.
- One was called FE-A, and was designed for submission to AMS 0.8μ BiCMOS. This process was viewed as a prototype vehicle for DMILL. The chip was submitted in Oct. 97, and testing began in Jan. 98. A second, purely CMOS version, FE-C, was submitted in May 98. This chip has 880K transistors.
- The second was referred to as FE-B, and was designed for submission to HP 0.8μ CMOS. This process was viewed as a prototype vehicle for Honeywell. This chip was submitted in Feb. 98, and testing began in Apr. 98. This chip has about 850K transistors.
- A DMILL prototype matrix (no EOC, simple readout) called MAREBO was also submitted in Jul 97 and tested in Jan 98, to verify the FE design in DMILL.
- The MCC was submitted in May 98, along with the FE-C, and returned in late summer. FE-C chips were tested and bonded for evaluation in Sept. testbeams.
- All of these chips contain minor errors, but in all cases their functionality was quite close to the submission goals. Extensive lab testing and testbeam studies have been carried out on all chips. Excellent performance has been achieved.

Demonstrator FE Chip Geometry

- Agreement on pixel size was struck in Sept 96, in order to allow compatible, parallel detector and electronics development.
- The geometry adopted was 50μ x 400μ for the pixel size, with pixels arranged in 18 columns of 160 pixels per column.
- The geometry was mirrored between columns, so that the inputs for pixels in column 0 and 17 are on the outside, and all other columns are paired.
- The input pad geometry in the inner column pairs is then a double row of 50μ pitch pads. The metal pad is specified to be 20μ square, with a 12μ opening in the passivation for the bump-bonding.
- The cut die size must not extend beyond 100μ from the edge of the active area on three sides of the die. Hence, nothing outside of the pixel circuitry is allowed on three sides of the chip, to allow module construction.
- The bottom of the chip (all peripheral logic and I/O pads) are allowed 2800μ, making the total active die region 7.2mm x 10.8mm.
- An I/O pad structure of 48 pads, each consisting of a 75μ x 75μ wire-bond pad, and a group of 4 bump-bond pads, was frozen.

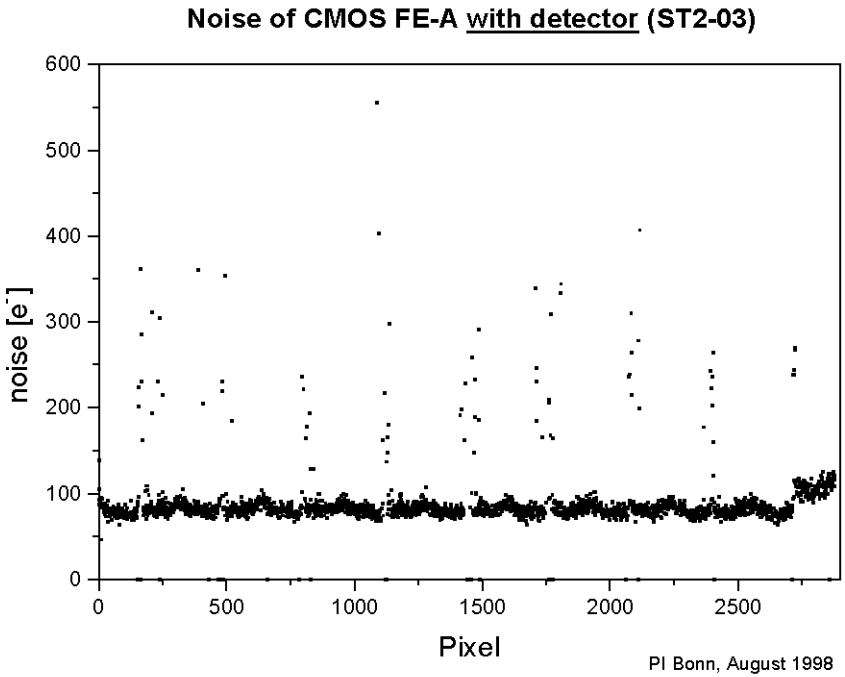
Some highlights of the performance of the present chips

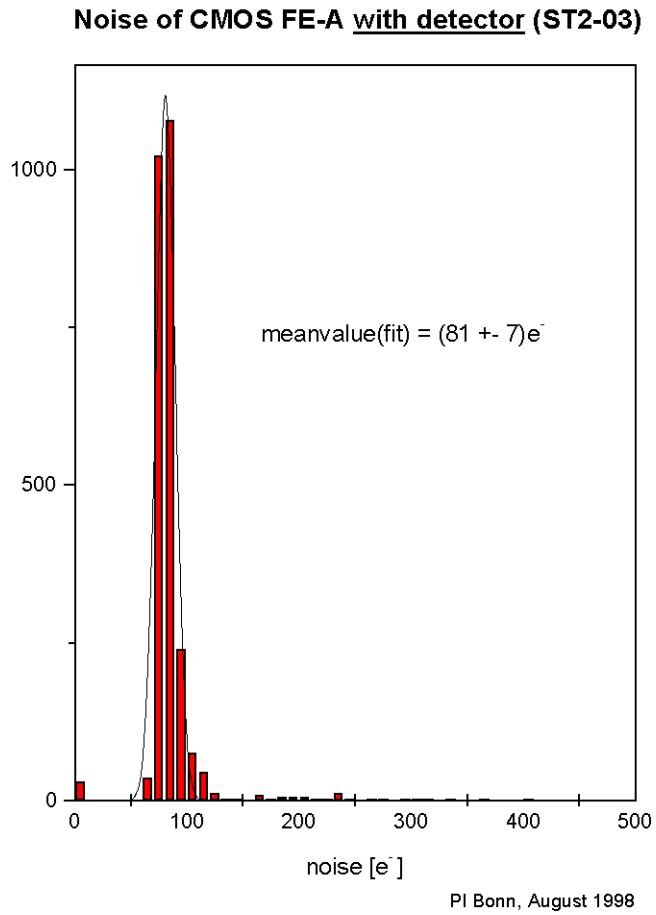
- Basic performance of FE-C:



- Preamp output, showing TOT behavior and linear return to baseline.

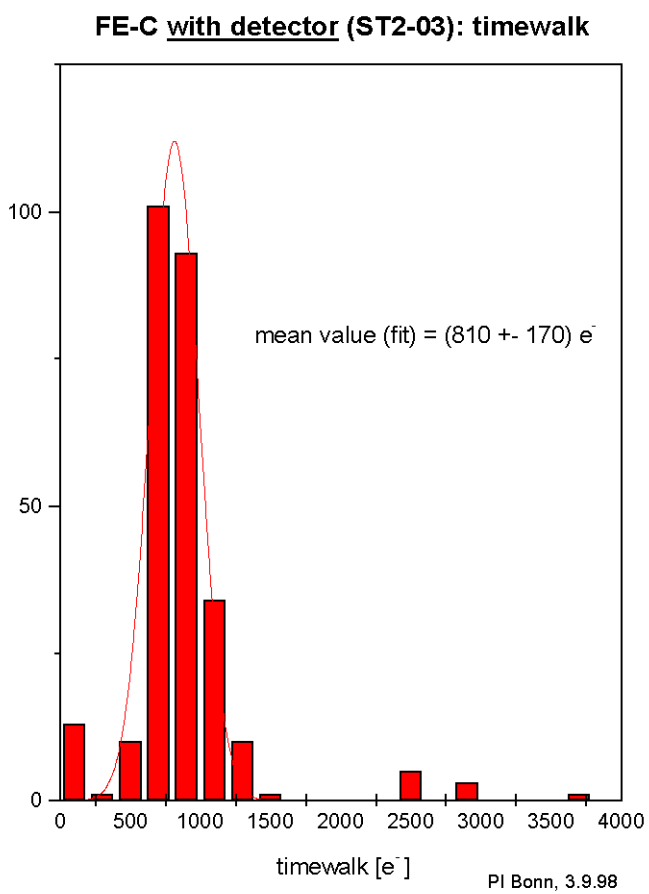
- Basic threshold scan results (slow shaping used for reduced noise):





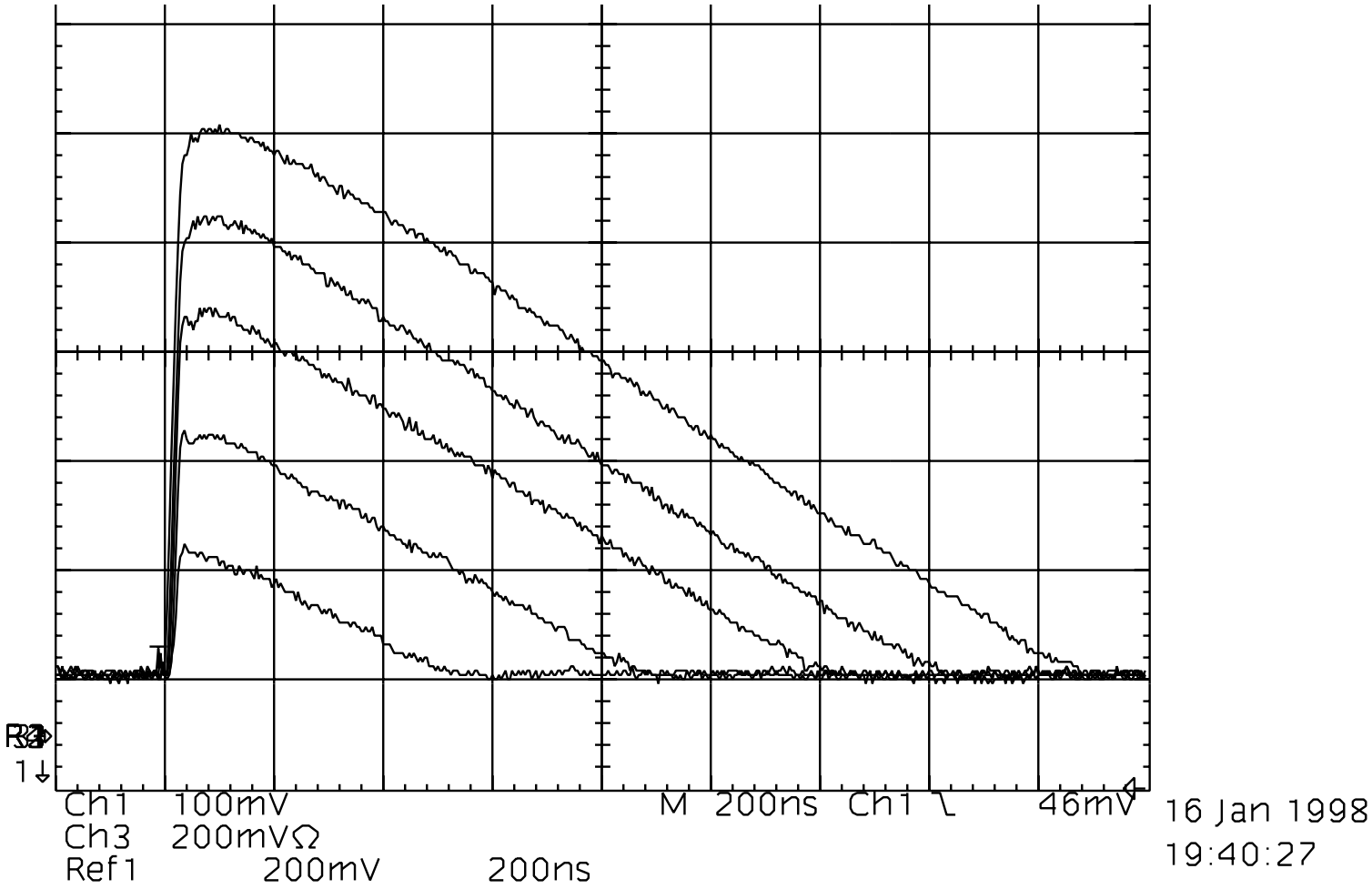
- Thresholds have been tuned, and a shaping time of about 3µs has been used.

- Measured overdrive for channels in FE-C chip:

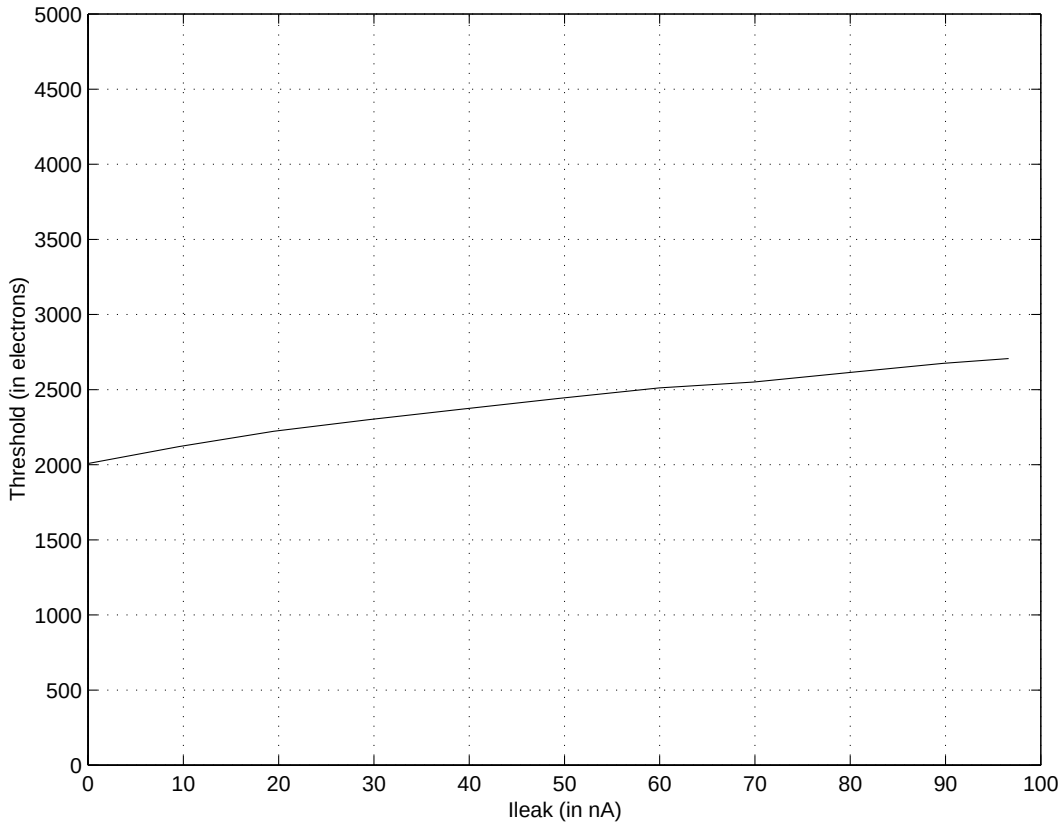


- Measure minimum charge above threshold required to turn on discriminator within 25 ns.

- Preamp performance in DMILL:

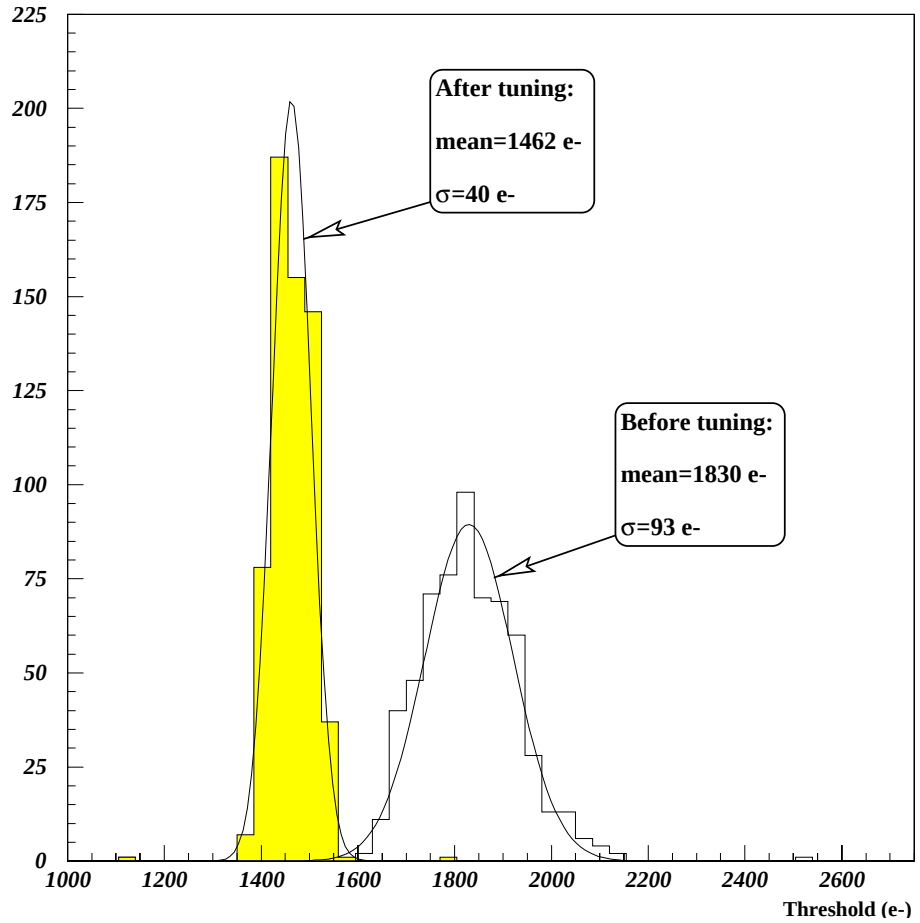


- Leakage current tolerance of DMILL version:



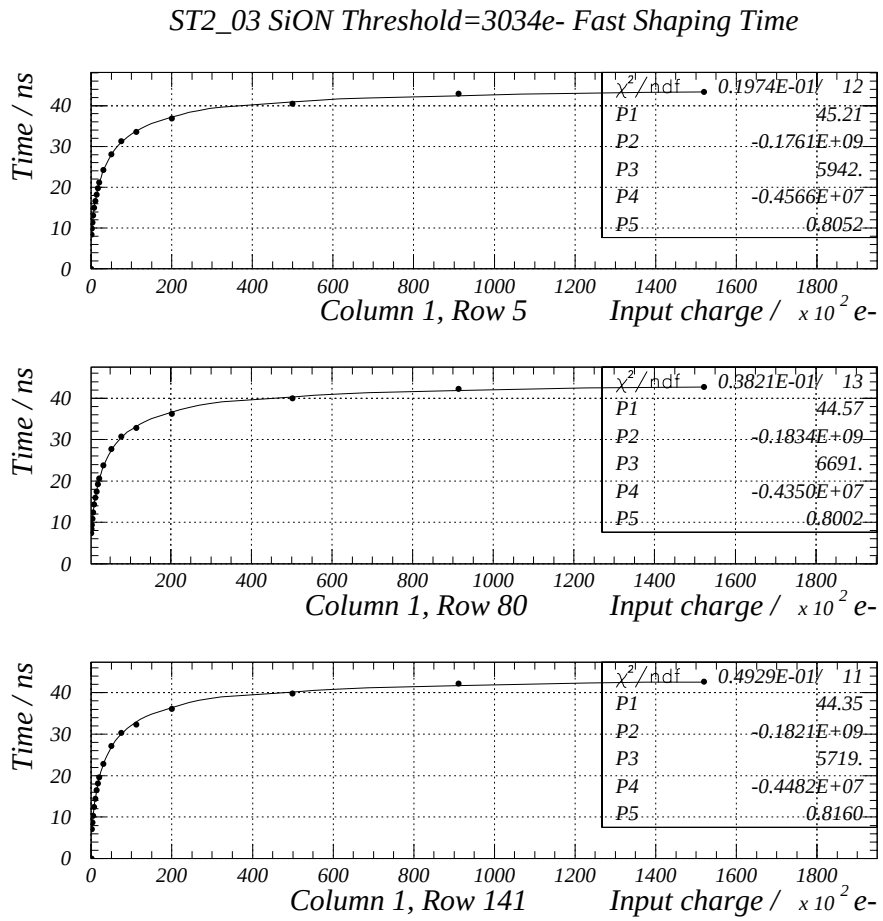
- Modest threshold shift observed with injection of large leakage current.

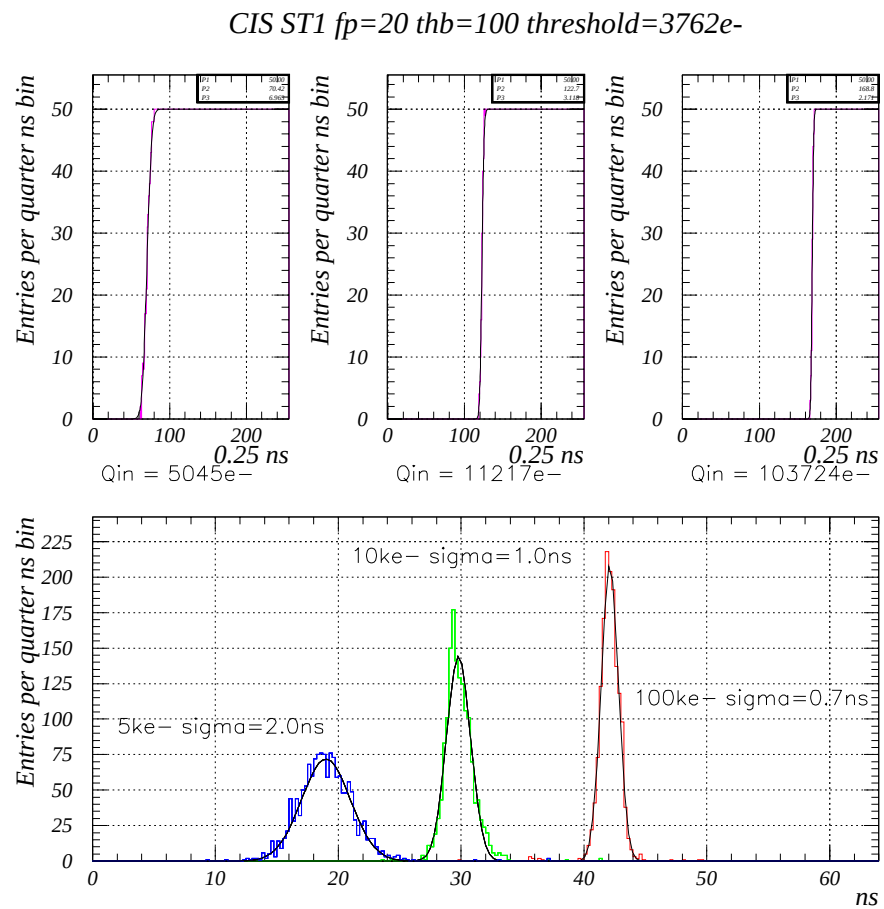
- Threshold tuning using DMILL version:



- This threshold tuning was performed on an electronics die without attached detector.

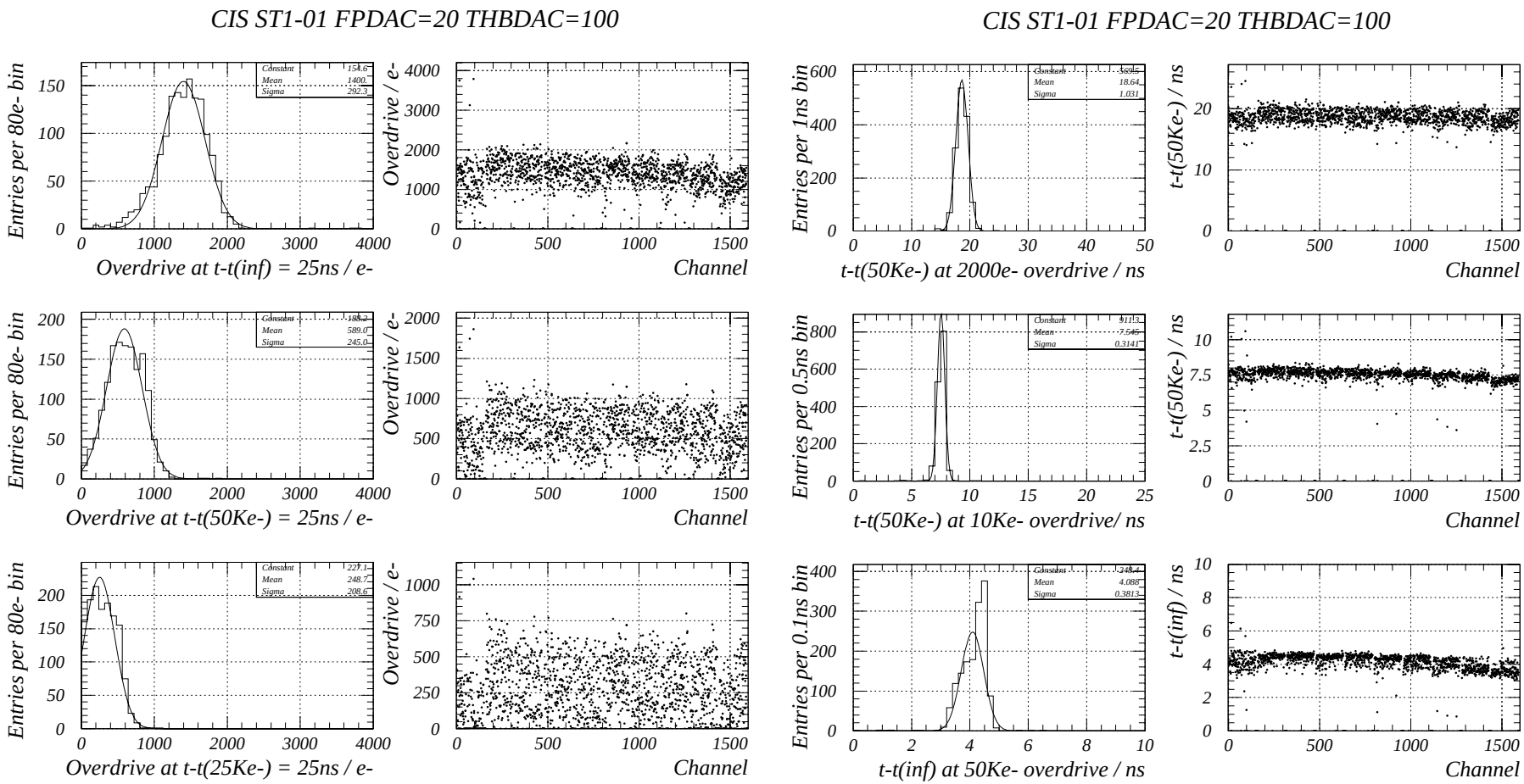
- Measurement of timewalk performance in FE-B:





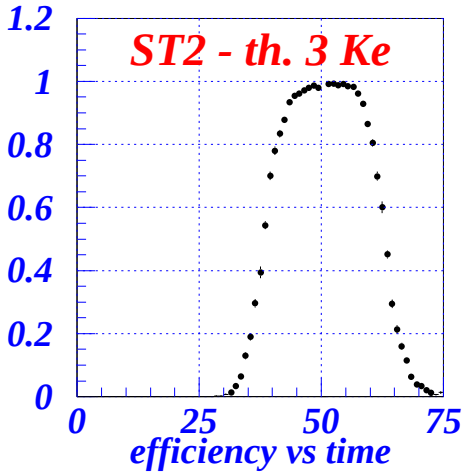
- Curves on left show typical timewalk versus charge. Plots on right show timing scans (change injection time for fixed charge), and indicate excellent timing uniformity across the full array.

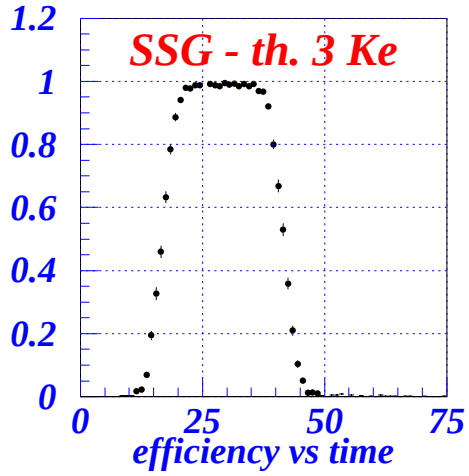
- Measurement of timewalk performance in FE-B:

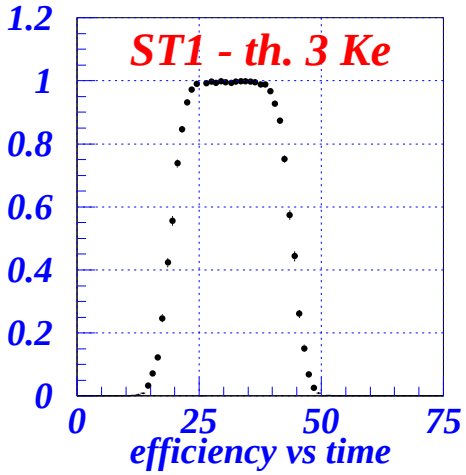


- Curves on the left show required overdrive relative to a particular input charge. Curves on the right show the time difference distribution for the same charges.

- Test beam results from FE-B chips:



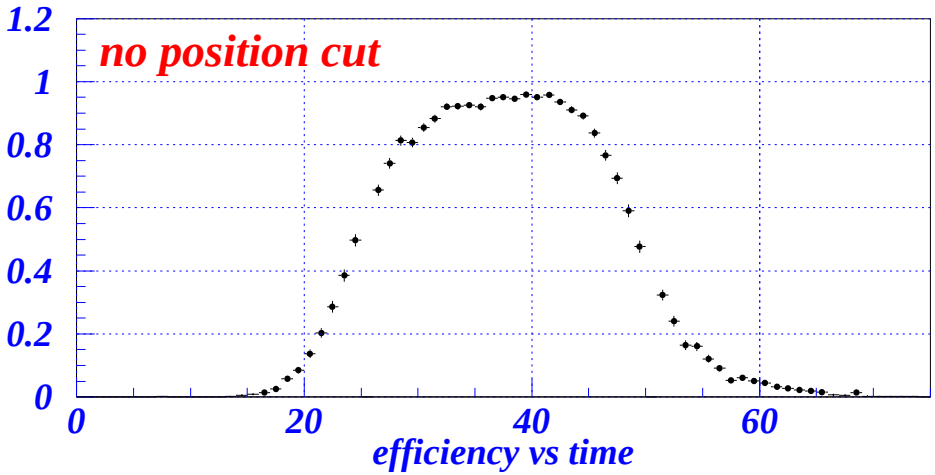


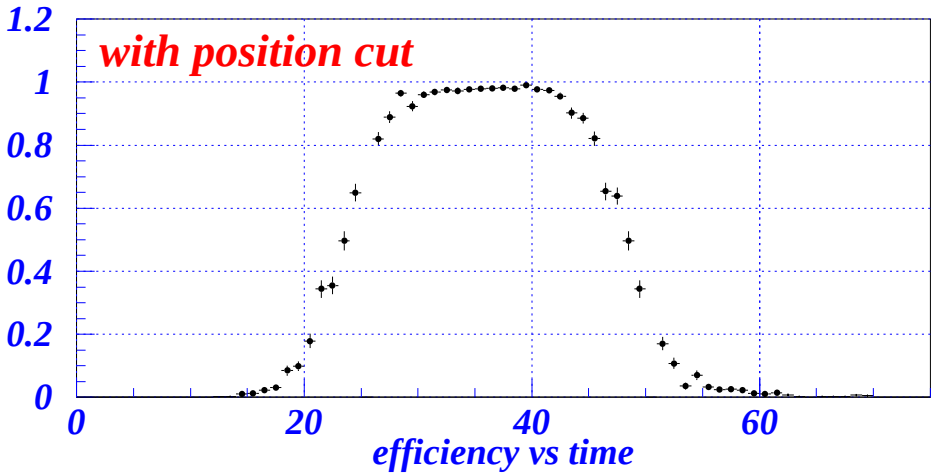


- Efficiency measured as a function of the time of passage of the beam particle through the trigger counters.
- Observe large flat region where efficiency is 100%, except for the ST2 type detector, where there are significant charge loss effects.

- Measured efficiency (single crossing) varies from 98.8 to 99.7%, with from 0.5% to 0.1% out of time hits. In particular, the ST2 detector type has large charge losses, and hits close to the 3K charge threshold.

- Same results for a detector irradiated to the full 10^{15} LHC fluence:

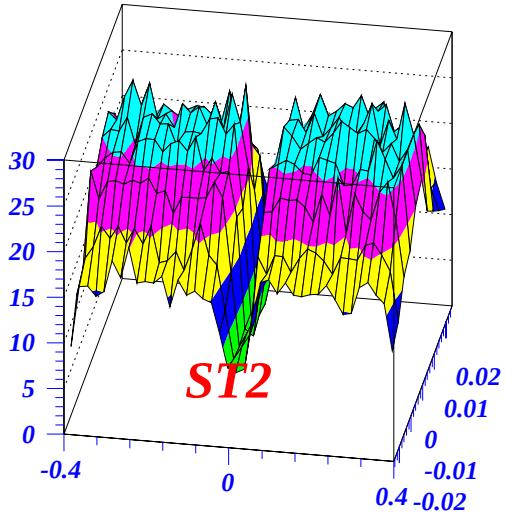




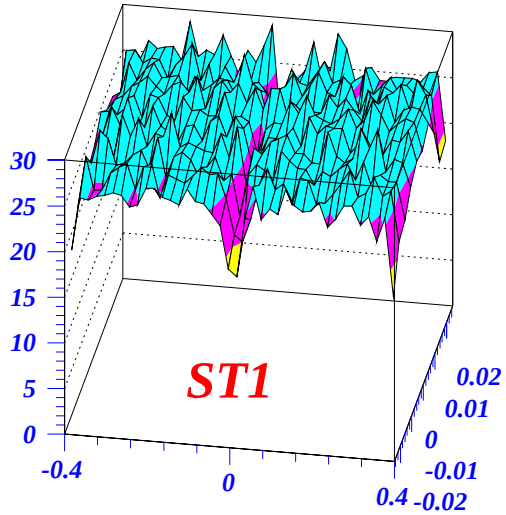
- The detector was operated at -10C and 600V bias. In these particular detectors, there is charge loss occuring because of an internal biassing structure, which is why the position cuts are required to achieve full efficiency.
- The leakage current per pixel is about 25 nA. Data was also taken at a higher temperature to give twice the leakage, and good efficiency was still obtained.

- The overall efficiency measured for this case (about 3Ke threshold), was 95.3%, but when the regions with large charge loss were excluded from each pixel, the efficiency was 98.2% with about 1.2% of the hits in other crossings.

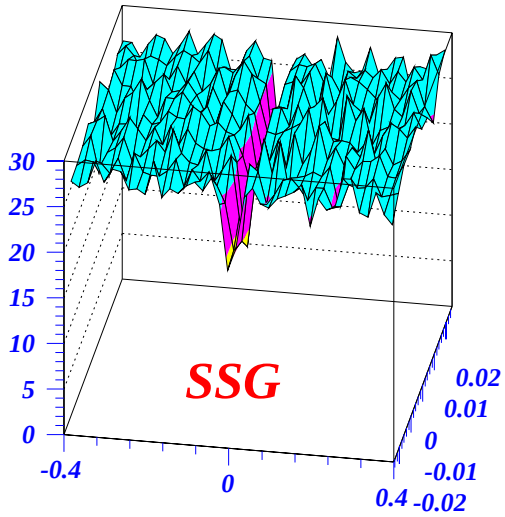
- Use of the TOT charge measurement to study uniformity of charge collection in different detector designs:



charge (Ke) vs x-y



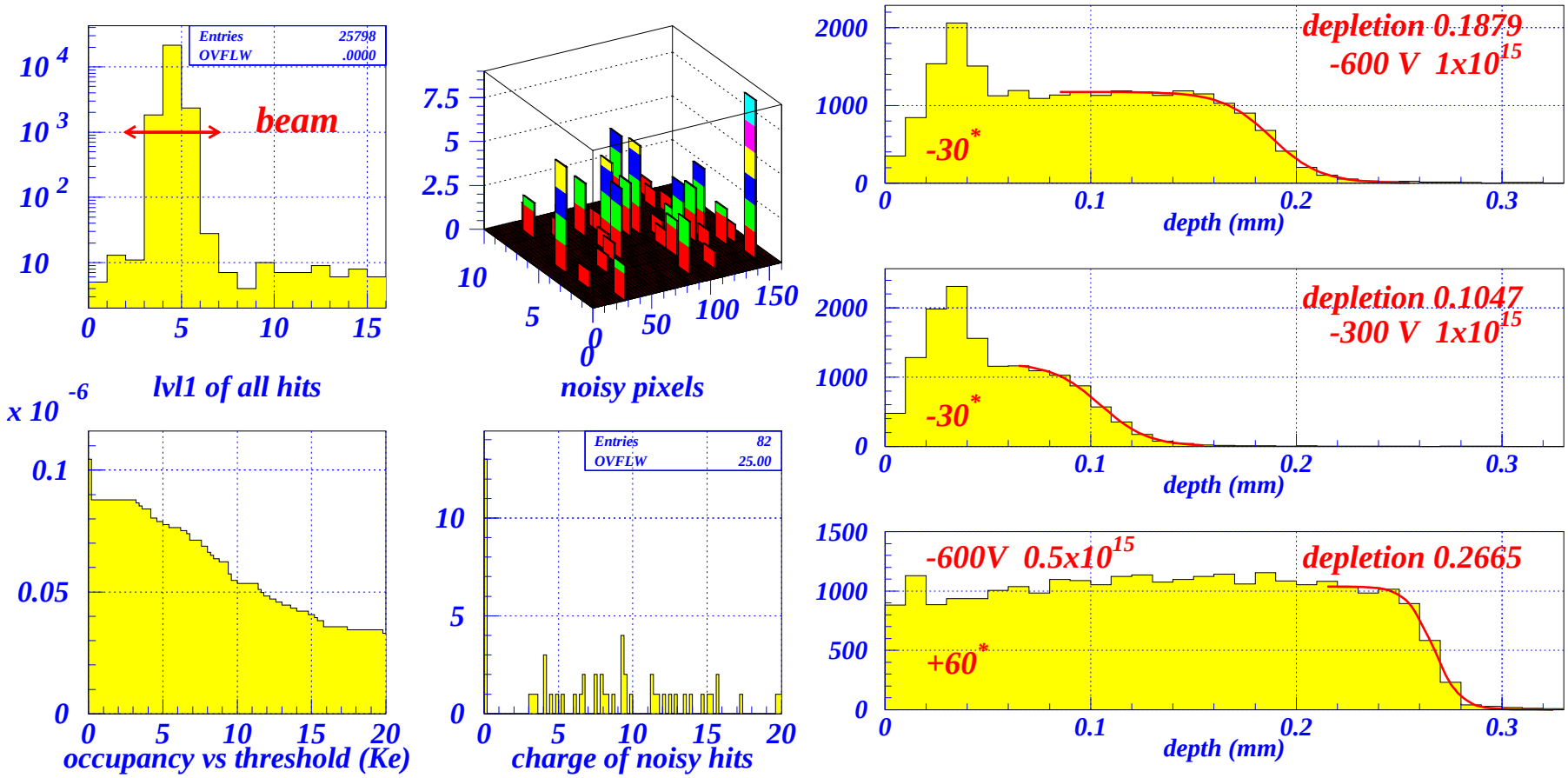
charge (Ke) vs x-y



charge (Ke) vs x-y

- Uniform collection observed in the p-stop design (ST1).
- Some loss observed near large bias structure in small gap design (SSG).
- Significant loss observed near floating n-ring in p-spray design (ST2).

- Study noise occupancy and depletion depth for irradiated detector:



- Plots on the left show a noise occupancy of about 10^{-7} hits/pixel/crossing for the 10^{15} fluence detector operating at 600V.
- Plots on the right measure the depletion depth using cluster length for highly inclined tracks. Similar studies with unirradiated detectors reproduce detector thickness to better than 10μ.

Scope of this Review

This is the first external review of ATLAS FE pixel electronics:

- We have completed the layout of all of the major blocks of the FE-D chip. We are just beginning to integrate these blocks into the overall floorplan of the chip.
- We have done simulations of these top level blocks, but they are still rather incomplete.
- We are preparing the overall chip simulation framework, and working out how to do the overall verification.
- We are several weeks behind where we had planned to be for this review. The principle missing ingredient for the review is documentation.
- However, several comments are significant: The new DMILL chip is a combination of circuit blocks which have been successfully built and studied already, and so the major activity involves converting these designs to DMILL.
- In addition, we anticipate that it is the following submission which would be a “pre-production” design. The present chip is the first rad-hard version of the demonstrator design, and most likely will require further iterations based on 25 MRad irradiation experience. Hence, we regard it as critical that this chip work well enough that we continue to learn from it, but it does not have to meet all specifications, as a pre-production chip would.

- We need to get experience with these new chips before testbeams disappear this year, and so we are prepared to trade some perfection for wafers that work roughly as we expect, and are available on time.

What do we expect from this review ?

- We hope to submit the present chip in 6-8 weeks. Depending on whether or not this review indicates major issues for follow-up, another review could be needed.
- We would like to bring our reviewers up to speed on our designs, and we hope they will continue to work with us for future submissions to Honeywell, and as we approach true production quality chips.
- We look for your advise on whether our circuit designs look reasonable, whether there are specific DMILL issues, and whether our simulation and verification protocols are good enough. We look forward to learning from designers with greater experience in DMILL.
- We imagine a modest list of suggestions, which would increase our chances for a successful submission, and perhaps point out areas where with continued effort, we could improve our designs further. Of course, any glaring problems should be brought to our attention too !

Overview of FE-D

Common design effort, based on combining different aspects of FE-A/B/C chips:

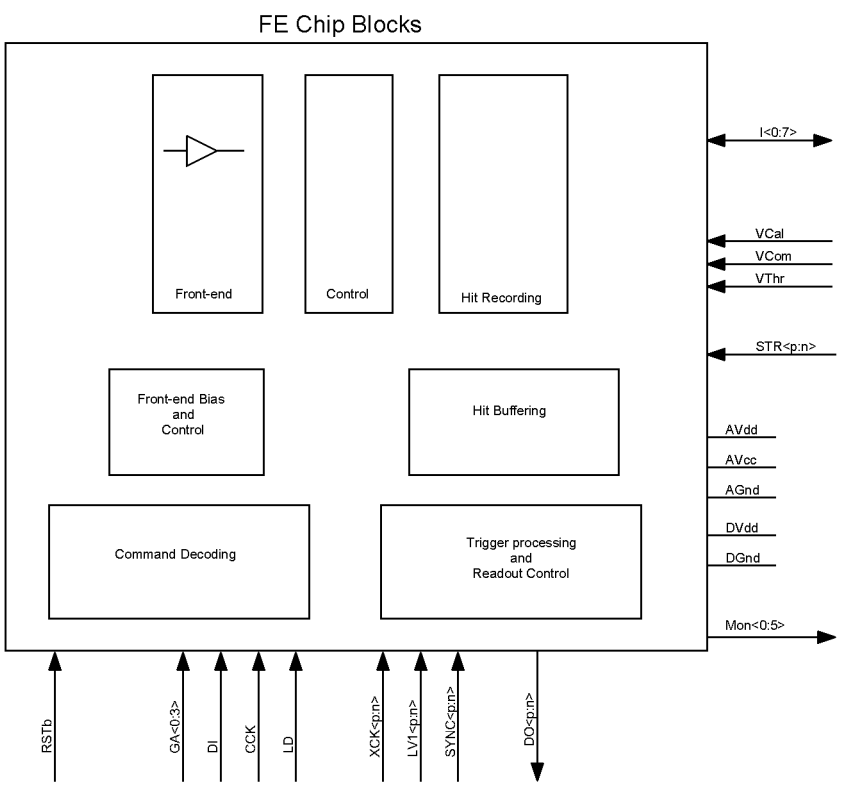
- Front-end design is basically that of FE-C and MAREBO, but is purely CMOS. Although there is a BiCMOS version of this FE (2 bipolars used for discriminator input) which has slightly better timing performance than the purely CMOS version, this cell appears to be too large for FE-D.
- The FE uses a DC-feedback preamp design which provides excellent leakage current tolerance, close to constant-current return to baseline for TOT, and very stable operation with different shaping times.
- It is followed by an AC-coupling stage, and a fast discriminator. A divider network provides fine input baseline (threshold) control and provides the resistance for the high pass filter AC-coupling stage.
- The control logic provides a 3-bit threshold trim capability in each pixel, plus individual mask and calibration inject control. A global FastOR net is created using all pixels enabled for readout, and provides a self-trigger capability.
- All critical bias currents and voltages on the chip are controlled by internal DACs (6 current mode, 2 voltage mode), which are referenced to an internal V_{BE} reference, and controlled via the chip command decoder.

- Readout design is an upgraded version of the readout architecture of FE-B.
- It uses a 7-bit Grey-coded 40 MHz “timestamp” bus as a timing reference throughout the active matrix. All pixels measure their leading and trailing edge timing by asynchronously latching this reference in RAMs.
- Hits (address plus LE/TE timing) are transferred from the pixels as soon as the trailing edge occurs, using a shared bus structure in the pixel column pair. This bus should operate at transfer rates up to 20 MHz in order to meet our requirements. Low swing signal transmission and sense amplifiers are used to achieve this.
- Significant buffering is provided in the end of column region for hit storage during the L1 latency (up to 3.2µs in ATLAS). Twenty buffers are available for each column pair. The coincidence with the L1 trigger is performed in this buffer. Hits from rejected crossings are immediately cleared.
- A readout sequencer stores information on up to 16 events pending readout. As soon as the output serial link is empty, transmission of a new pending event begins. Essentially, sending a L1 trigger corresponds to making a request for the all hits associated with the corresponding beam crossing, which are then pushed off the FE chip to the MCC.

- Global control of the chip is implemented using a simple command protocol. A global register controls Latency, DAC values, enabled columns, clock speeds, and several other parameters.
- A pixel register which snakes through the active array provides access to the 5 control lines in the pixel (Select, Mask, Trim<0:2>).
- Each chip on a module is geographically addressed, and its identity is controlled by external wire-bonds to avoid confusion.

FE-D Block Diagram:

Basic FE block diagram, expanded from module diagram:



- Within the pixel, there is the front-end (preamp/ discriminator), the control block, and the readout block.
- Just below the active pixel matrix is the biassing and control for the front-end blocks, and the buffering for the readout blocks
- Finally, there is the overall readout control and the command decoding.

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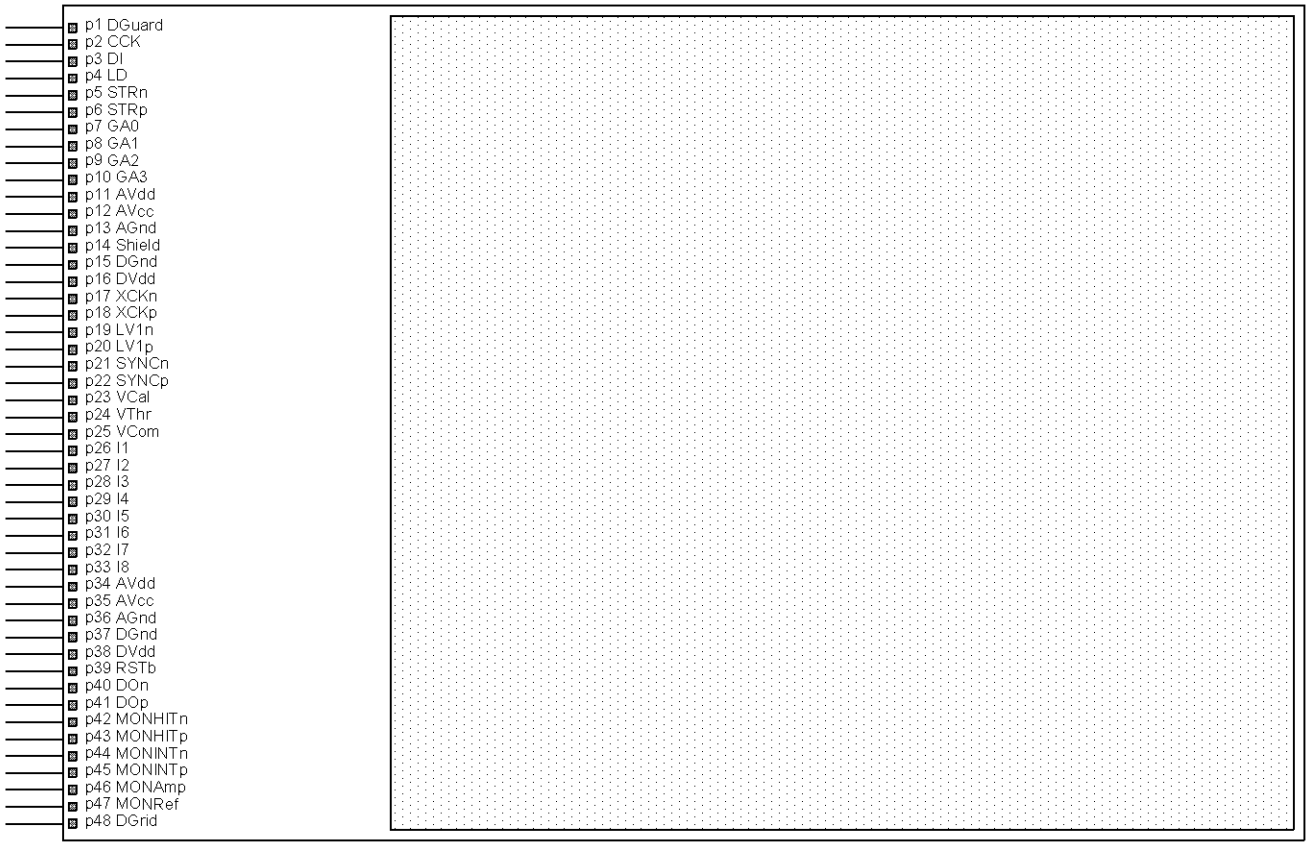
- Basic Digital I/O shown on bottom: 4 CMOS inputs for control (RSTb, DI, CCK, LD), and 4 fast, differential I/O's for timing and readout (XCK, LV1, SYNC, DO).
- Calibration and monitoring are shown on the right. A fast, differential strobe (STR) supplies calibration timing, and an analog voltage input (VCal) supplies calibration input. Dedicated monitoring pins include FastOR and test pixel output.

FE-D Pinout and Geometry

Sketch of pin assignments and overall geometry of die:



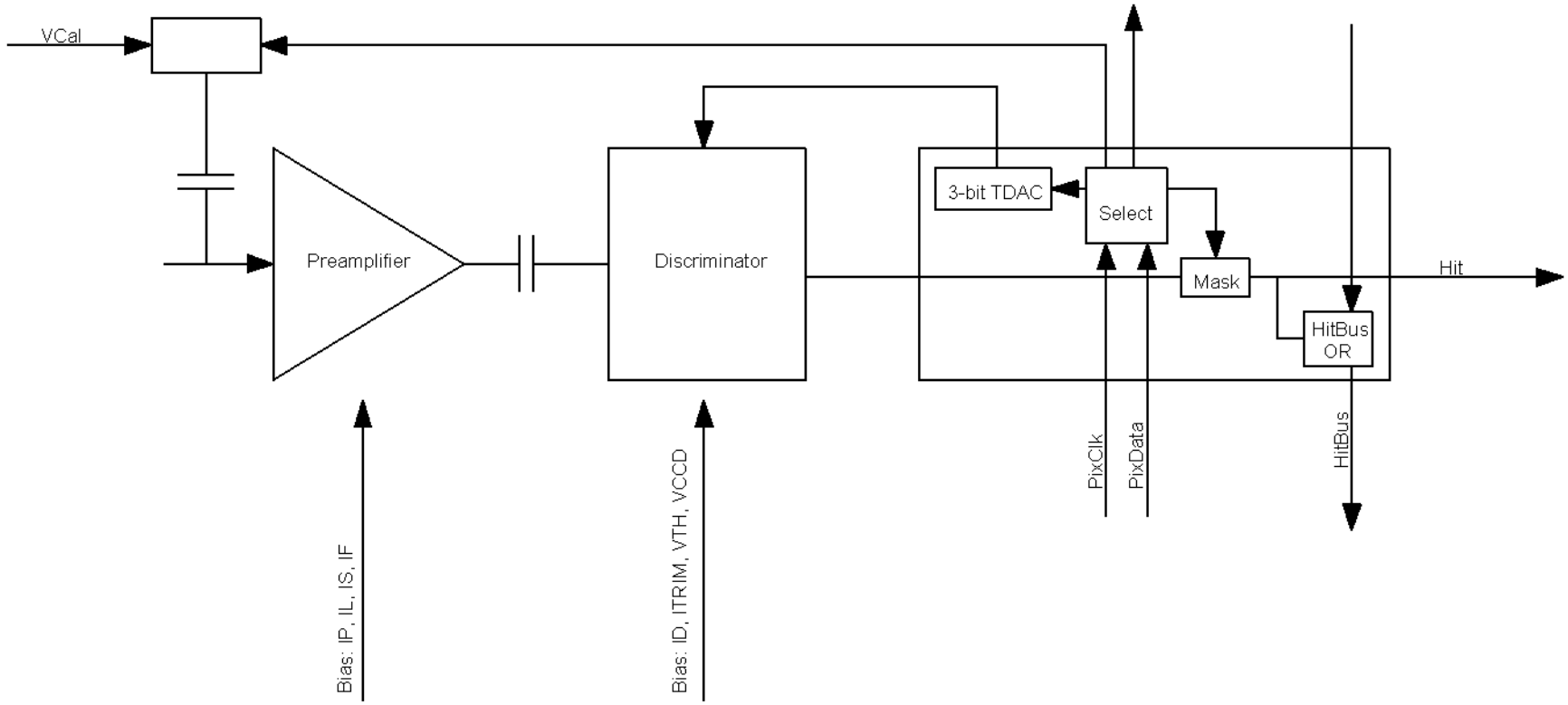
Front-end, biassing and control

Summary of the requirements:

- A nominal capacitive load of 200 fF is expected, roughly half to ground (parasitic) and half to the nearest neighbors (inter-pixel). Good performance should still be obtained with loads of 400-500fF. The n^+ on n-bulk detectors provide negative signals.
- Pixels are oriented to maximize signal and efficiency (minimize charge sharing).
- The outer layers should be 250μ silicon, and the B-layer should be 200μ.
- The expected signal after the lifetime dose of 10^{15} n-equiv/cm^2 is about 6Ke with 200V bias, and about 10Ke with 600V bias. We now propose to operate at the higher bias at the end of the detector lifetime, and have real prototype experience to show that this works well.
- This leads to an in-time threshold requirement of about 3Ke (this would be 2Ke for the lower bias voltage). This requirement has often been defined using a maximum timewalk relative to some large reference charge of 25ns, however, we believe 20ns is the right target for the complete FE chip. This could be achieved by for example setting a 2Ke threshold, and having the required overdrive for a timewalk of 20ns be less than 1Ke. This is the most challenging requirement for our front-end.

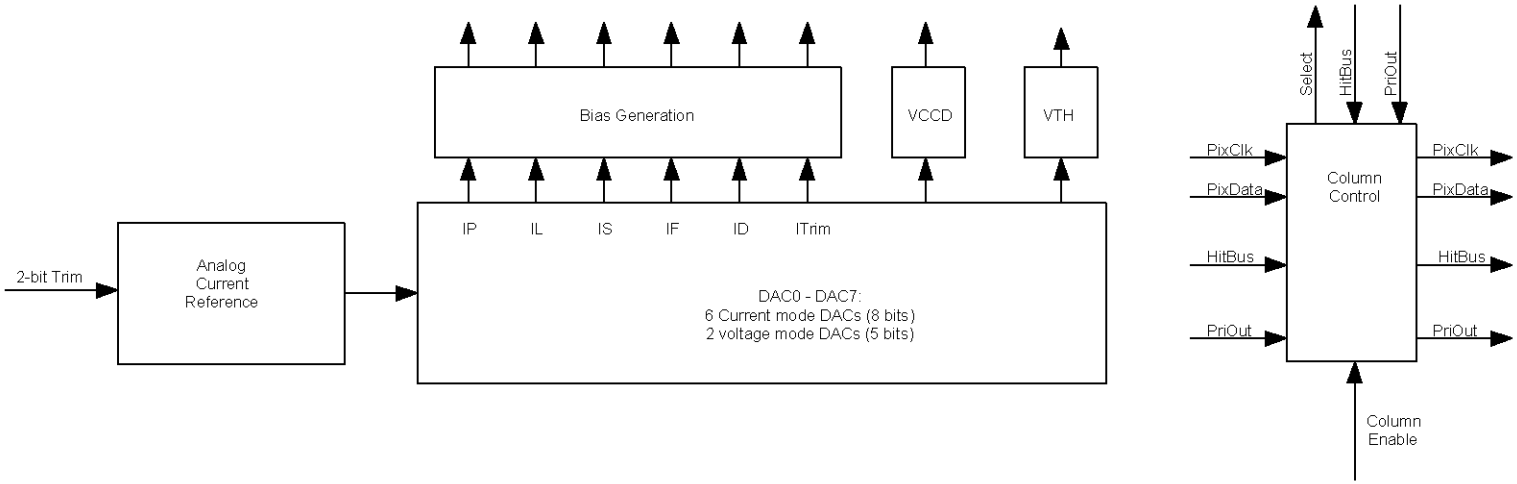
- Noise should be less than 300e and threshold dispersion less than about 200e, leading to an overall threshold “variation” of less than 400e.
- Leakage current tolerance should be at least 50nA per pixel, without significant changes in operating performance, and independently achieved for each pixel.
- Noise occupancy should be less than 10^{-6} hits/crossing/pixel.
- Crosstalk between neighboring pixels should be less than 5-10%, where this is defined as the ratio between the threshold and the charge which must be injected into a pixel to fire its neighbors.
- A double pulse resolution of 2µs is required for the outer layers, and 0.5µs for the B-layer, in order to achieve our total deadtime requirements.
- It is required to provide binary readout of each pixel, but a modest analog resolution (4-5 bits) is very desirable if it can be achieved without a large impact on the other performance specifications.
- A threshold range of 0 - 6Ke is needed.
- A calibration injection capacitor of 10fF should be included in each pixel.
- We do not know whether real diode input protection is needed. In all present chips, no explicit input protection is provided, and no major problems have been observed.

FE and Control Blocks:



- Preamp has roughly 3fF DC feedback design, 10fF injection cap, and 40ns risetime. Input transistor operates at about 9µA bias and 1.5V. Cascode and follower operate at 3V and about 1.5µA each.
- Discriminator is AC-coupled and uses a bias current of about 6µA, plus two tunable voltage supplies (VTH and VCCD) which control the threshold and AC-coupling time constant.

FE Biassing and Control Blocks:



- A V_{BE} reference is used to supply a 16µA reference current to the current mode DACs. It has 2-bit trim capability to ensure roughly +/-1µA output variation for parameter variations within DMILL corners (this is a convenience).
- The current mode DACs are a rad-tolerant 8-bit design with good linearity.
- The two tunable voltage supplies use resistor chains to control output amplifiers which supply the necessary voltages.
- A single column enable bit controls the major operations of a column pair. It allows bypassing a column pair in the pixel shift register chain, bypassing a column pair in the HitBus FastOR net, and bypassing the sparse scan readout of a column pair when transfering an event out of the FE chip.

Digital readout

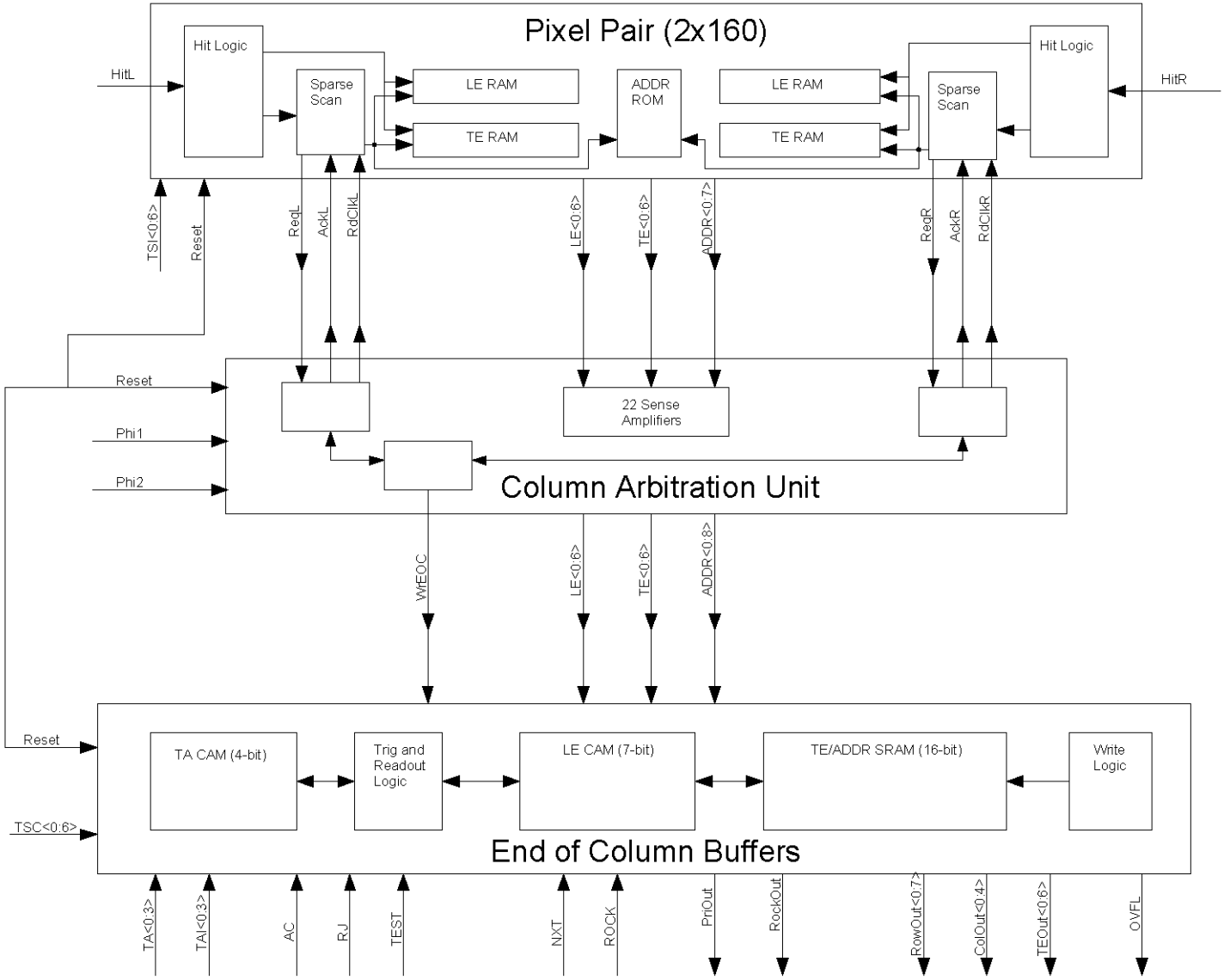
Summary of the requirements:

- Make a unique association of each hit pixel with a 40 MHz beam crossing.
- Store hits in pixel array for L1 latency period, which can extend up to 3.2µs.
- Make a modest TOT measurement by counting time differences between leading and trailing edges in 40 MHz units.
- Simulations for the current architecture exist, driven by the full GEANT simulation of ATLAS. This suggests that the current architecture needs to operate with a 20 MHz column clock rate and have 20 buffers per column pair in order to provide safe operation of the outer layers. The B-layer requirements are more stringent, and require something like 30 buffers. Further study is underway for this layer.
- There is only a single error condition which occurs, namely overflow of the EOC buffers. In the case where the EOC buffer block in a given column pair overflows, hits are lost until a free buffer exists, and the error condition is stretched to cover a full L1 latency (covering all possible events which could have lost hits due to this condition). The error status is then transmitted in the EOE word.

Specifications:

- Clock duty cycle specified to be between 40% and 60% (high phase lies between 10ns and 15ns, or nominal +/- 2.5ns).

Block diagram of the basic column-pair readout:



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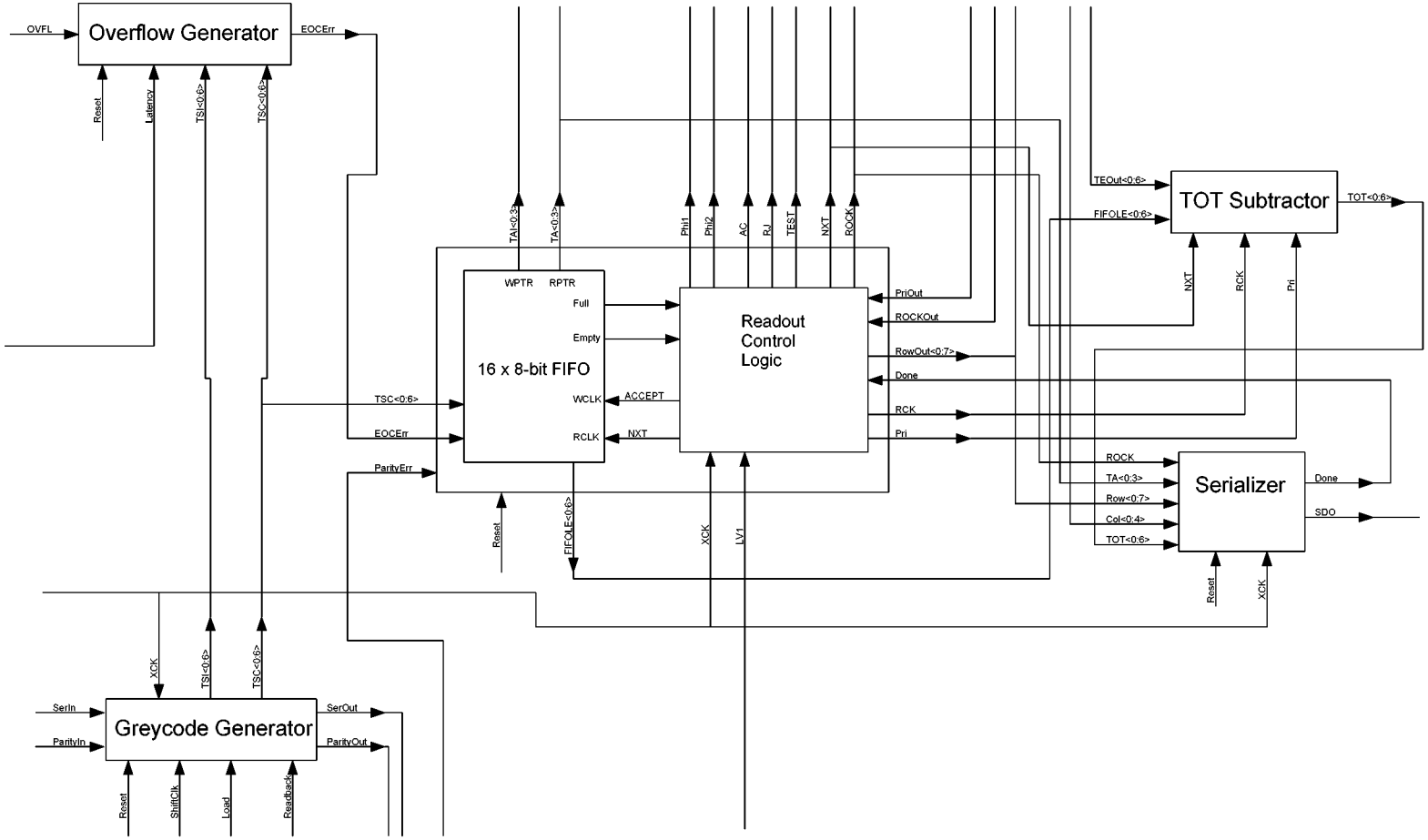
Block diagram of the Readout Control:



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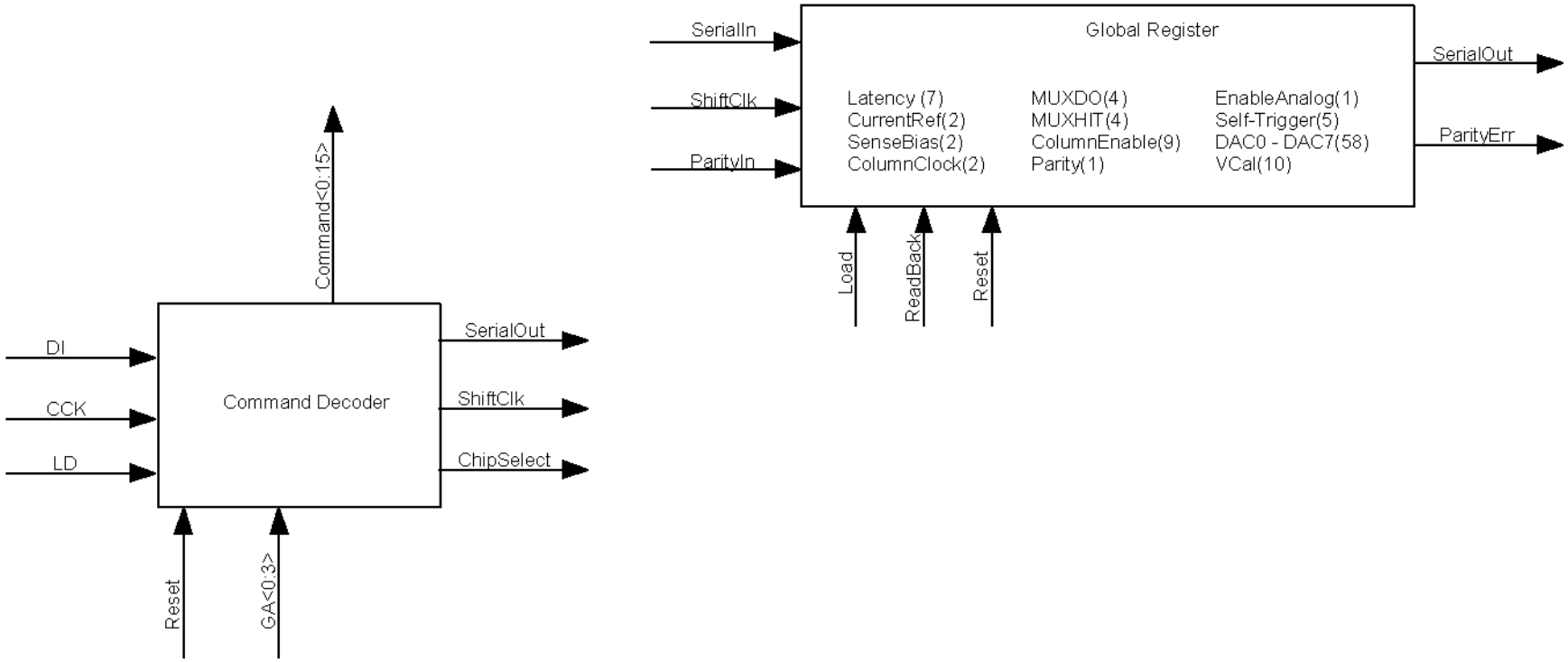
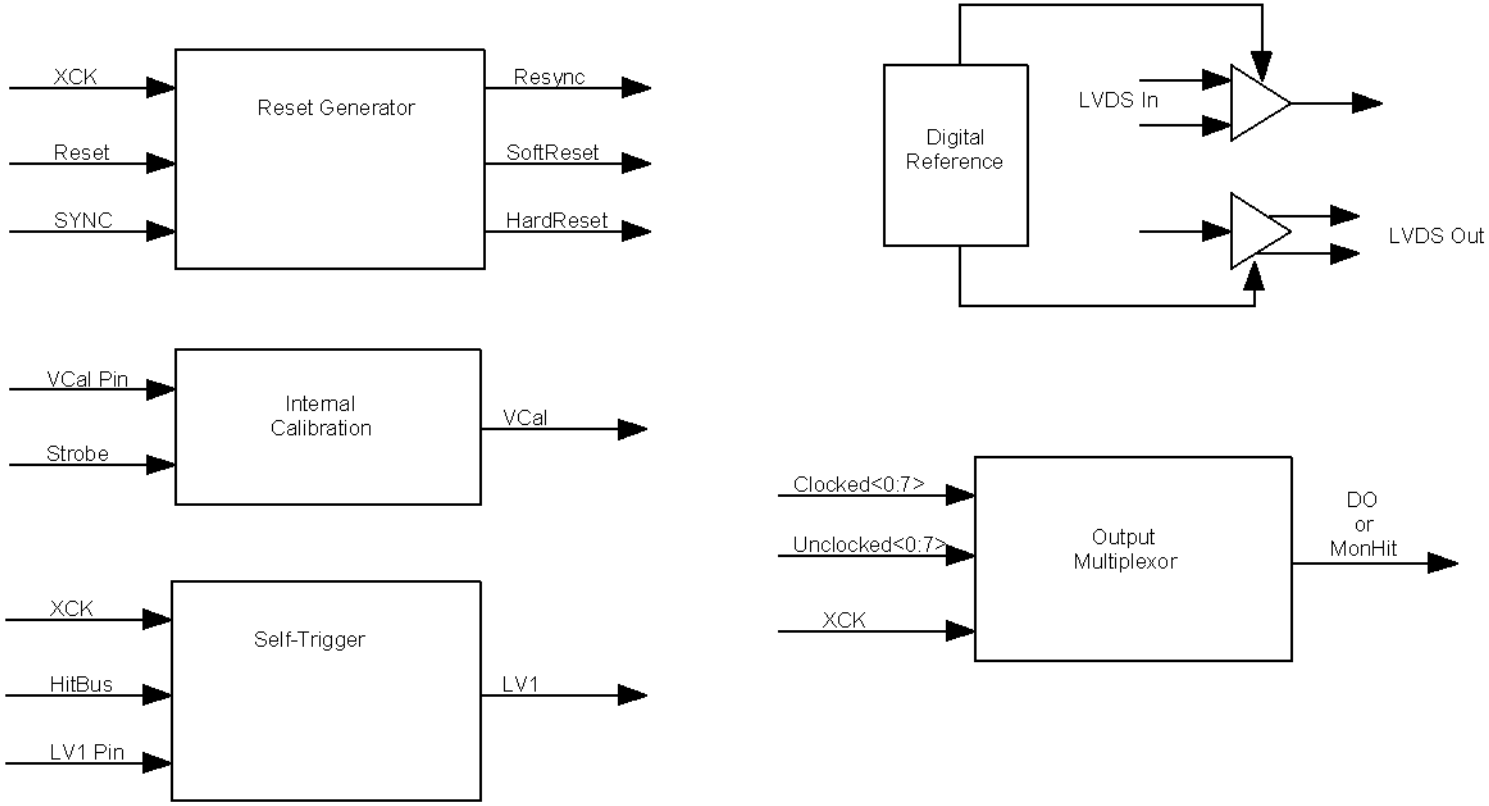
Block diagram of Command Decoder and Global Register:



- Simple command protocol, based on a 21-bit command field, after which LD goes high and associated data may be transmitted. This supports 16 different, independent commands.
- Global Register controls overall operation of FE chip. Because of the critical importance of its bits, it does a parity calculation (chain of XORs) of the contents, and generates a Parity Error if the parity is not what is expected (due to SEU). This parity error is transmitted as part of the EOE word to flag such errors.

Block diagrams of remaining blocks in the periphery:



- The previous chips use a compensated FET switch to chop an incoming voltage and inject the corresponding charge into the pixel injection capacitors. A new circuit is under study to perform this task, see talk of P. Fischer.
- There is a reset generator that either uses the external RESET pin, or the width of the SYNC input in XCK clocks, to generate internal reset signals.

- There are three basic reset signals. The Resync makes sure that all FE on a module are using the same trigger number (it resets the trigger FIFO). The SoftReset puts the chip into the “empty” state for data, but does not alter any configuration information. Finally, the HardReset also resets all configuration information to default states (typically zero for most register bits).
- There is a self-trigger generator, which either passes the input LV1 through to the trigger processing circuits, or uses the internal FastOR signal to generate its own LV1 signal after a programmable latency. This allows the chip to be used in self-trigger mode with a source, and it will simply produce output data whenever it sees a signal on the internal FastOR.
- There is a dual 8-fold output multiplexor which selects which internal signal or data stream is transmitted off the chip through the serial output. The first eight inputs are synchronized with XCK, while the second eight are not. An identical multiplexor circuit is used both for the standard serial output pins, and for the MONHIT output pins.
- The LVDS driver/receiver circuits use a second internal current reference to define the drive current. The common mode voltage is referenced to the DVdd supply using a diode. While not quite conforming to the LVDS specification, the design works well enough for local pixel module communication. Have performed corner simulations of the performance of a driver/receiver pair with realistic loading. The most critical signal (XCK) was found to be within specifications.

Simulation Issues

- Base timing and drive analyses on use of TEMIC-supplied SPICE models (strictly optimized for ELDO use only).
- We have models for fast/typical/slow pre-rad and after 25 MRad, including possible rebound effects in NMOS. We use these models extensively in our corner analyses.
- We perform analyses with fast-fast pre-rad, typical prerad, and slow-slow postrad as our three nominal cases. These three SPICE models are also used to annotate delays in our simple standard cell libraries for use in Verilog simulations as well, so we can also perform corner simulations in Verilog.
- Our goal is to make a chip that is still fully functional at supply voltages of AVdd/AVcc of 3.0V/1.5V and DVdd of 3.0V.
- This looks very challenging for some critical circuit blocks.
- The principal requirement is that we live inside our power budget, which is clearly easier at lower supply voltages. However, for the digital supply, the present FE-B uses only 70 mW at 3.5V (the budget is 100 mW). We would be quite satisfied if this DMILL chip operates correctly for the worst case (slow-slow post-rad) at a somewhat elevated supply voltage of 3.5V, or perhaps even as high as 4.0V.