

Proposal for Chip/Sensor Assemblies in 1999

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Leo and myself charged to work on a draft plan for chip/sensor assemblies during the 1999 “final prototyping” period

First draft sent out in October, some comments received...

Goals of Plan

During the 1999 period we need to:

- Build enough parts of different types to fully evaluate the new generations of components (chips, sensors, etc). In particular, there will be Prototype 1.5 and 2 Sensors and FE-D and FE-H rad-hard demonstrator chips.
- Build enough parts to confirm that the module design really performs as needed. This will surely lead to minor (or major) improvements in existing designs.
- Build a large enough volume of parts that we begin to understand the procedures and yields well, and that the expertise to build and test modules becomes distributed to the institutions who will play these roles during production.

This will be a very significant effort:

- Significant volume of bump-bonding and flip-chipping required
- Many peripheral items needed (support cards, test systems, infrastructure at institutes)
- Begin discussions now to allow financial and manpower planning

Available Parts

Sensors:

- Prototype 1 wafers: still several wafers available for work at IZM and Alenia
- Prototype 1.5 wafers: 20 wafers to be available with improved p-spray designs. These have two tiles per wafer, only one of which is p-spray
- Prototype 2 wafers: 20-40 wafers to be available by Summer 99. There would be either 2 or 3 tiles per wafer, most likely of a single baseline “style”.

Electronics:

- There are 15 remaining FE-B wafers, with typically 80 good die after probing, or an expected 1200 good die
- There are a total of 200-250 good FE-C die available
- The FE-D order will most likely be for 8 wafers. The number of die per wafer will depend on what else we place in the reticle. I would expect about 80 die per wafer, or about 600 potentially good die. If the yield is (worst case ?) 30%, this would give about 200 parts. More optimistic assumptions would give 400 parts.
- The FE-H order will be in the range of 5-8 wafers. We have done a reticle layout and would get 104 potentially good die per wafer. This gives a similar range of 200-500 good parts, depending on yield assumptions.

Goals of Assembly Construction

Sensors:

- Evaluate performance of Prototype 1.5 and 2 designs, before and after irradiation

Electronics:

- Complete evaluation of existing chips before submitting rad-hard versions
- Evaluate performance of new rad-hard FE chips

Bump-bonding:

- Continue to evaluate vendors for yield and other technology issues

Modules:

- Evaluate performance of different designs, and iterate details of designs

Build a mixture of single-chip devices and modules of various types:

- Single chip devices best for detailed studies of many options, and for performing irradiation studies (they don't require scanning during exposure).
- Modules would be build in "non-hybrid" as well as Flex and MCM-D flavors to be sure we understand the effects of the module design itself on the performance.

Details of Proposal

Very near-term (existing parts, multiple module types):

- Build as many modules as possible with existing detector parts using IZM and Alenia for bumping. This amounts to about 6 non-MCM-D modules at IZM (4 FE-C and 2 FE-B) and up to 8 non-MCM-D modules at Alenia.
- Use remaining Prototype 1 sensor wafers for second run of MCM-D with IZM
- Make new versions of support cards (at least for “non-hybrid” module and Flex)

Next steps (single-chips assemblies):

- Make about 20 assemblies to evaluate Prototype 1.5 sensor designs
- Make about 30 assemblies to evaluate FE-D and FE-H performance
- Make about 20 assemblies to evaluate Prototype 2 sensor designs
- The total number of assemblies would probably be about 60 due to “overlaps” between the three classes.
- **Note:** H8 testbeam schedule has runs in May, July, and Sept. 99 of about 2 weeks each. May should concentrate on MCC-based modules and Prototype 1.5 sensors. July would possible add FE-D, and Sept would possibly add FE-H.

Next steps (module assemblies):

- Make about 15 modules with new Prototype 1.5 p-spray design. In order to gain further module experience, we should also make about 15 Tile1 modules as well from this sensor run. This would probably be about 10 FE-C modules and 20 FE-B modules (at which point, there would be no remaining FE-C parts).
- Make at least 10 modules using FE-D and 10 using FE-H. These modules would use the most advanced detector designs at the time of their construction. If the yields of these chips are high (60% instead of 30%), then we could double this number.
- Make the largest possible number of modules using the Prototype 2 sensor run. Here, we will ultimately be limited by electronics. The conservative approach would be to build as many modules as possible using existing FE-B parts. There should be parts for a further 40 FE-B modules at this stage. If we wanted to build more rad-hard modules, additional electronics wafers would need to be purchased at considerable extra expense.
- The total number of modules would be in the range of 60-100. As we understand the program today, all of these modules would be built with the “nominal baseline” design.

Testing and Evaluation Issues

Single-chip support cards:

- So far, we have used 60 of these cards in 1998. Parts now exist for building 50 more, and 10 are being loaded next week. More can be ordered as needed.

Module support cards:

- All existing “non-hybrid” module support cards have been used. An improved design is under way, and it is proposed to build 10-12 additional cards.
- A total of 10 Flex support cards were built, and about 6 have now been used. It is proposed to implement similar improvements here, and make more boards.
- A total of 4 MCM-D support cards were built.
- Up to an additional 50-70 “hybrid” support cards would be needed. The number and type of the cards depends on the module baseline and the number of modules that would be dedicated to more realistic mechanical mounting studies.

Realistic Prototypes:

- We will need to move to module prototypes with realistic attempts at optolink and power tape connections. We will also want to build up multi-module prototypes on stave-like and sector-like mechanical supports, but readout of such systems will be difficult in 1999 (it requires real module interconnects and working RODs).

Test systems:

- Eight PLL/PCC test systems have been delivered already. Eight more are under construction and should be delivered by Jan. 99
- We are proposing to build a simple “optoboard” interface for the PLL to support construction of modules with the prototype opto-link parts to be provided by the SCT community in mid-99. This would be available in limited quantities (we will only get 10 opto-link packages in 99), but seems a better match to our needs than collaborating on a full optoboard interface to a ROD with the SCT groups.

Test Software:

- New release of PixelDAQ and PLL firmware should provide basis for further development in module testing area. Support for readout in full MCC mode is provided and works (only tested with FE-B so far).
- Complete threshold scan time for one chip is now down to under 3 minutes (about 50% I/O) using hardware histogram capability (such a run acquire 15K events per pixel). This allows a basic module characterization in less than one hour.
- We have not yet addressed the question of simultaneous characterization of multiple chips (e.g. source run with all chips enabled for readout). PLL internal memory supports only single-chip histogramming. Very significant memory needed for histogramming 50K pixels !
- PixelDAQ does not support operation with multiple PLL's. This may be needed.

Module Support Cards

- After initial very positive experience, there are a number of proposed changes for the Module Support cards for the “next generation”. We will keep the existing mechanical design, but resize Aluminum support pedestal to fully support chips: 22.2 mm by 60.6 mm. Wire bond lengths will grow slightly.

“Non-hybrid” support card:

- Include external VCal capability with LEMO and 5:1 resistor divider.
- Provide HitBus buffering, and support global, jumper-selectable “module wide” HitBus output using LVDS-CMOS conversion, open-drain OR, and CMOS-LVDS conversion. Provide jumper to allow disconnect of power for all non-MCC and non-FE power from PCC, with alternate external connection.
- Remove decoupling capacitors for bias nodes (8 DAC currents and MON_REF)
- Increase the size of the remaining 3 decoupling capacitors at the FE chip level (I would recommend an 0508 part to give us flexibility in sizing). Attempt to make all five power connections (AGnd, AVcc, AVdd, DGnd, DVdd) as complete planes.
- Drop all monitoring pads along the outside edge of the card, and also drop termination for FE-B MON_TIME outputs (only MON_HIT connection remains)
- Put jumper-selectable DC connections on DGUARD and DGRID to AGnd.
- Route traces so that board opening can fit over as-cut module (22.2 x 63.4 mm)

Flex hybrid support card:

- Add AGnd/DGnd connection jumper close to module
- Provide HitBus support for source testing, including the full “module wide” OR capability described previously.
- Modify trace routing to allow larger cutout which will clear the module dimensions of 22.2 by 63.4 mm
- Implement jumpers to allow external connection of power, either by connection to header or by soldering of Flex pigtail (footprint to be defined).
- Implement connections for placing at least one Pt100 on the Flex
- Implement a scheme for mechanical protection of the module for transport and lab use.

Summary

List of objects required for this program:

- Flip-chip of about 60 single-chip assemblies
- Construction of about 60 single-chip support cards
- Flip chip of about 60-100 module assemblies
- Construction of about 10 “realistic” modules which include power tapes and optolinks (not necessarily both on a given module), included in flip-chip above.
- Construction of 10 additional “non-hybrid” module support cards
- Construction of about 50 additional baseline module support cards
- Construction of PLL optoboard for optical link tests
- Construction of more realistic mechanical prototypes (stave-like and sector-like objects for multi-module mounting) ? Difficult to do multi-module tests without real interconnects (opto-links)

This does not include a corresponding mechanical prototyping program, which should also be organized, and could involve significant bump-bonding with thin substrates, etc...