

Studies of Data Corruption in FE-I2/FE-I2.1 Modules

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Summary of earlier measurements:

- Original split-VDD FE-I2.0 modules: LBL_20 and LBL_22
- First FE-I2.1 modules for irradiation: LBL_23, LBL_24, LBL_25

Detailed measurements of recent FE-I2.1 modules:

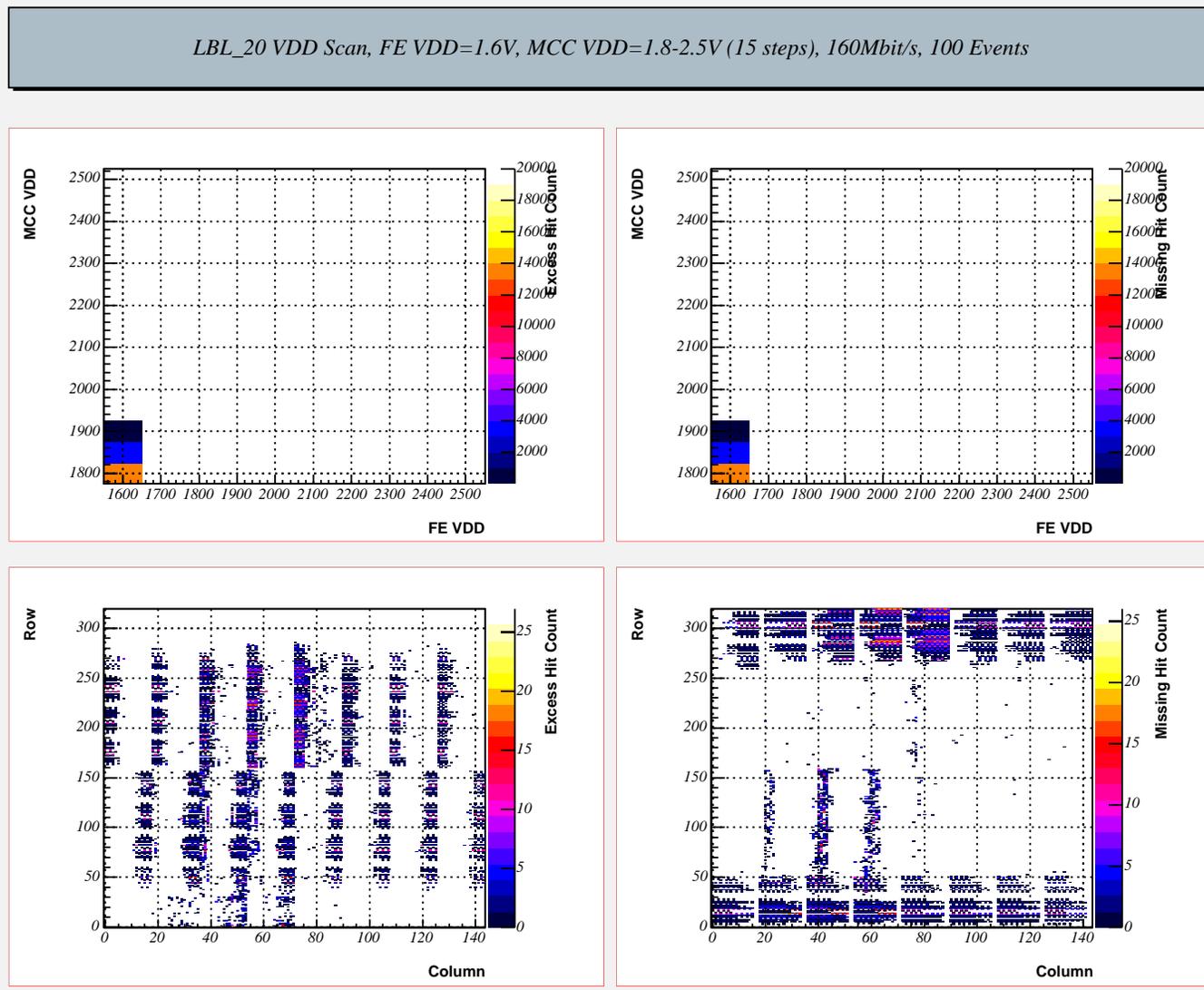
- Standard FE-I2.1 module: LBL_26, and split-VDD FE-I2.1 module: LBL_27
- Study transients on FE_VDD and MCC_VDD during operation using picoprobes
- Study error rates (missing and excess hits) versus FE_VDD and MCC_VDD

Pattern of failures:

- MCC-I2 shows data corruption at VDD in range of 1.8-2.1V, depending on output bandwidth and temperature.
- During standard scans, see FE_VDD transients related to activity in chip when hits are injected. Amplitude of transients is significantly larger when using PP2 regulators.

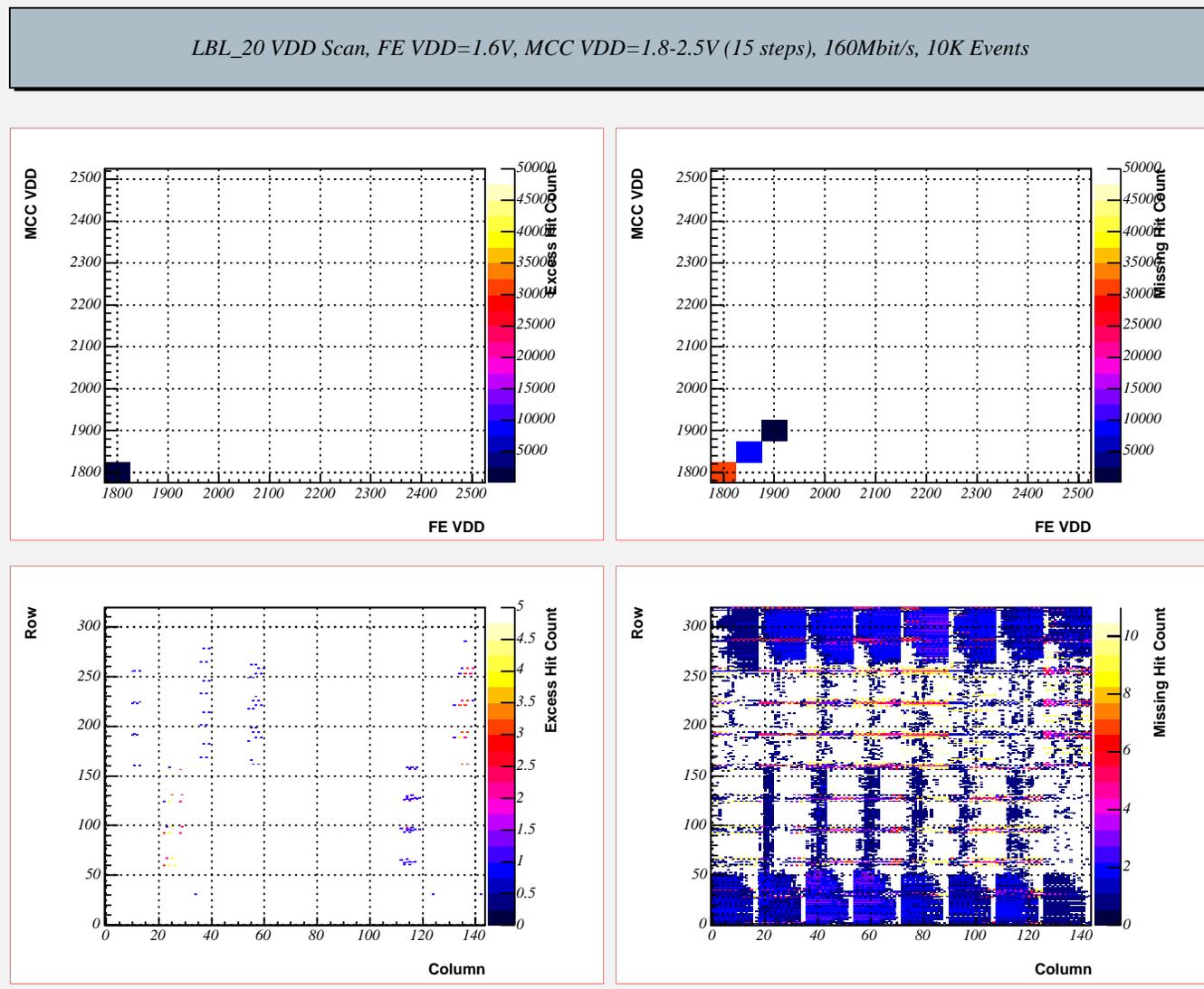
Summary of earlier measurements

- Example of LBL_20, split-VDD FE-I2.0 module:



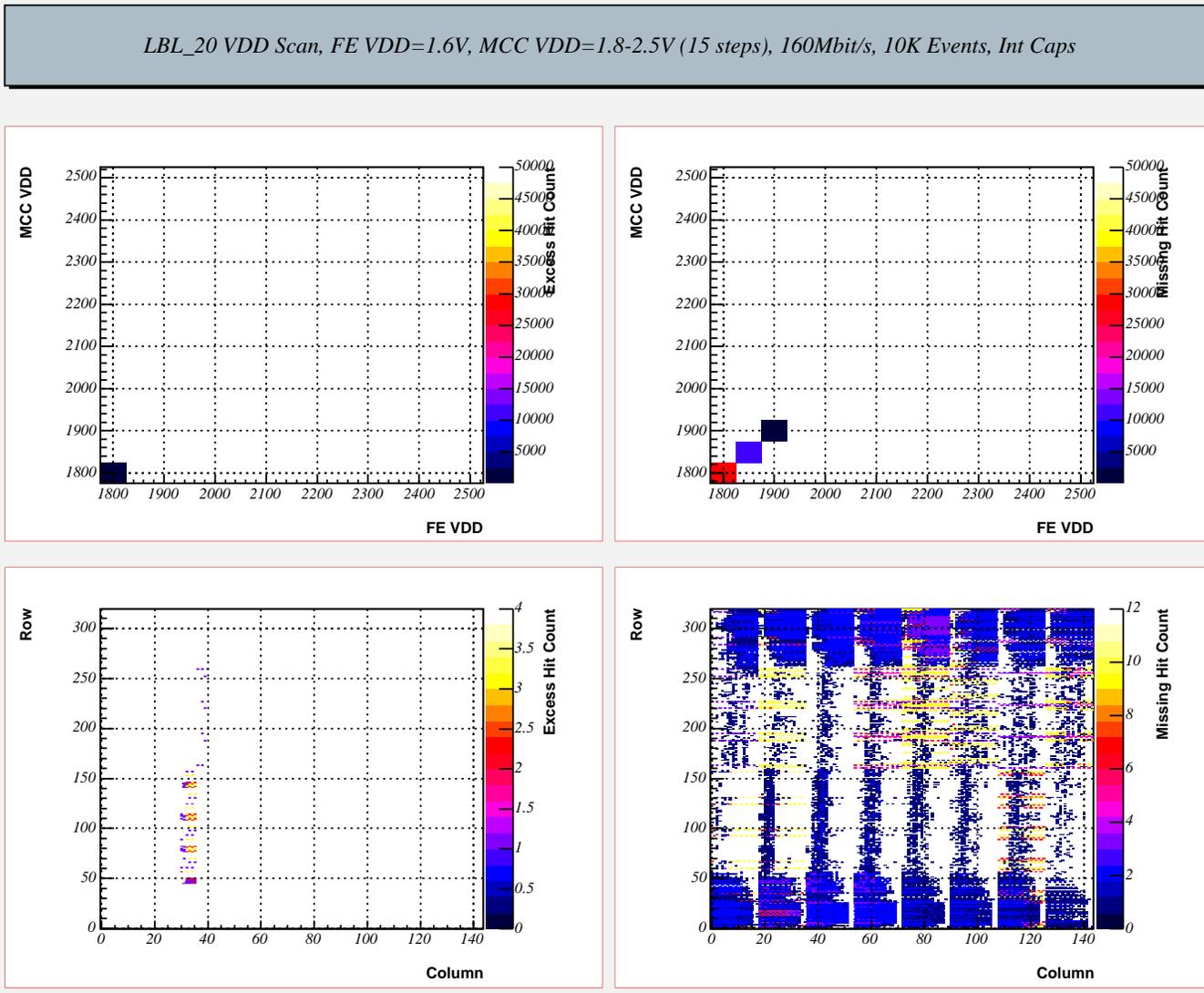
- Error rate disappears at 1.95V for VDD (FE_VDD forced to 1.6V for FE-I2.0).

- Example of LBL_20, split-VDD FE-I2.0 module, with 10K event statistics:



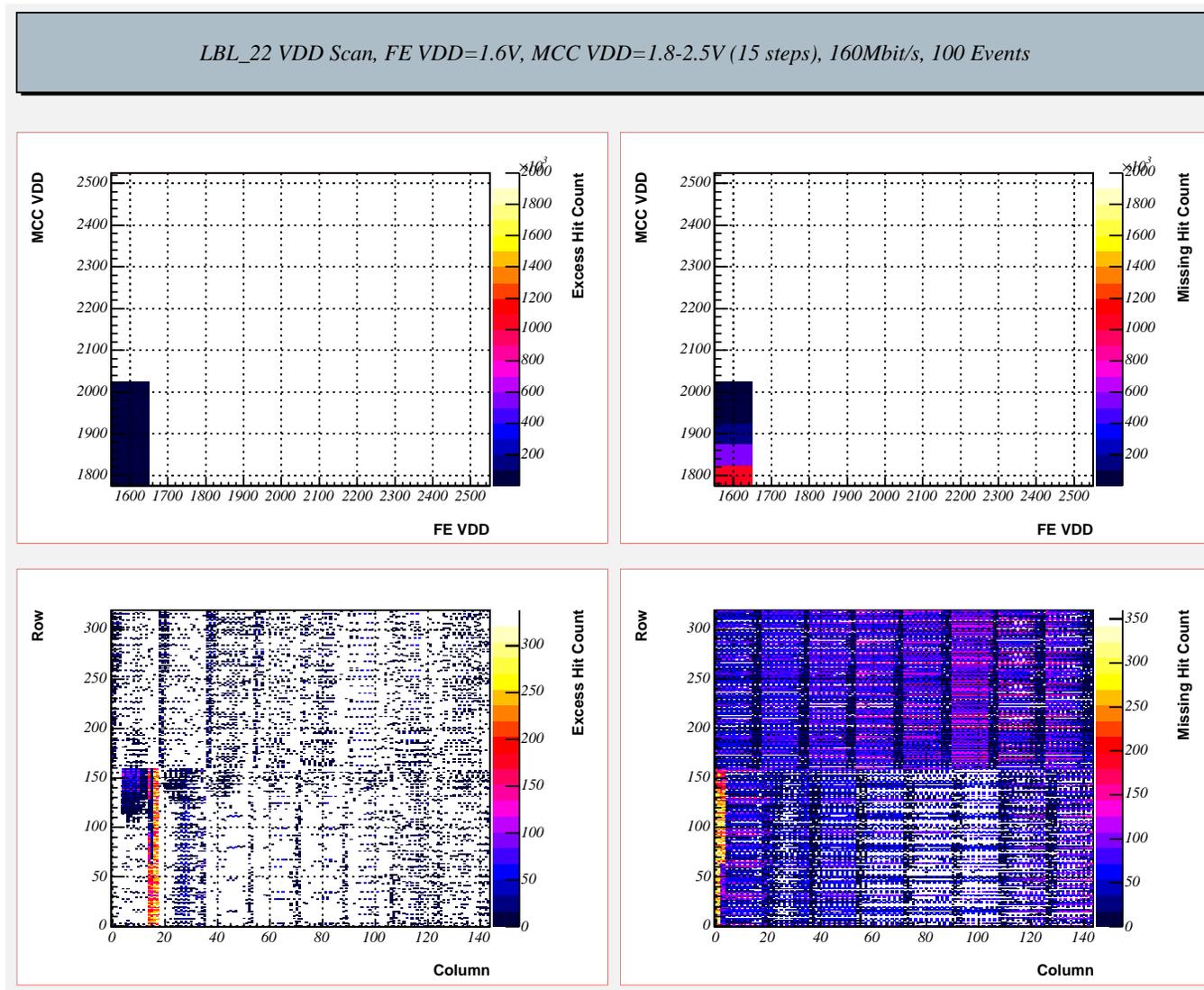
- Reference plot to compare internal decoupling on pixel VDD off (default) with internal decoupling on (next plot).

- Example of LBL_20, split-VDD FE-I2.0 module, with 10K events, decoupling on:



- No significant change observed with internal decoupling enabled.

• Example of LBL_22, split-VDD FE-I2.0 module:



- Error rate disappears at 2.05V for VDD (FE_VDD forced to 1.6V for FE-I2.0), about 100mV higher than for LBL_20. Total number of errors is about 100 times higher for this particular scan as well. Note: one dead pixel in module removed by hand.

- Also have results for LBL_23, LBL_24, and LBL_25. However, these results are suspect because they all involved long micro-cables used with the Andreas board, where the timing was probably too marginal to reach stable conclusions.
- Made measurements on modules for the irradiation after they had been connected through PP0 while in the T7 barrack. These tests were done with conservative CKR delay timing on PP0 board, and should be reliable. Again, the temperature was about 30C (depending on how long we waited to make measurements).
- In this case, set regulator boards to 2.35V, then 2.25V, and finally 2.15V, doing 50K event digital inject scan for each. In the barracks, these scans could be run at 160Mbit/s. Observed that BN_30 showed MCC data corruption symptoms at 2.15V, and LBL_25 showed MCC data corruption symptoms at 2.15V. BN_30 and GE_26 showed a different type of data corruption for several scans, typically associated with 1-2 mask stages, and for a wider range of VDD. Other modules showed perfect digital behavior at 2.15V regulator setting. We did not have time to pursue this further. Decided to carry out irradiation with VDD=2.35V.
- At the end of the irradiation, four of the seven modules (BN_30, GE_26, LBL_24, and LBL_24) showed MCC data corruption in 100 event DFIFO scans at -7C and the nominal 2.35V VDD. Further investigations of this are planned soon.
- Note also that barrel modules have additional voltage drops not covered by the sense loop compared to disk modules. This should be in the range 50-100mV, but have never seen a measurement of difference between sensed voltage and voltage on large decoupling caps on a barrel module (Genova claims 80mV ?).

Reminder of IDD versus VDD:

- Measured for an idle but configured FE-I2.1 module:

VDD	IDD
1.6 V	537 mA
1.7 V	572 mA
1.8 V	611 mA
1.9 V	649 mA
2.0 V	689 mA
2.1 V	731 mA
2.2 V	776 mA
2.3 V	823 mA
2.4 V	874 mA
2.5 V	929 mA

- Increasing VDD from 2.0V to 2.2V is about a 13% increase in current, and only barely inside the 800mA IDD total budget with the module in the idle state.

Recent Measurements

Assemblies:

- LBL_26 and LBL_27 built using recent low bump-quality IZM modules. LBL_26 is standard module. LBL_27 has split MCC and FE VDD trace (DGND is still common).

Measurement setup:

- Used Agilent supply in remote sense mode for FE VDDA and VDD supplies. Used Agilent supply in normal mode for MCC VDD supply. Supply cable length for remote sense was about 2m and used AWG20 wires.
- Initially used modified Andreas board, but with present 80cm disk micro-cables, this works correctly only for the most extreme TPLL phase ($-4T_u$). It was apparent that this was having a large influence on the results (shifting error thresholds by 100-200mV relative to PP0 board). With modest changes in MCC voltage, the output data timing will shift slightly, causing even the most extreme TPLL phase to no longer work perfectly. This could explain some of the earlier higher voltage thresholds found for error free operation in the lab at LBL.
- All subsequent measurements were made with a PP0 Support board with XCKR delay cable length adjusted so that the typical good phase window ($\pm 2-3T_u$) was centered roughly at $0T_u$. This should prevent small changes in output data phase from causing extra data corruption errors.

Comments on module scan operation:

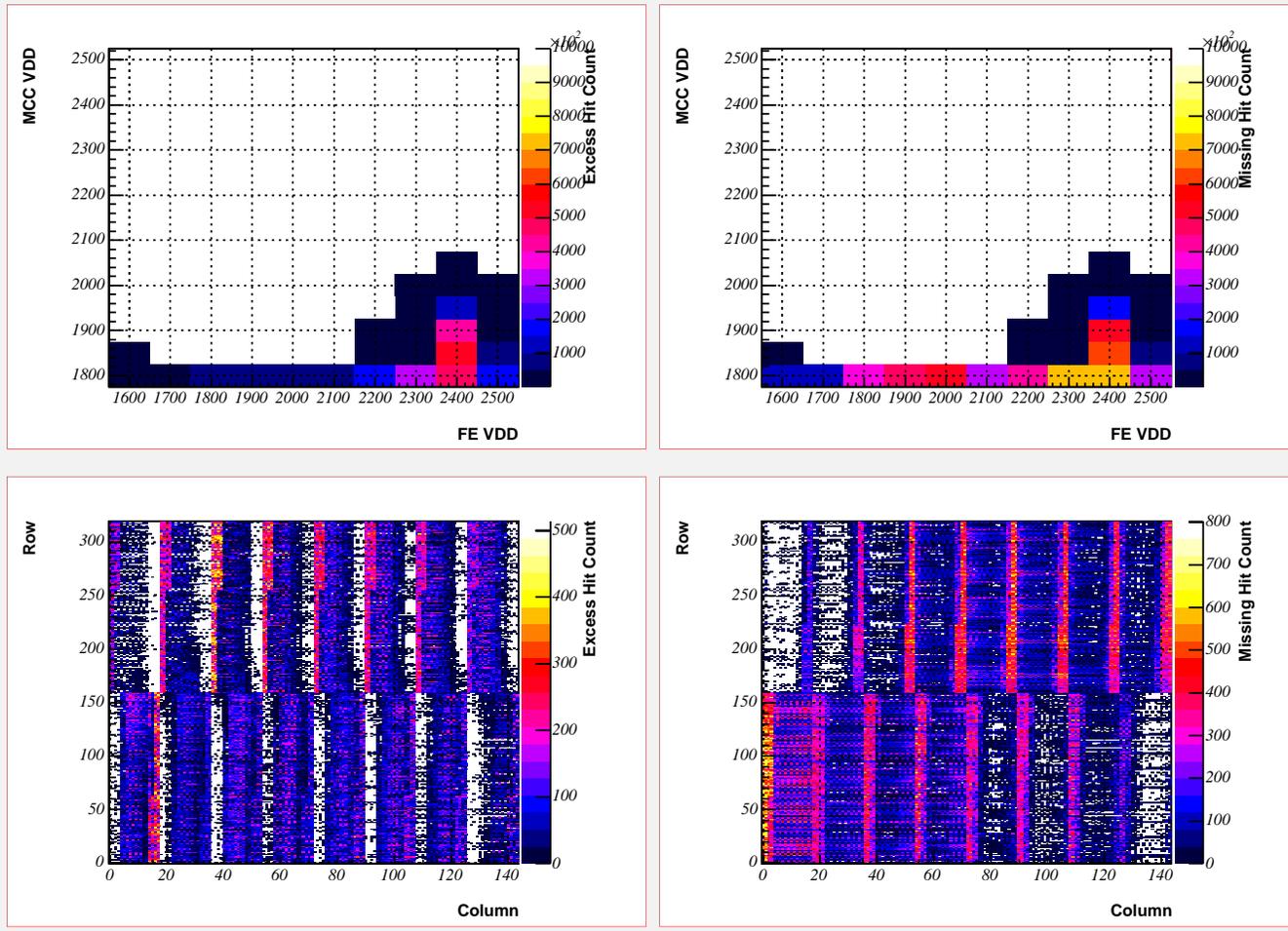
- Due to problems observed in critical tests like the T7 irradiations, TurboDAQ by default now issues a TPCC reset at each mask stage. Note that this is a drastic step, and results in the TPCC FPGA being reloaded, with all registers cleared. This results in stopping the clock for a period of a fraction of a second. In the latest TurboDAQ version, there are switches to control the TPCC and MCC resets issued by default at each mask stage (located inside the Advanced panel).
- Brief tests with TPCC resets off or on indicate that this does not seem to have a significant effect on the MCC data corruption problems observed. However, the transient on the VDD lines when operating with regulators in remote sense can be very significant.
- Another observation is related to the operation of Digital Injection in FE-I chips. Presently, the digital injection per pixel only requires the enabling of the Readout latch in the pixel to operate, unlike analog injection which requires both the Select and the Readout latch to be enabled. This was on the change list for FE-I2, but was not implemented due to time constraints. The result is that one must be careful NEVER to do a digital inject scan with Readout enabled for all pixels (default static mask in older versions of TurboDAQ), as this results in all pixels being injected with hits, and produces VERY LARGE power transients. If one is not careful in doing “one FE at a time” scans, this could happen, because the default static mask used to have Readout enabled for all pixels, and the static masks are used to initialize all un-scanned chips.

Measurements of error rates using 2D VDD scans for LBL_27:

- Use obscure TDAQ features to scan FE_VDD from 1.6V to 2.5V, and MCC_VDD from 1.8V to 2.5V, with a digital inject scan at each voltage point (150 scans). Scans must be done in “Binned TOT” mode in order to perform the mask staging as the innermost loop. GPIB scan code modified to force supply output stabilization before continuing with the scan. Typical scans used 100 events per pixel, some high statistics scans were made with 10K events per pixel.
- This feature is now supported in TurboDAQ 5.0 for 2-channel Agilent LV supplies only (use GPIBAUX1 and GPIBAUX2 as scan variables). Note for now, must be sure the same supplies are not controlled from the Power panel
- Analysis consists of counting the number of “excess” hits (more than expected) and “missing” hits (less than expected) in each pixel.
- Examine effects of output bandwidth (only 40Mbit/s and 160Mbit/s work in V14 TPLL firmware for FE-I2.1 modules). Significant differences seen, but are not related to trigger interval (performed 160Mbit/s scans with longer trigger interval, and did not reproduce worse results seen for 40Mbit/s). TPLL V15 firmware fixes the problem with 80Mbit/s scans, so these have also been studied.
- Examine effects of concurrent injection (1440 hits per module) versus one FE at a time (90 hits per module). As expected, this has a large effect.
- No temperature control available during these tests, so typical module temperatures are in range 28C to 35C. This is known to enhance error rate effects.

Standard scan of 100 events per pixel for LBL_27 (160 Mb/s):

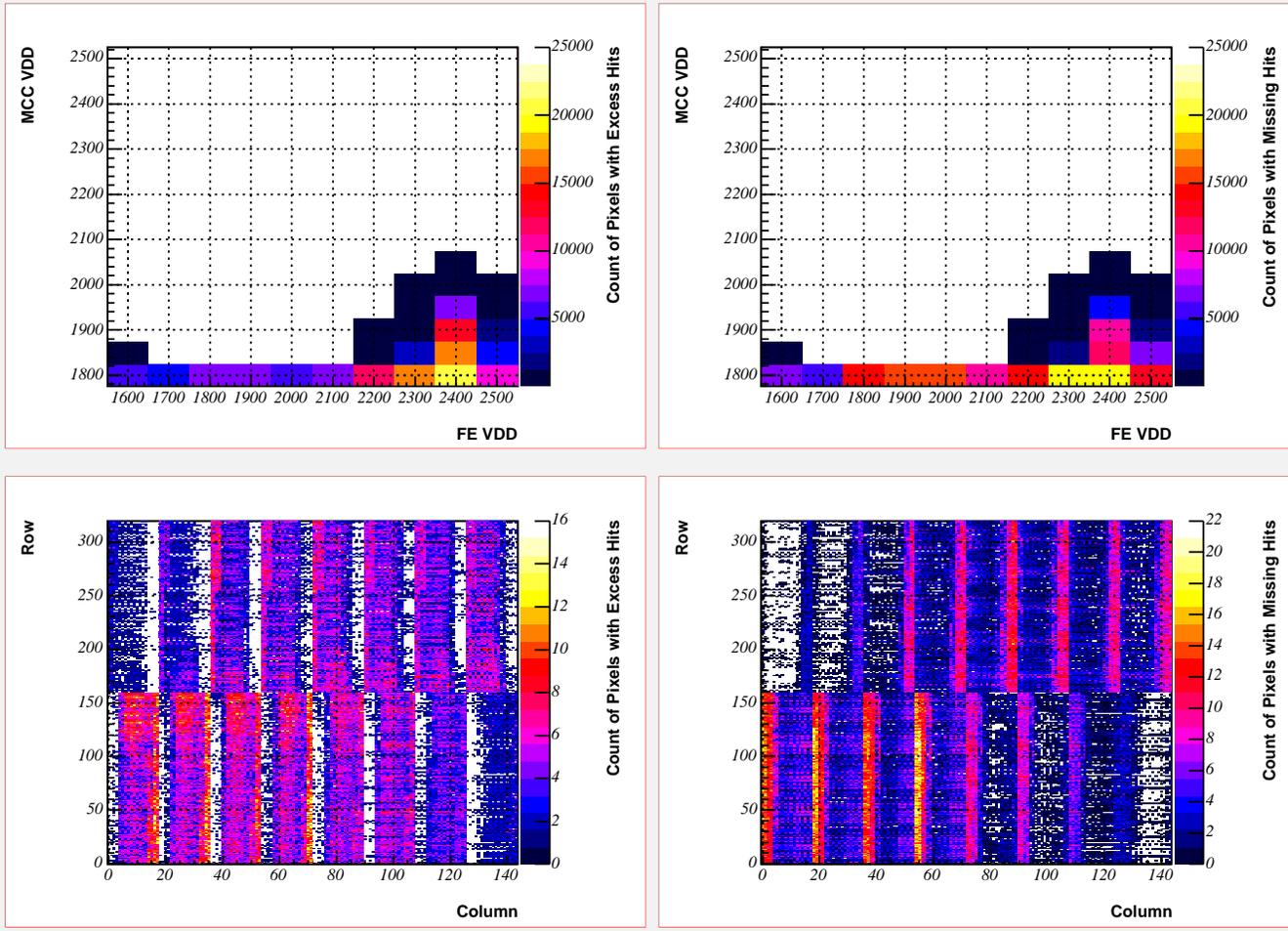
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 160Mbit/s



- Observe corruption for all FE_VDD if MCC_VDD less than 1.85V. For larger FE_VDD, must raise MCC_VDD as well to avoid problems. However, if assume FE_VDD = MCC_VDD, then no problems seen above 1.85V.

Scan of 100 events pixel for LBL_27 (160 Mb/s), pixel map:

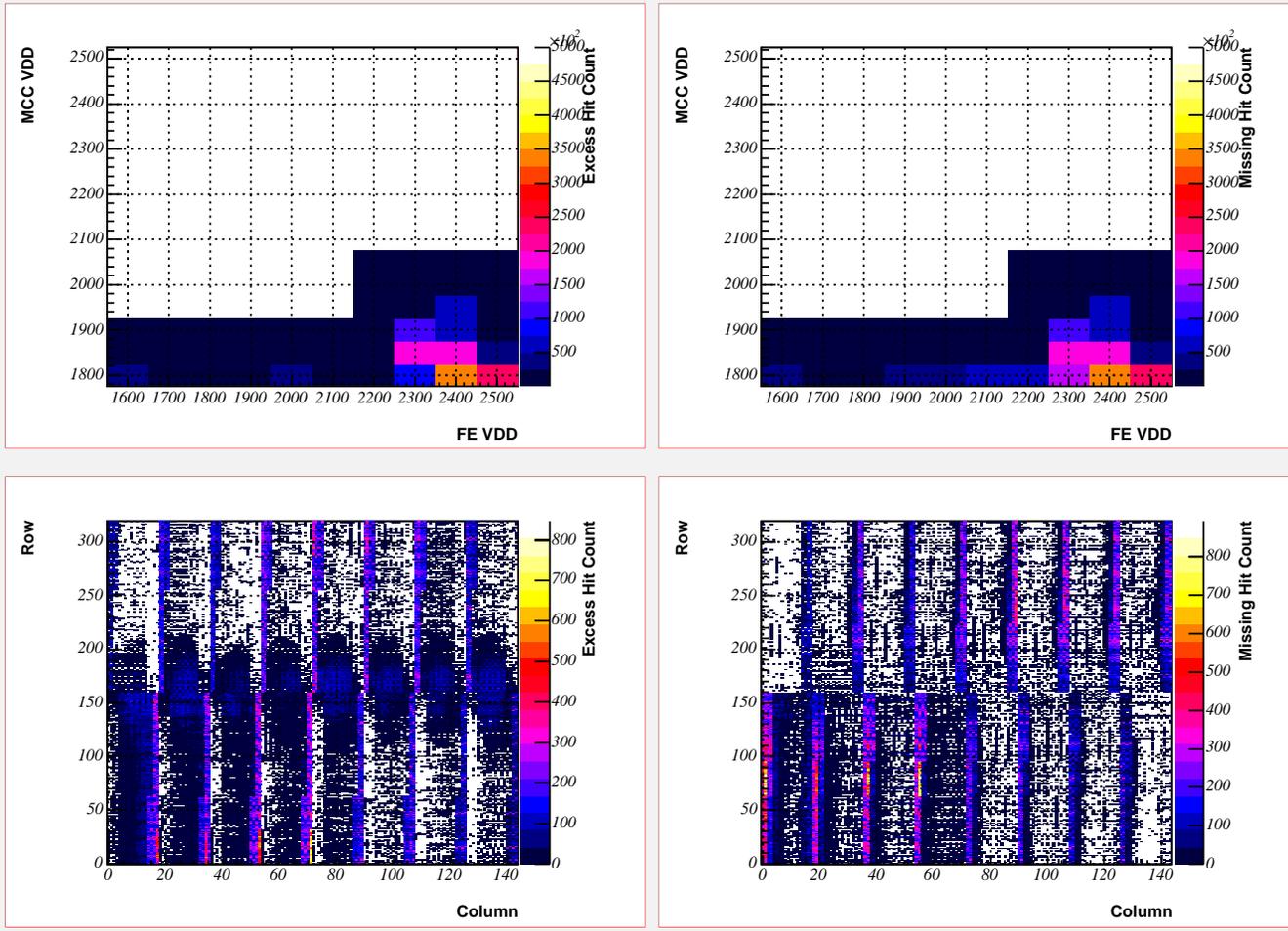
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 160Mbit/s 100 Events



- Previous plot summed all missing hits or excess hits for each pixel. This plot counts each pixel only once if it had missing or excess hits for a given LV setting. No significant new information, so only show hit counts for other studies.

Standard scan of 100 events per pixel for LBL_27 (40 Mb/s):

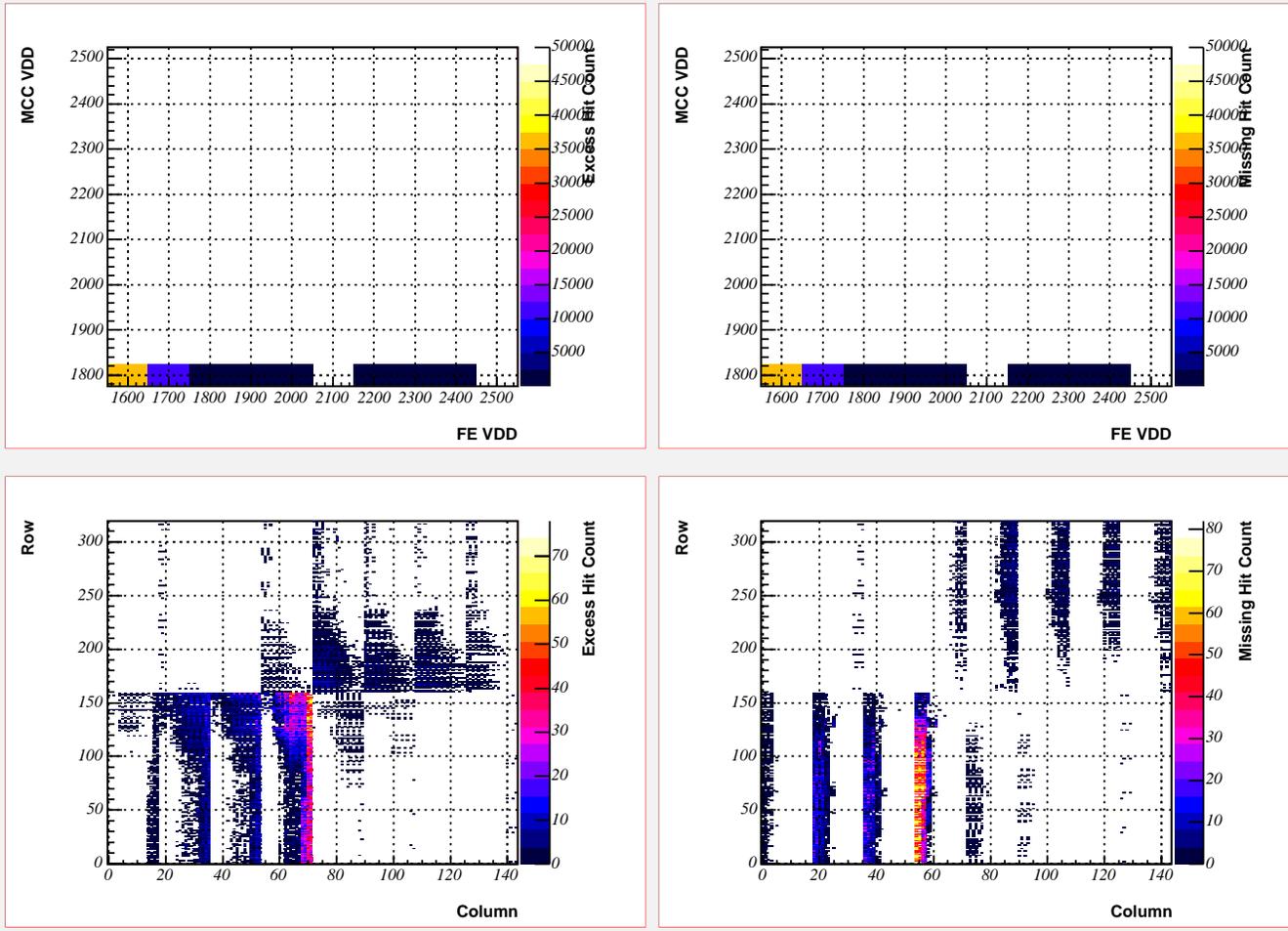
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 40Mbit/s



- Observe corruption for all FE_VDD if MCC_VDD less than 1.95V. For larger FE_VDD, must raise MCC_VDD as well to avoid problems. However, if assume FE_VDD = MCC_VDD, then no problems seen above 1.95V.

One FE scan of 100 events per pixel for LBL_27 (160 Mb/s):

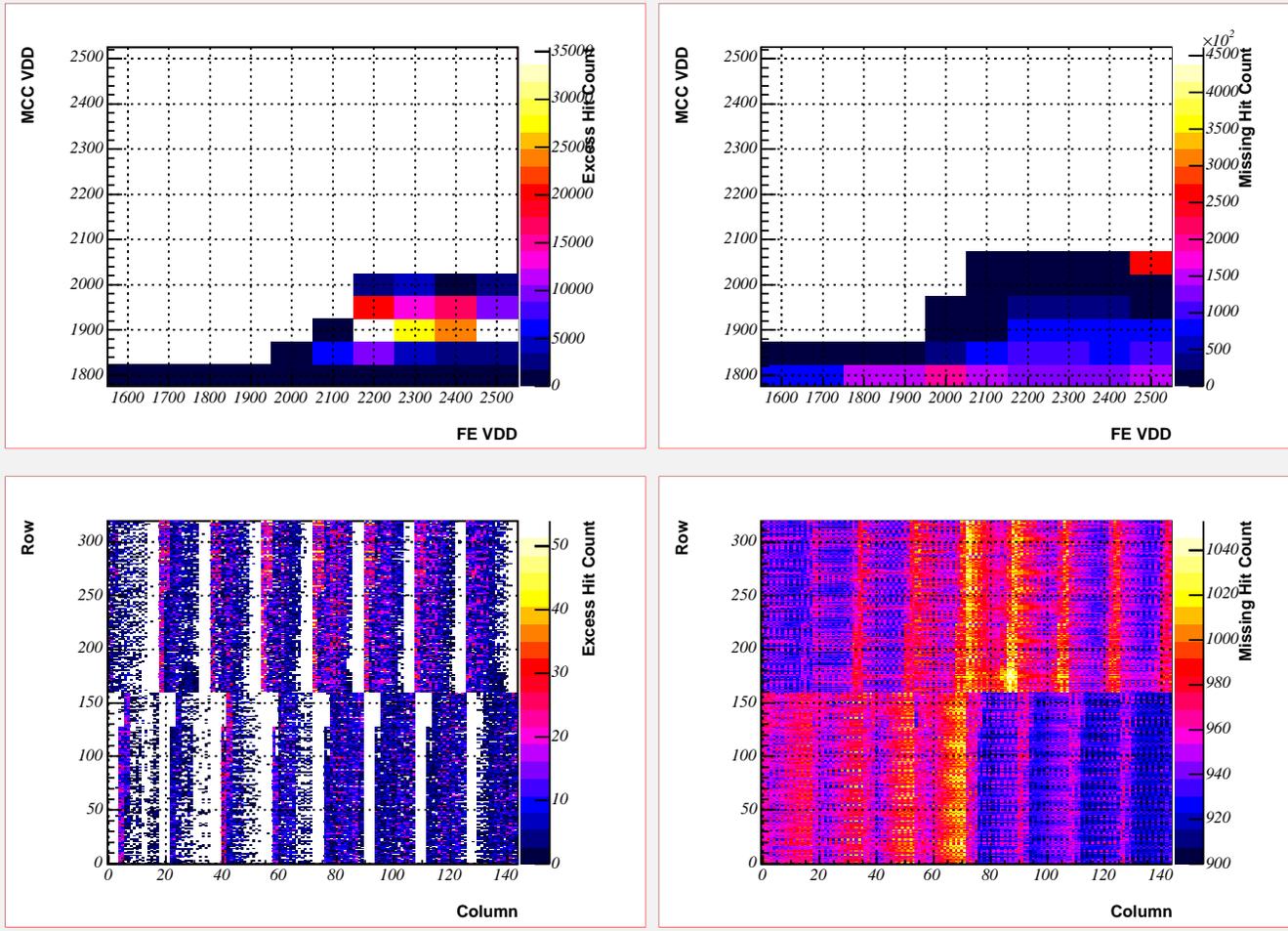
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 160Mbit/s One FE



- Observe corruption for most FE_VDD if MCC_VDD less than 1.85V. Problems seen at larger FE_VDD for concurrent scan have disappeared. Implies this was due to larger transients at larger FE_VDD, not timing shifts ?

Standard scan of 10K events for LBL_27 (160 Mb/s):

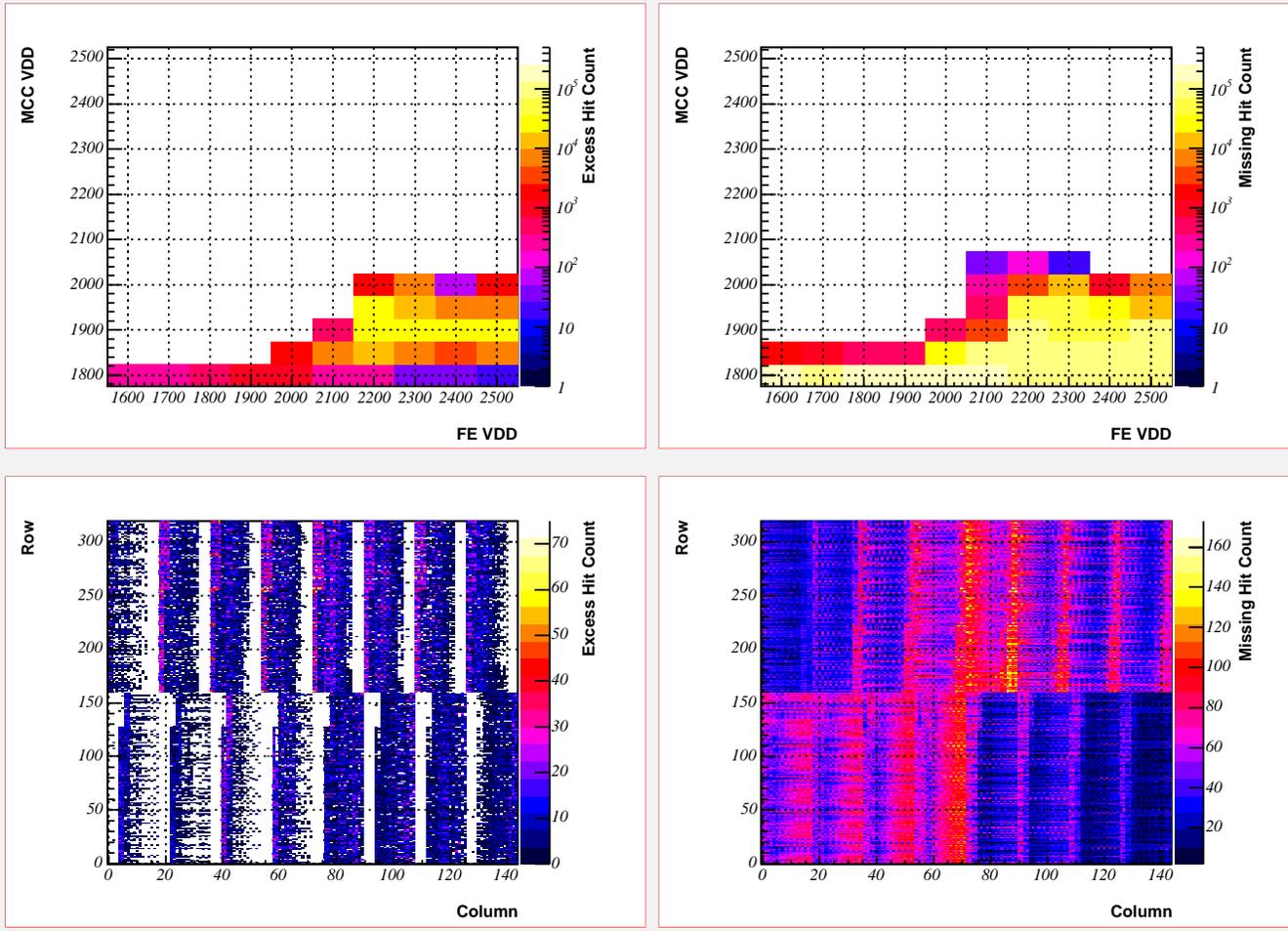
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 160Mbit/s 10K Events



- Observe corruption for all FE_VDD if MCC_VDD less than 1.90V. For larger FE_VDD, must raise MCC_VDD as well to avoid problems. However, if assume FE_VDD = MCC_VDD, then no problems seen above 1.90V.

Standard scan of 10K events for LBL_27 (160 Mb/s), log plot:

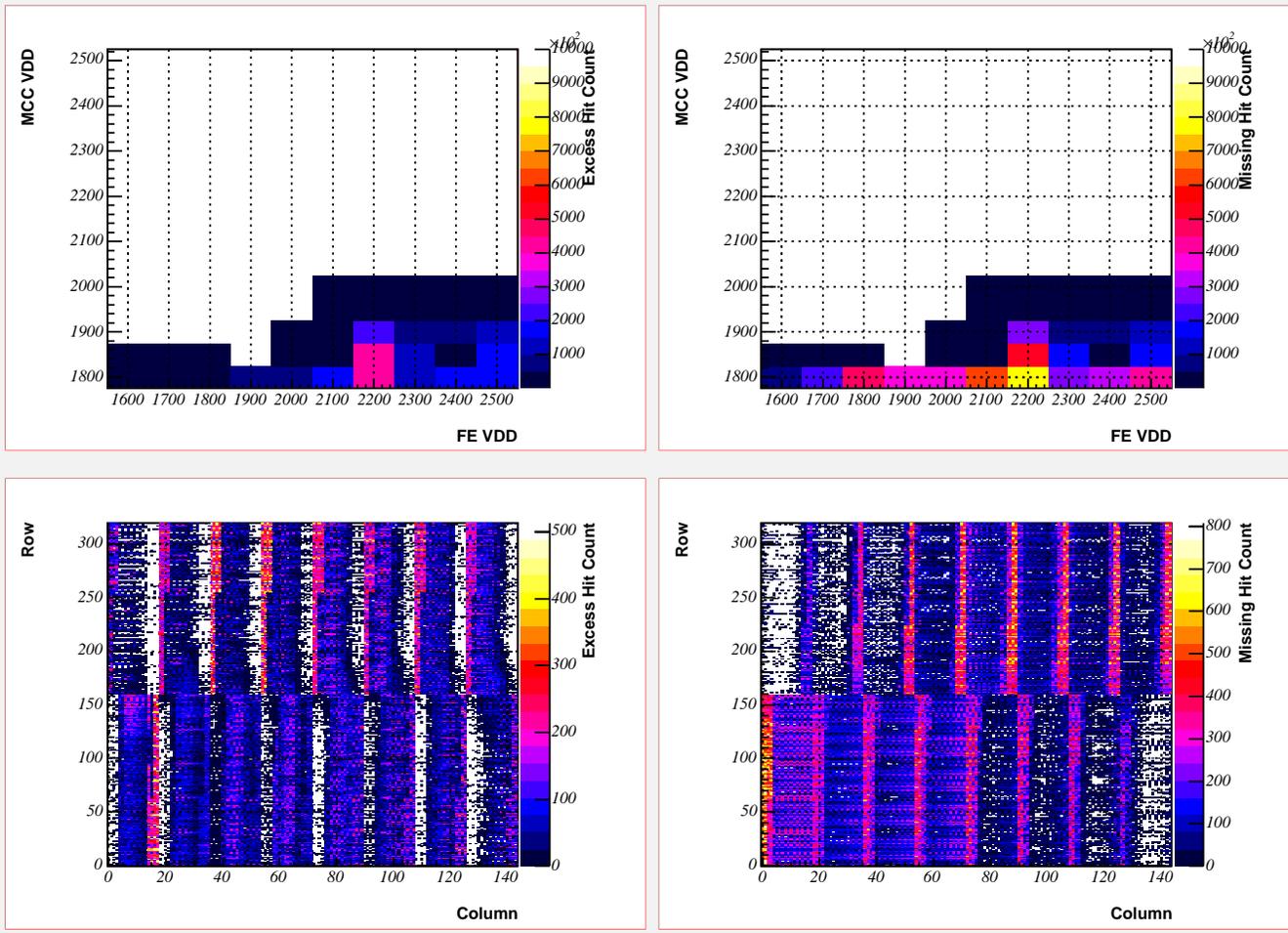
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 160Mbit/s 10K Events



- Still conclude that 1.90V is error free threshold for FE = MCC. No long tails seen with low counts.

Standard scan of 100 events for LBL_27 (160 Mb/s), 32_step:

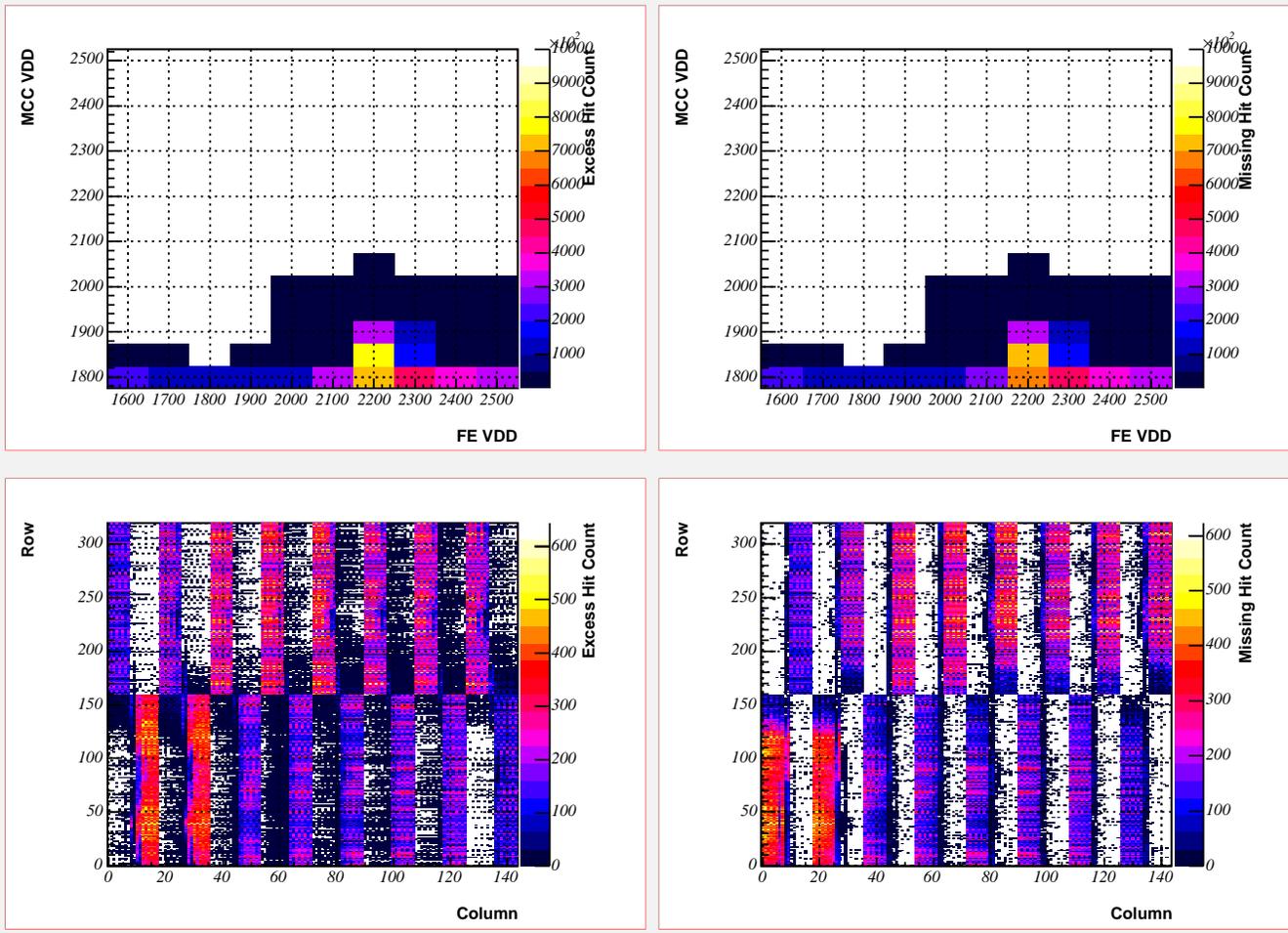
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 160Mbit/s 32 Step



- Observe corruption for all FE_VDD if MCC_VDD less than 1.90V. If assume FE_VDD = MCC_VDD, then no problems seen above 1.90V.

Standard scan of 10K events for LBL_27 (160 Mb/s), 80_step:

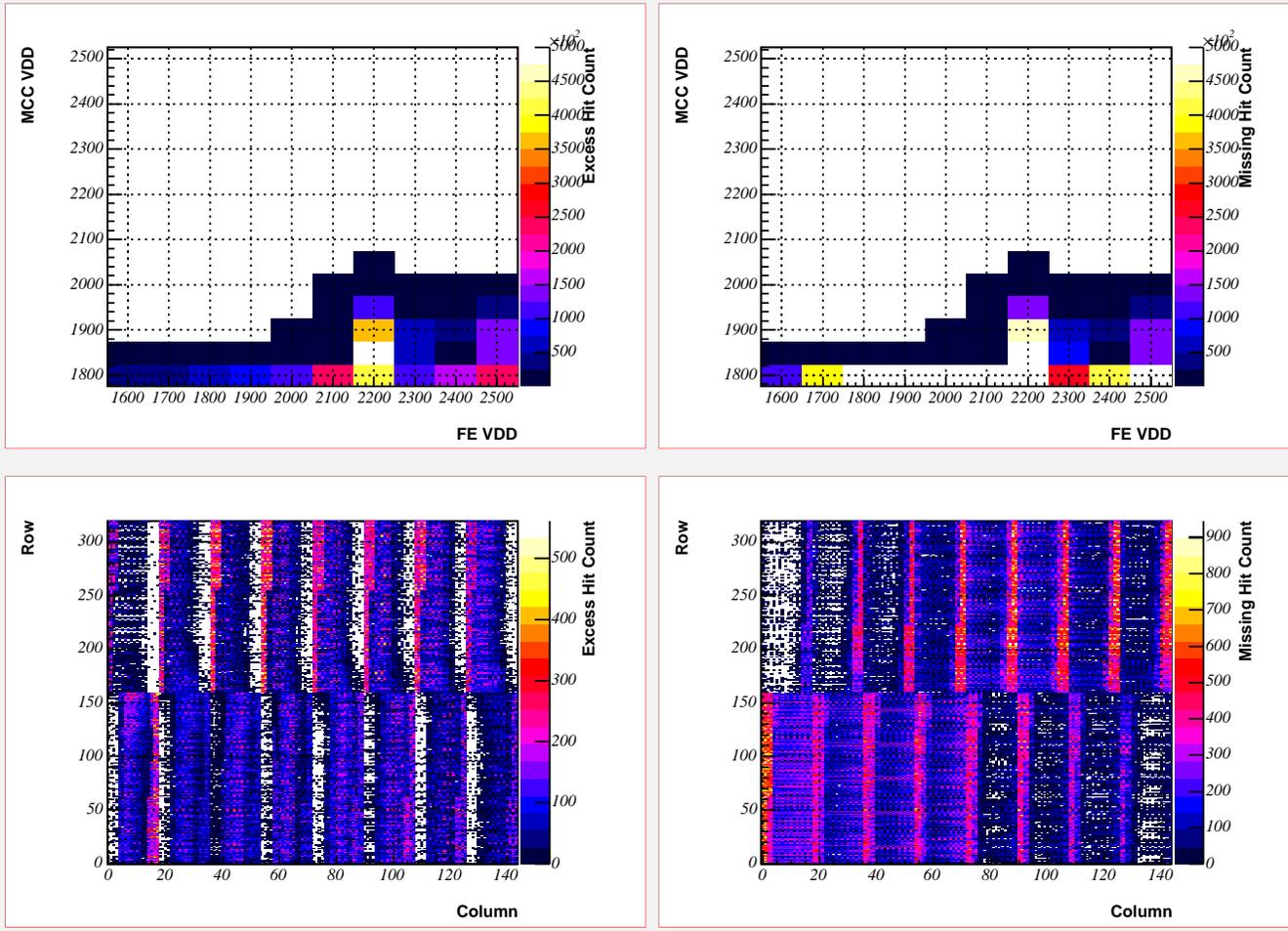
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), 160Mbit/s 80 Step



- Do not observe any significant reduction in error rate. Suggests that error rate scales with activity inside MCC not activity in FE (one FE had much lower error rate, and much lower activity in both).

Standard scan of 10K events for LBL_27 (Dual 80Mbit):

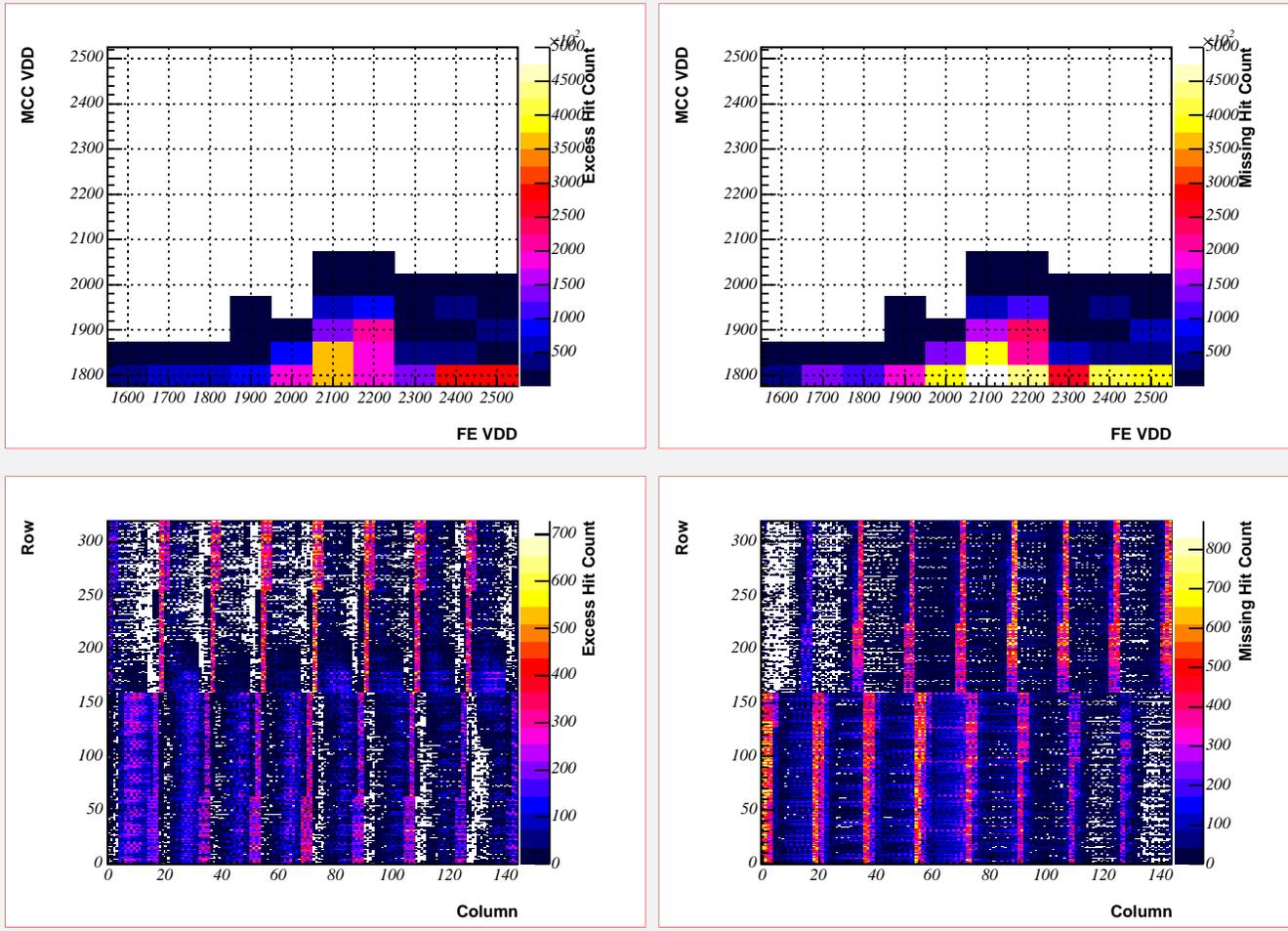
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), Dual-80 100 Events



- Reference scan to compare all 4 bandwidths using TPLL V15 firmware.
- Error-free above 1.90V for FE = MCC VDD.

Standard scan of 10K events for LBL_27 (Dual 40Mbit):

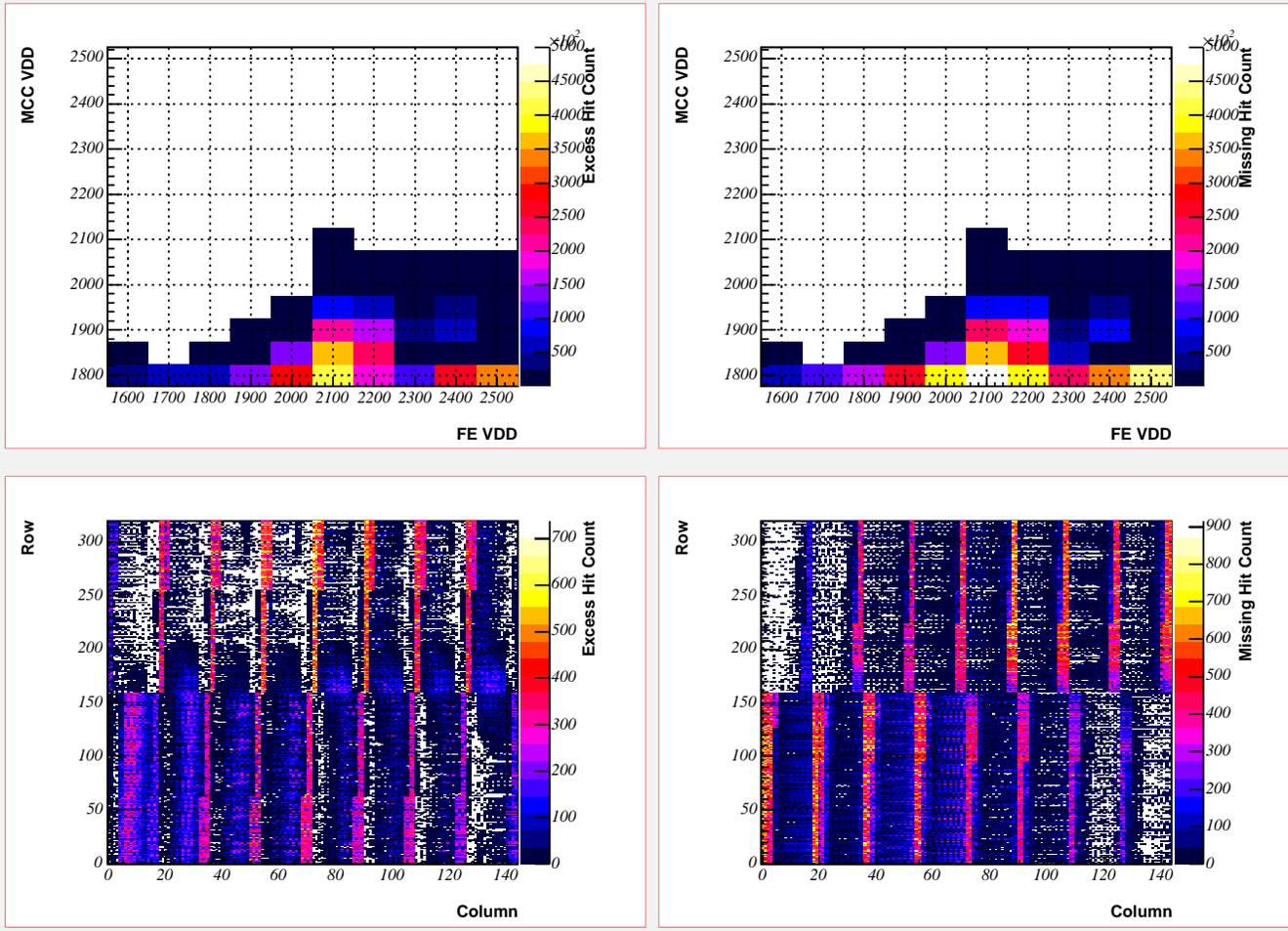
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), Dual-40 100 Events



- Observed error rate is slightly worse at MCC_VDD=1.90V than for dual-80 Mbit mode. Error-free above 2.00V for FE = MCC VDD.

Standard scan of 10K events for LBL_27 (Single 80Mbit):

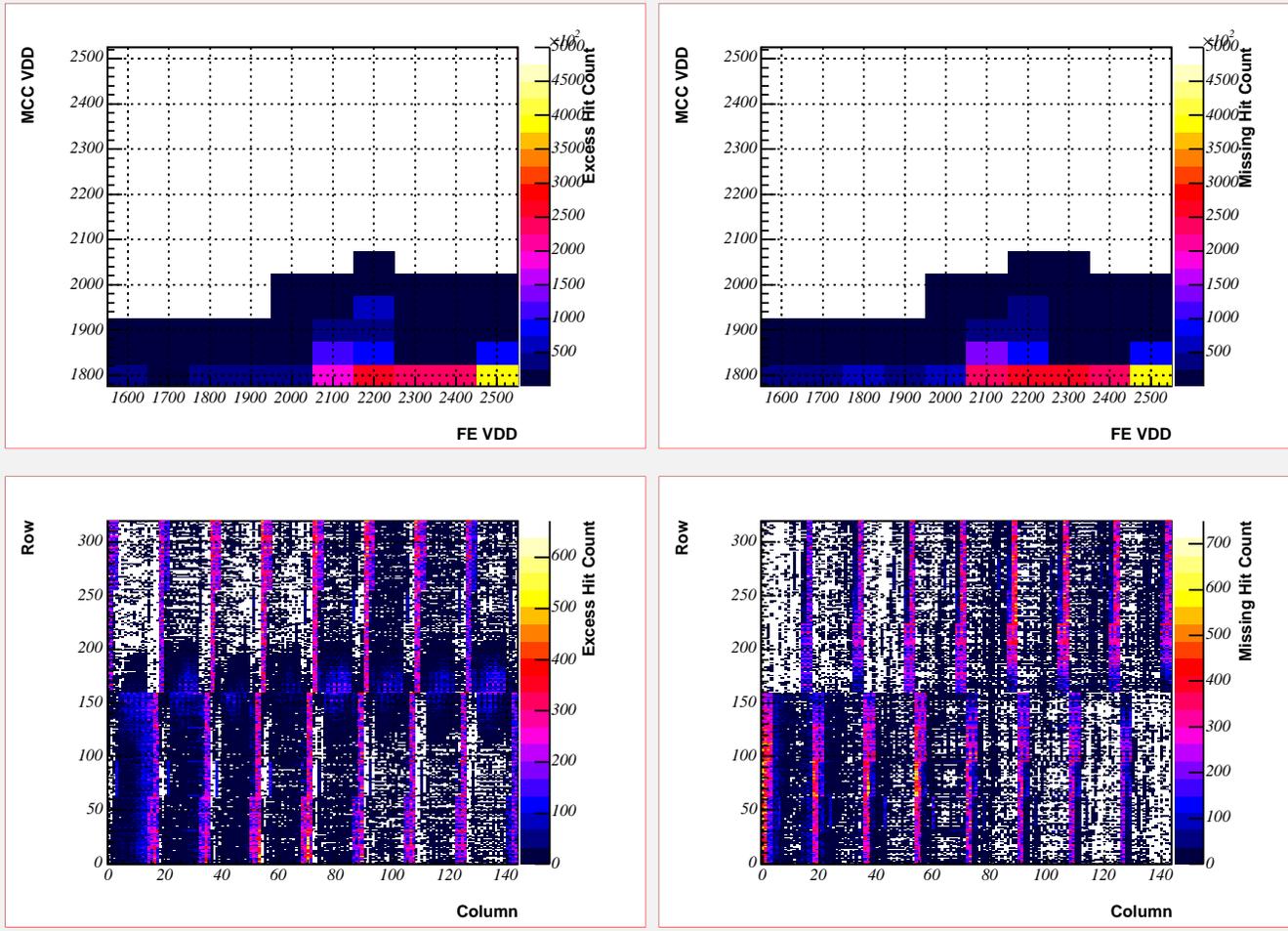
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), Single-80 100 Events



- Observed error rate is slightly worse at MCC_VDD=1.90V than for dual-80 Mbit mode. Error-free only above 2.15V for FE = MCC VDD due to single scan at 2.1V.

Standard scan of 10K events for LBL_27 (Single 40Mbit):

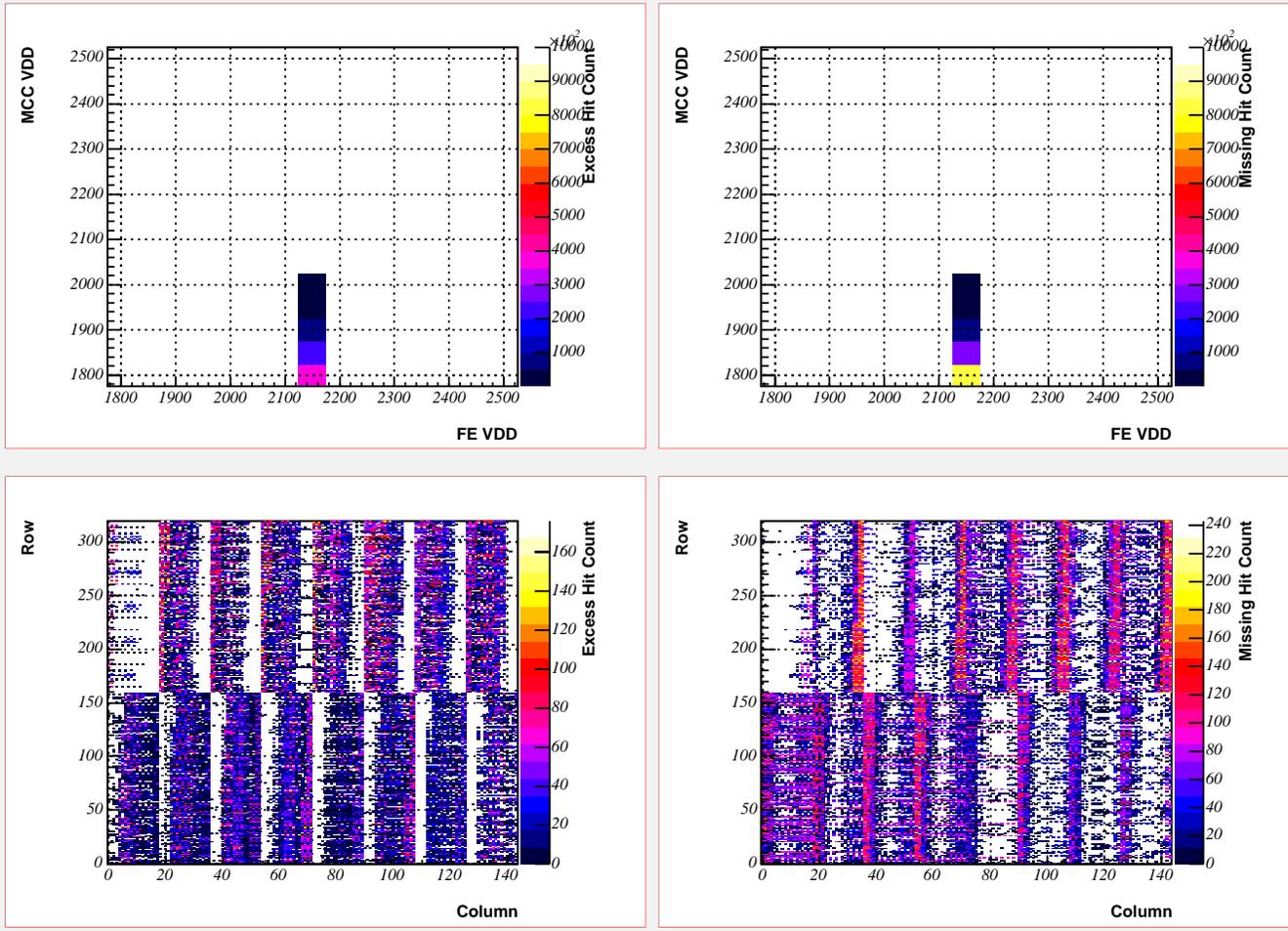
LBL_27 VDD Scan, FE VDD=1.6-2.5V (10 steps), MCC VDD=1.8-2.5V (15 steps), Single-40 100 Events



- Observed error rate is worse at lower FE VDD than for single-80 Mbit mode, but better at higher FE VDD. Error-free above 2.00V for FE = MCC VDD.

Scan of 100 events for LBL_27 with regulators (160 Mb/s):

LBL_27 VDD Scan, FE Reg VDD=2.15V, MCC VDD=1.8-2.5V (15 steps), 160Mbit/s 100 Events



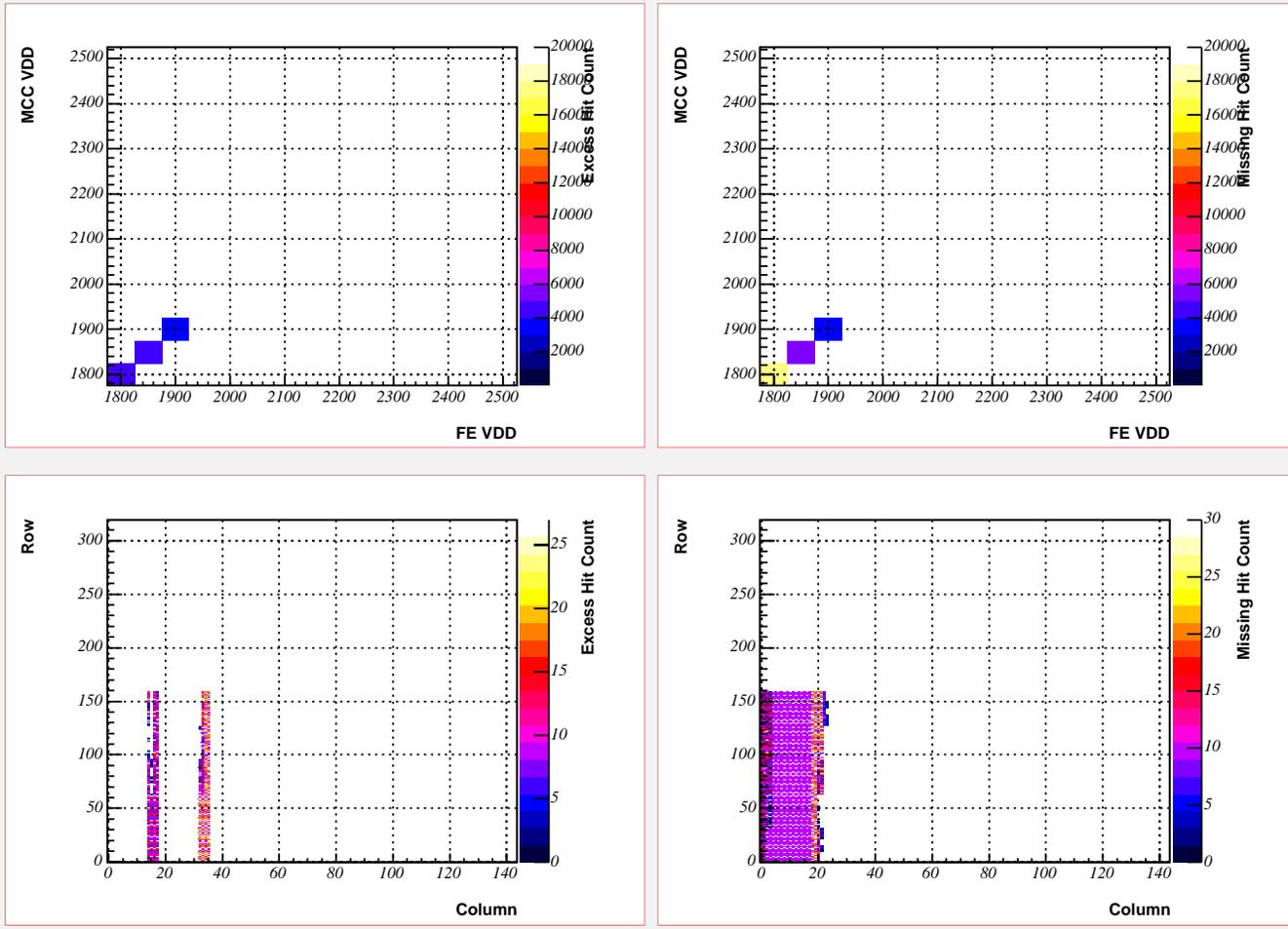
- Observe corruption for all FE_VDD if MCC_VDD less than 1.85V. Previously observed clean operation above 1.85V - 1.95V, and here it is clean above 2.05V. This implies a shift of about 100-150mV in the error threshold.

Measurements of error rates using 1D VDD scans for LBL_26:

- Use obscure TDAQ features to scan MCC_VDD from 1.8V to 2.5V, with a digital inject scan at each voltage point (15 scans). Typical scans used 100 events per pixel, some high statistics scans were made with 10K events per pixel.
- No modifications made to standard Flex connectivity.
- Study impact of additional, local ceramic decoupling. Options available commercially now as possible replacement capacitors:
 - Size 0402 1 μ F X5R dielectric, 6.3V rating.
 - Size 0603 1 μ F X5R dielectric, 10V rating
 - Size 0603 4.7 μ F X5R dielectric, 6.3V rating
- For production, would only consider 10V capacitors, so would need to upgrade 0402 capacitors to 0603 capacitors.
- For lab testing, modified module with addition of 1 μ F 0402 caps on top of existing three MCC decoupling capacitors.

Standard scan of 10K events per pixel for LBL_26 (160 Mb/s):

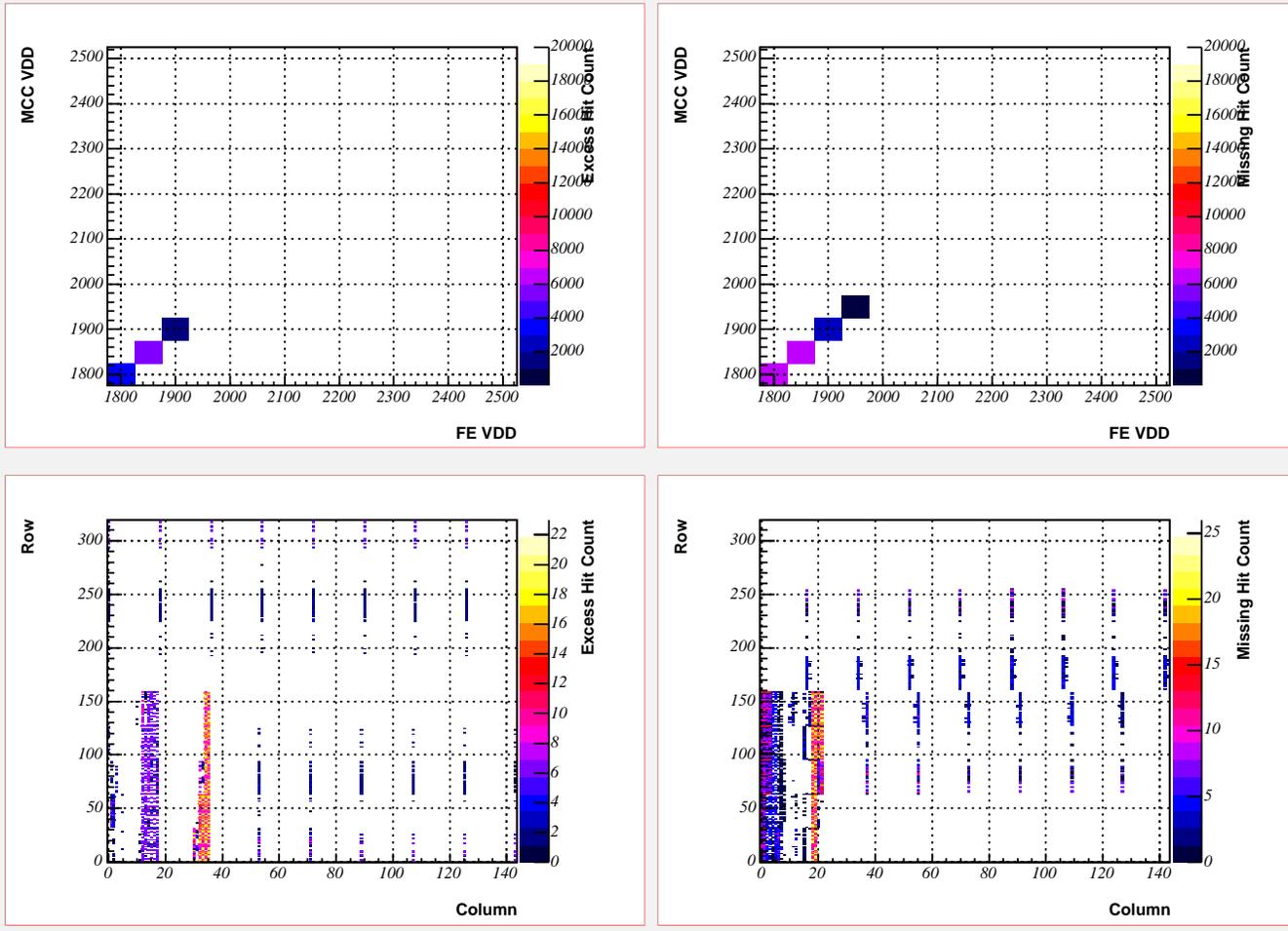
LBL_26 VDD Scan, FE+MCC VDD=1.8-2.5V (15 steps), 160Mbit/s, 10K Events



- Observe corruption if FE_VDD and MCC_VDD (connected together) are less than 1.95V. Don't know whether the higher error threshold (compared to LBL_27 module) is due to different MCC or due to connection of FE_VDD and MCC_VDD.

Standard scan of 10K events per pixel for LBL_26 (40 Mb/s):

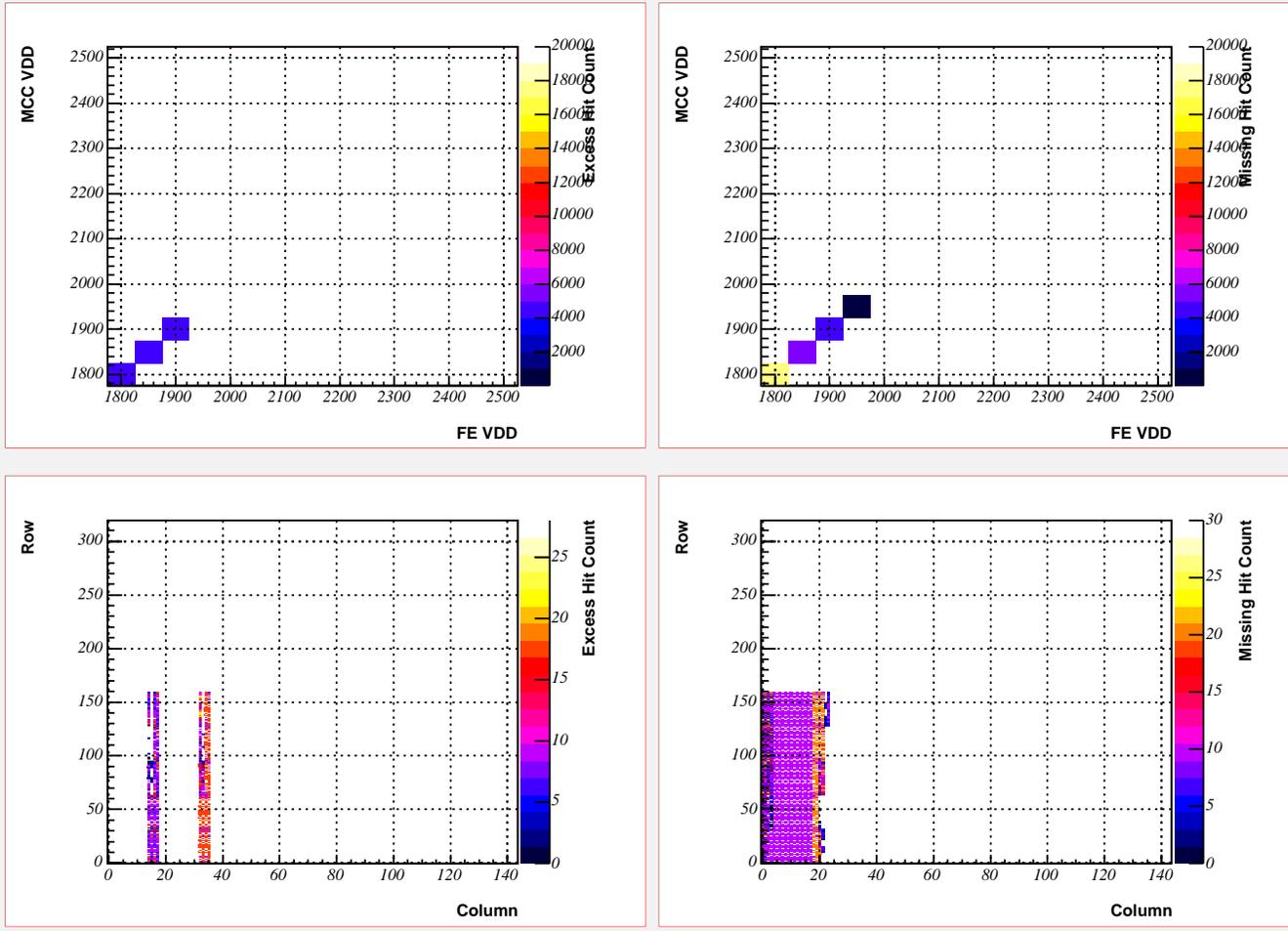
LBL_26 VDD Scan, FE+MCC VDD=1.8-2.5V (15 steps), 40Mbit/s, 10K Events



- Observe corruption if FE_VDD and MCC_VDD (connected together) are less than 2.00V. Errors are now distributed among all FE chips, instead of chip 0 and 1 only.

Scan 10K events per pixel for LBL_26 (160 Mb/s), new caps:

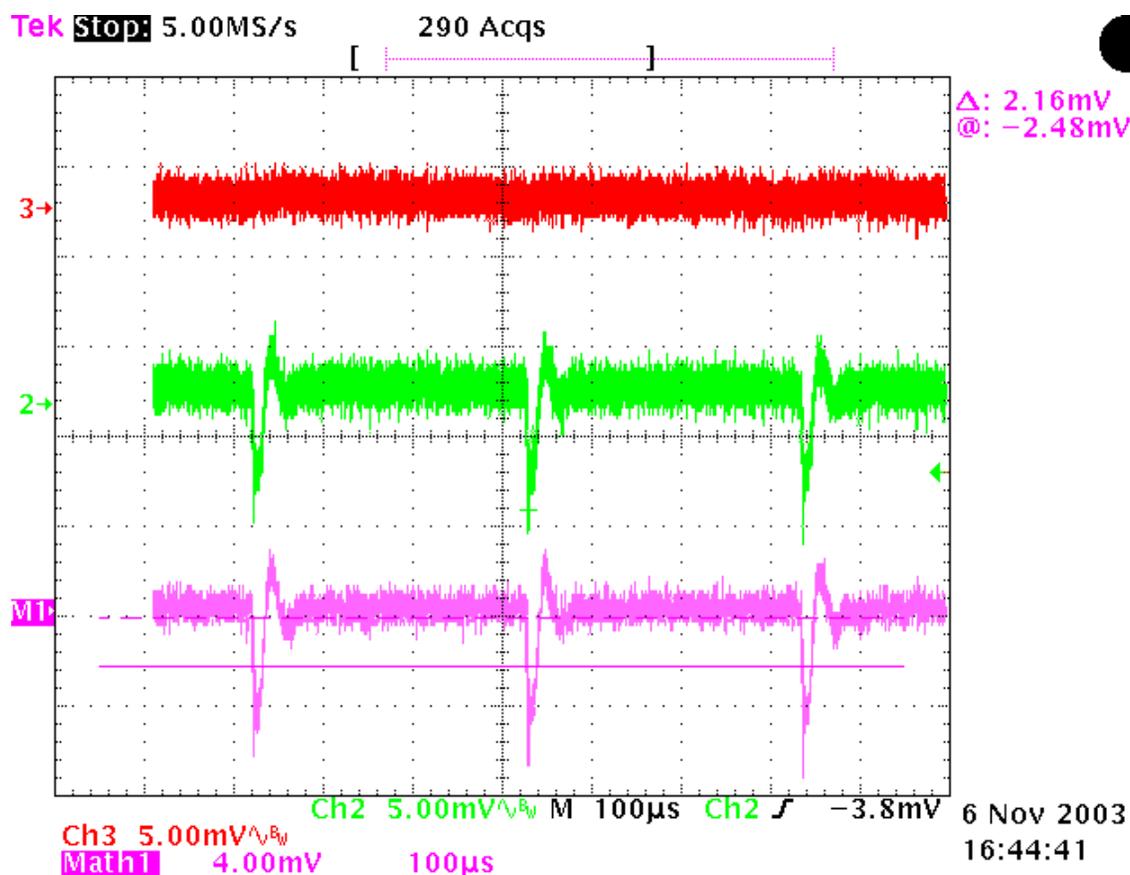
LBL_26 VDD Scan, FE + MCC VDD=1.8-2.5V (15 steps), 160Mbit/s, 10K Events, New Caps



- Observe no noticeable improvement in data corruption thresholds compared to standard case with three $0.1\mu\text{F}$ caps instead of three $1\mu\text{F}$ caps.

Measurements of VDD transients:

- Pico-probes placed on 0402 cap solder pads. Use MCC cap towards center of module for MCC_VDD, use VDD cap in center of H-bus for FE_VDD.
- Significant activity is seen on FE_VDD. Use LBL_27 (split-VDD) module for these studies. Individual picoprobes referenced to DGND on module, so transient appears only on VDD (both VDD and DGND should be symmetric).
- Example from 160Mbit/s digital inject scan (300 μ s trigger interval):

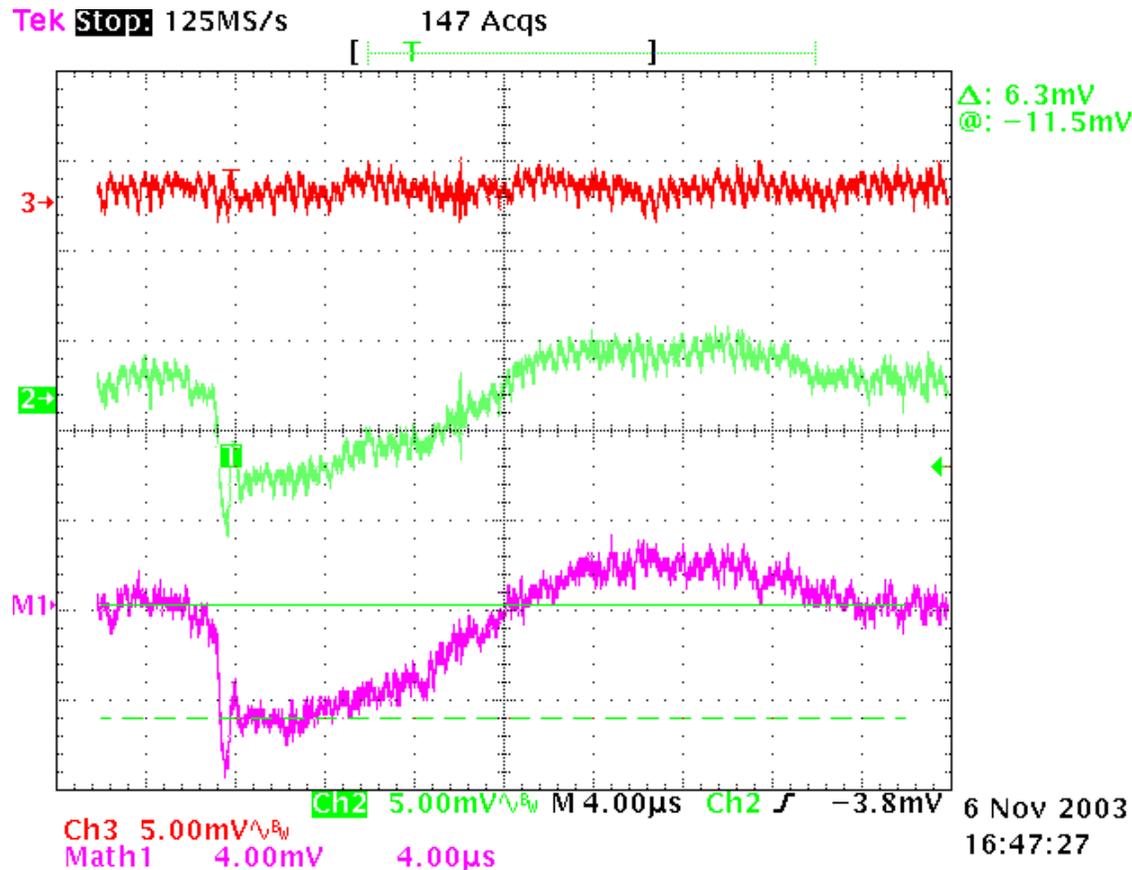


Upper trace is DGND

Middle trace is VDD

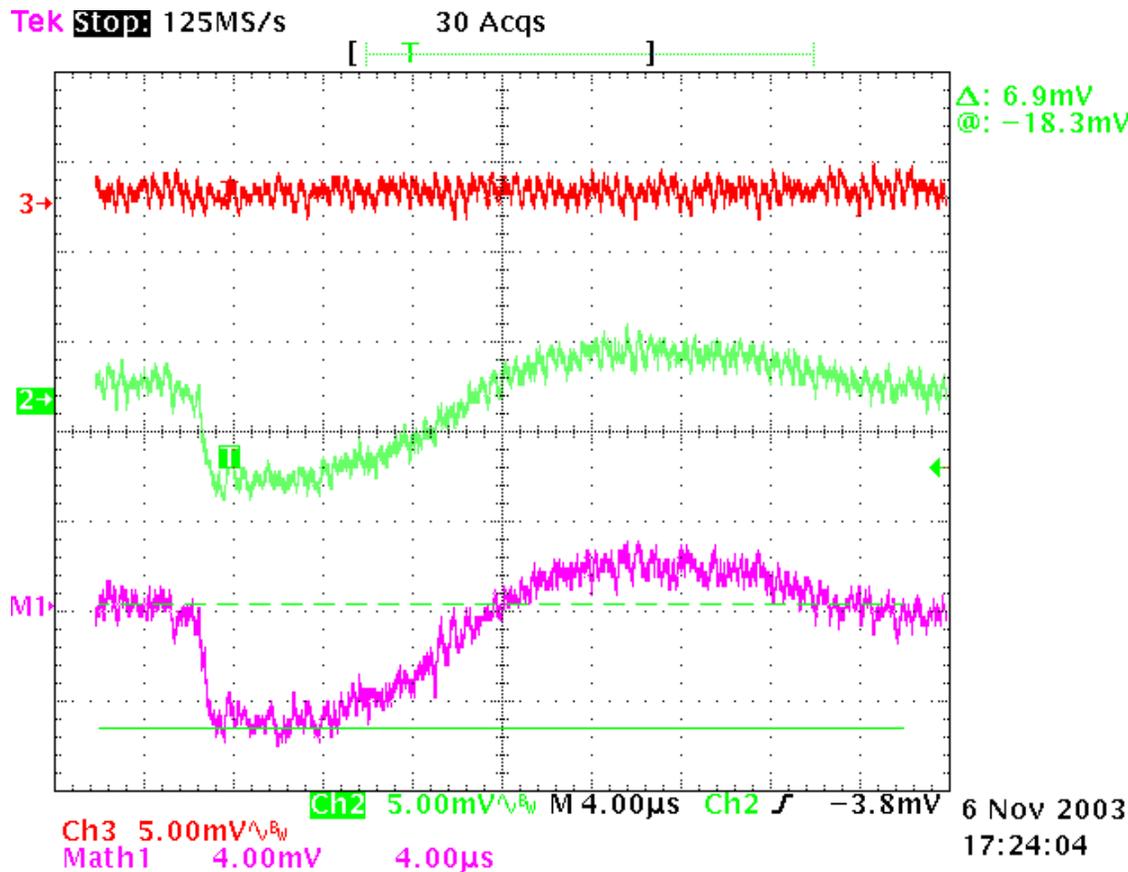
Bottom trace is VDD-DGND

- Zoom into transient shows large initial spike associated with hit transfer down column pair into EOC buffers (here shown for CEU=40MHz). Hit transfer takes roughly 500ns for 10 hits in each column pair.
- Additional activity seen as hits are stored in EOC buffers, and 40MHz TSC comparator begins operating. Once hits are triggered, this comparator stops running. Latency is 6.4μs minus 50 TOT counts, or 5.2μs.
- Amplitude of transient is about 50mV (picoprobes are 10:1):



Upper trace is DGND
 Middle trace is VDD
 Bottom trace is VDD-DGND

- Zoom into transient shows large initial spike associated with hit transfer down column pair into EOC buffers (here shown for CEU=20MHz). Hit transfer takes roughly 1000ns for 10 hits in each column pair.
- Additional activity seen as hits are stored in EOC buffers, and 40MHz TSC comparator begins operating. Once hits are triggered, this comparator stops running. Latency is 6.4μs minus 50 TOT counts, or 5.2μs.
- Amplitude of transient is about 50mV (picoprobes are 10:1):

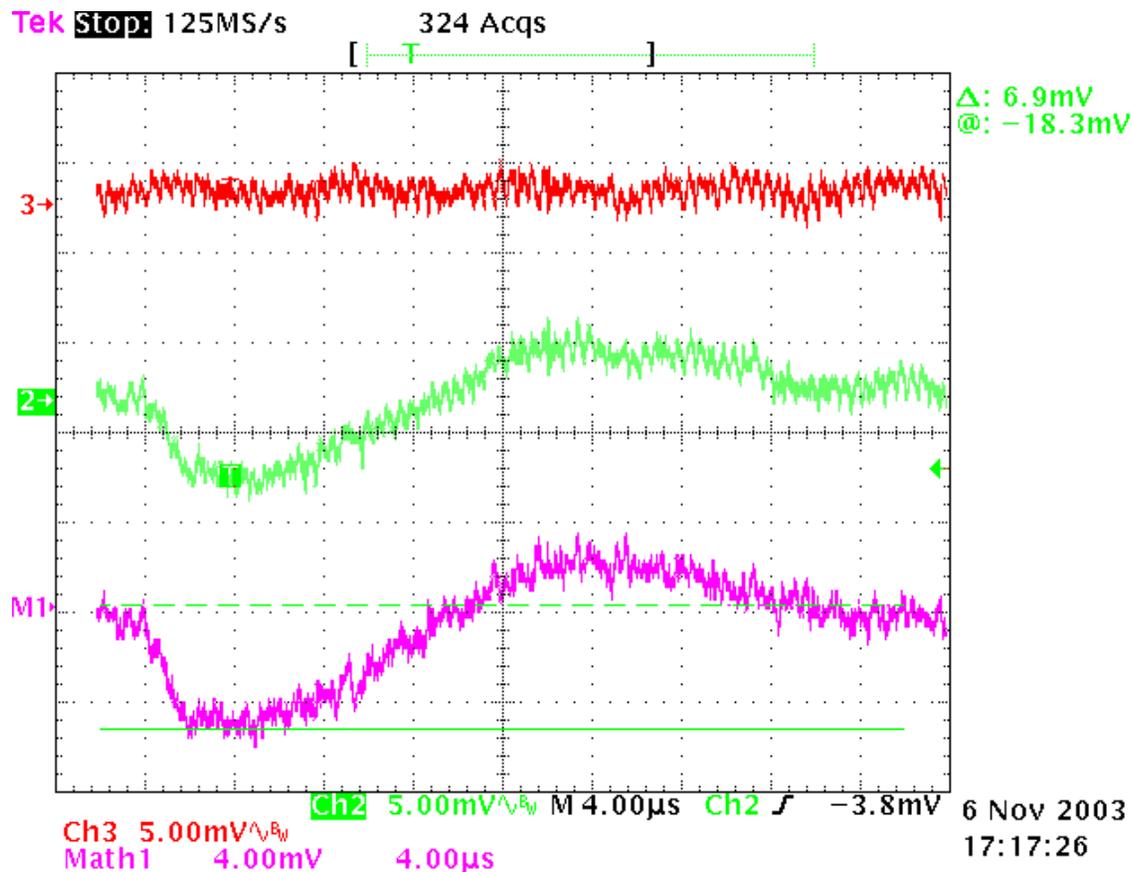


Upper trace is DGND

Middle trace is VDD

Bottom trace is VDD-DGND

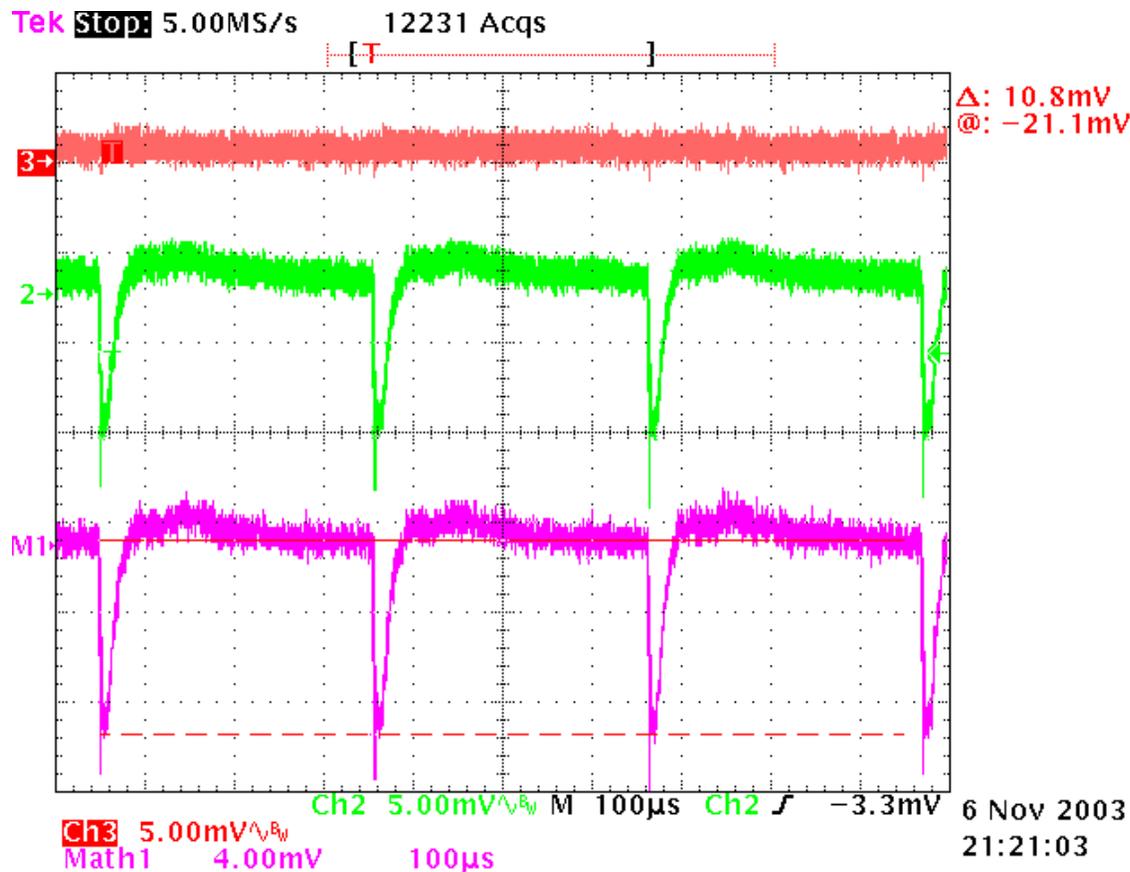
- Zoom into transient shows large initial spike associated with hit transfer down column pair into EOC buffers (here shown for CEU=10MHz). Hit transfer takes roughly 2000ns for 10 hits in each column pair.
- Additional activity seen as hits are stored in EOC buffers, and 40MHz TSC comparator begins operating. Once hits are triggered, this comparator stops running. Latency is 6.4μs minus 50 TOT counts, or 5.2μs.
- Amplitude of transient is about 50mV (picoprobes are 10:1):



Upper trace is DGND
 Middle trace is VDD
 Bottom trace is VDD-DGND

Measurements of VDD transients with regulators:

- Measure identical waveforms using old (not current compensating) regulator board, and 12m long Type 2 LV cable made from Raydex cable samples.
- Immediately see that transients are about twice as large as for Agilent remote sense operation with short remote sense cable. Recovery is more gradual with little overshoot.
- Example from 160Mbit/s digital inject scan (300 μ s trigger interval):

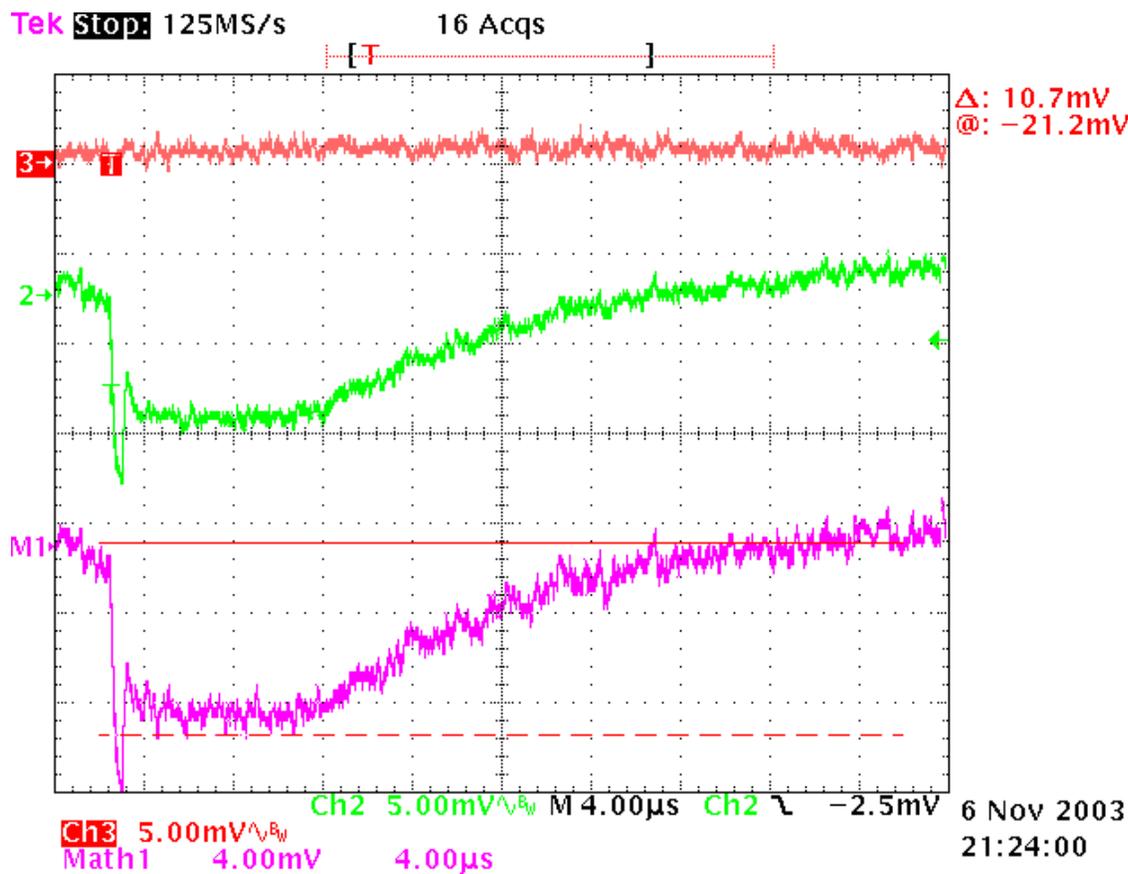


Upper trace is DGND

Middle trace is VDD

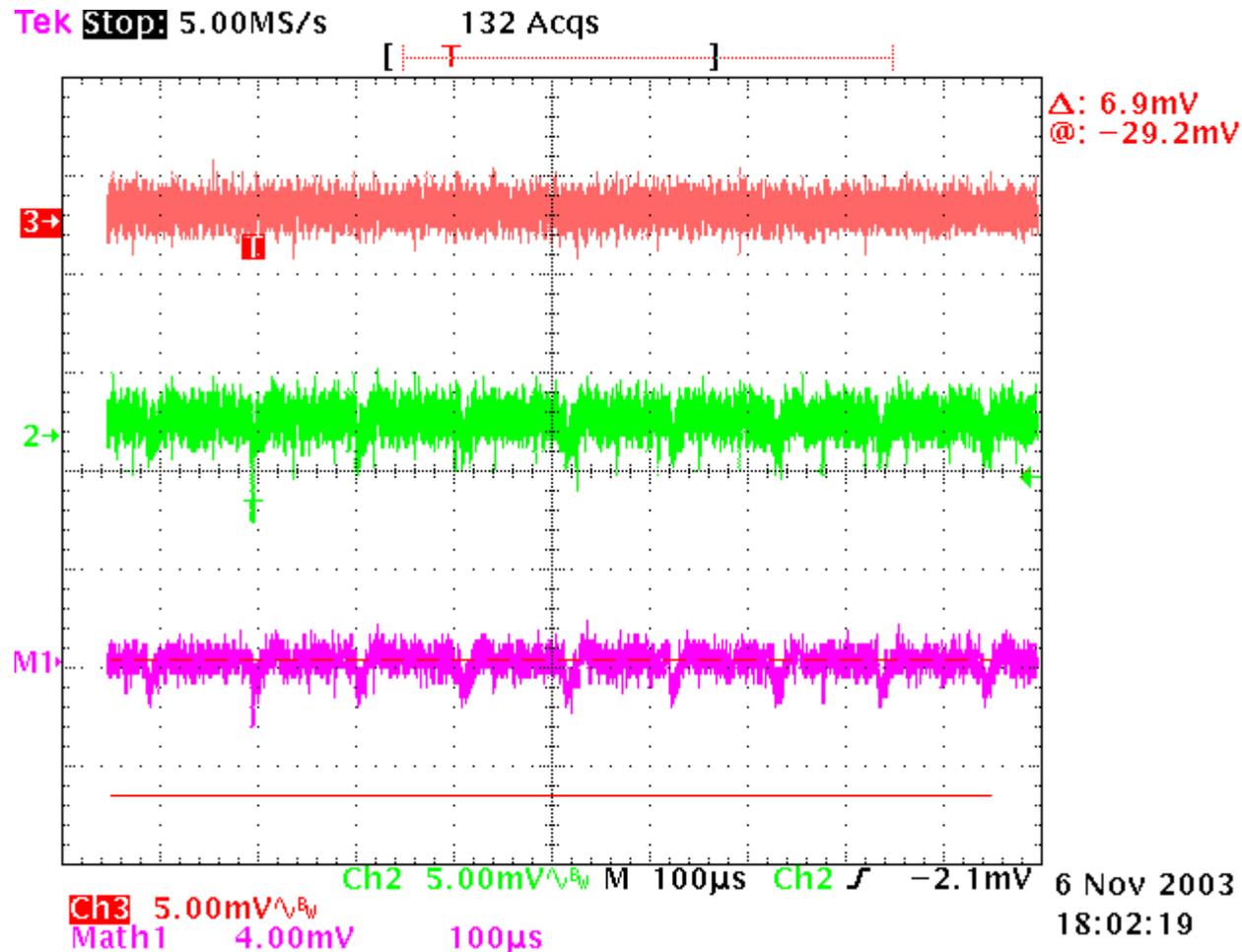
Bottom trace is VDD-DGND

- Zoom into transient shows large initial spike associated with hit transfer down column pair into EOC buffers (here shown for CEU=40MHz). Hit transfer takes roughly 500ns for 10 hits in each column pair.
- Additional activity seen as hits are stored in EOC buffers, and 40MHz TSC comparator begins operating. Latency is 6.4 μ s minus 50 TOT counts, or 5.2 μ s.
- Amplitude of transient is about 100mV (picoprobes are 10:1):



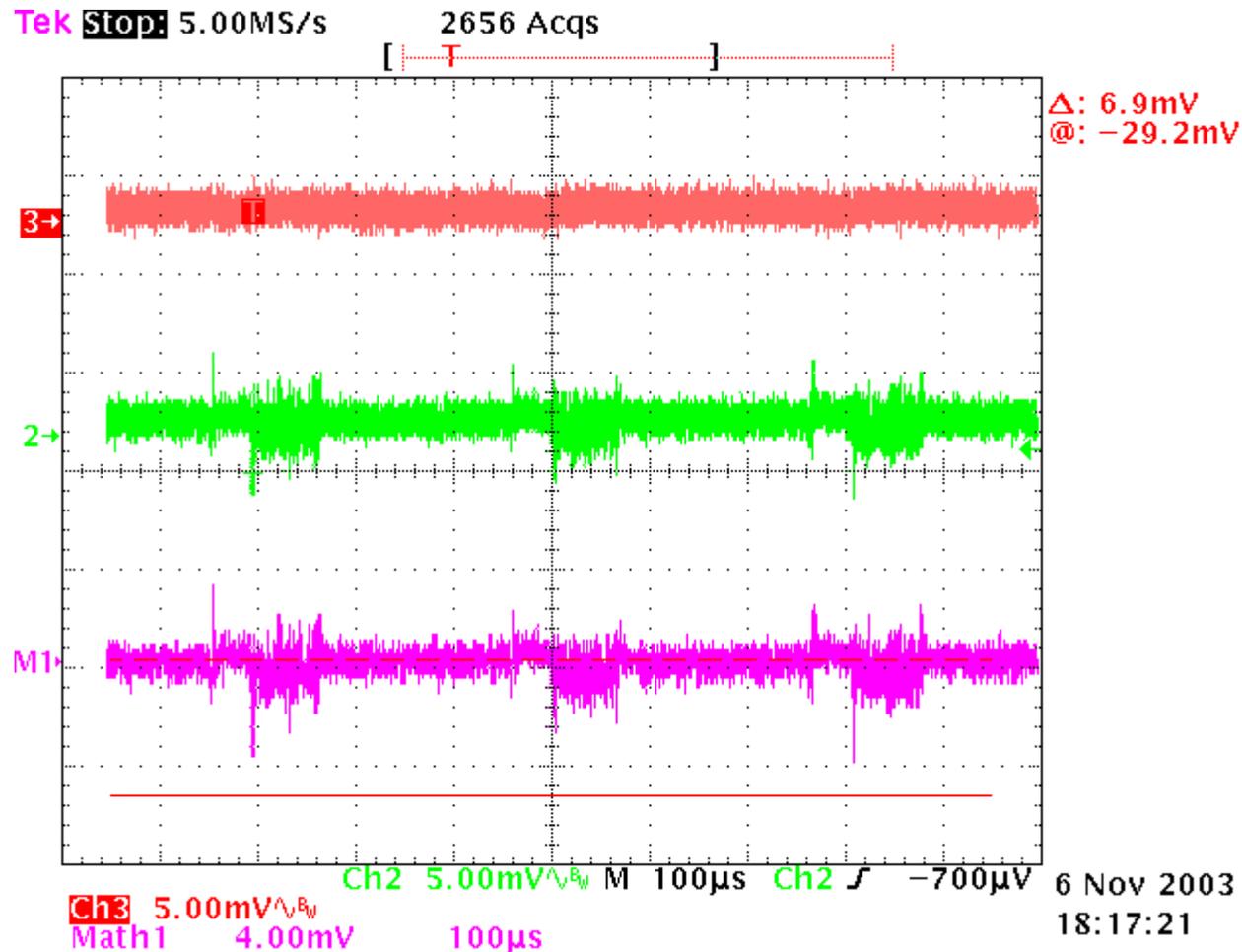
Upper trace is DGND
Middle trace is VDD
Bottom trace is VDD-DGND

Measurement of VDD transients for single FE readout case:



- No significant transients observed in this case.
- Note however that ALL FE transients have largely recovered by the time the critical FE to MCC data transfer occurs, so they should not have a large effect on the data integrity (or the instantaneous supply voltage at the MCC).

Measurement of VDD transients for MCC during scan:



- No significant transients observed in this case.
- Note however that this is being checked at the decoupling capacitor. Transients on MCC pads (and internal power busses) could be larger. Note also that these transients DO occur during the critical FE to MCC data transfer period.

Summary

- For measurements at room temperature or slightly above, operated with local remote sensing in the lab, always observe data corruption for MCC VDD of about 1.85V and below when operating FE-I2 modules at 160Mbit readout. For some modules, this error threshold is higher by 100-200mV.
- For 40Mbit data transmission, observe about 100mV higher VDD required for error-free operation. This is true even if 40Mbit and 160Mbit scans are performed using same trigger interval. Surprising, because no significant current transients are expected during data transmission (LVDS drivers are steered current devices).
- For modules operated with realistic services, including 140m Type 3 cable, 12m Type 2 cable and regulator board, observe higher error threshold by 100-150mV.
- Observe only minimal MCC error threshold when operating in one FE hit injection mode instead of concurrent injection. This emphasizes that problem is related to total digital activity on module. Scans with 80_step instead of 32_step mask (36 hits per FE instead of 90 hits per FE) show no difference, suggesting that even reduced activity in all FE (or all MCC receivers) will raise error threshold.
- Observe corresponding transients on Flex during these scans. Amplitude of transients is significantly large with realistic regulator + Type 2 cable setup, providing a possible explanation for higher error threshold for regulator case. Note however that transients recover before MCC data processing begins.

- Digital inject scans are very atypical because they inject roughly the maximum number of bufferable hits into a module. The 1440 hits have identical LE and TE timing, so all hits travel down the column pair at the same time, causing maximum VDD transients on the module.
- Have been somewhat surprised at the significant change in the magnitude of the local transients on the module when switching from local remote-sense powering to operation with realistic services, despite the presence of 10 μ F ceramic at the power entrance on the Flex.
- This suggests that the problem cannot be easily improved by adding still more capacitance. However, will continue to study whether adding very large ceramics at PP0 for example could have a beneficial effect.
- Have added three more decoupling caps on one module, close to the MCC, to provide 3 μ F of local decoupling, and this did not change the error threshold.
- Several options exist for adding more capacitance to the present modules. If we want to preserve our present conservative 10V rating on all on-module decoupling, then the only option is to add 0603 1 μ F caps by hand on top of existing 0.1 μ F 0402 decoupling caps. This is painful, but could be done if needed.

Conclude:

- There is a serious problem in the MCC with a VDD threshold under ideal conditions of about 1.8-1.9V, depending on the output bandwidth selected.
- The voltage range over which this problem can affect module operation depends strongly on the power supply configuration. The present low mass service scheme with distant regulators clearly makes the situation worse.
- Our present method of studying this problem, using concurrent digital scans and injecting the maximum number of hits possible, enhances the problem further. It is less clear what the operational implications of this problem would be. However, we can expect significant, peculiar time structure in LHC beam conditions, which will be reflected in reduced quality of the power on the module. Need to be conservative on retaining as much operating margin as possible.
- Some modules are observed to require VDD=2.2V to operate error free when used with remote sense regulators in a realistic services configuration. This is a 10% addition to the digital power consumption compared to our previous default of VDD=2.0V operation. Even higher voltages may be required in practice, depending on the module activity.
- Transients induced during digital inject testing are large enough that they seem not to be affected by adding significant additional decoupling close to the MCC.
- For now, propose that we release the Flex production, and to continue studying the problem in more detail.