Recent Measurements of FE-B/FE-C Chips and Modules

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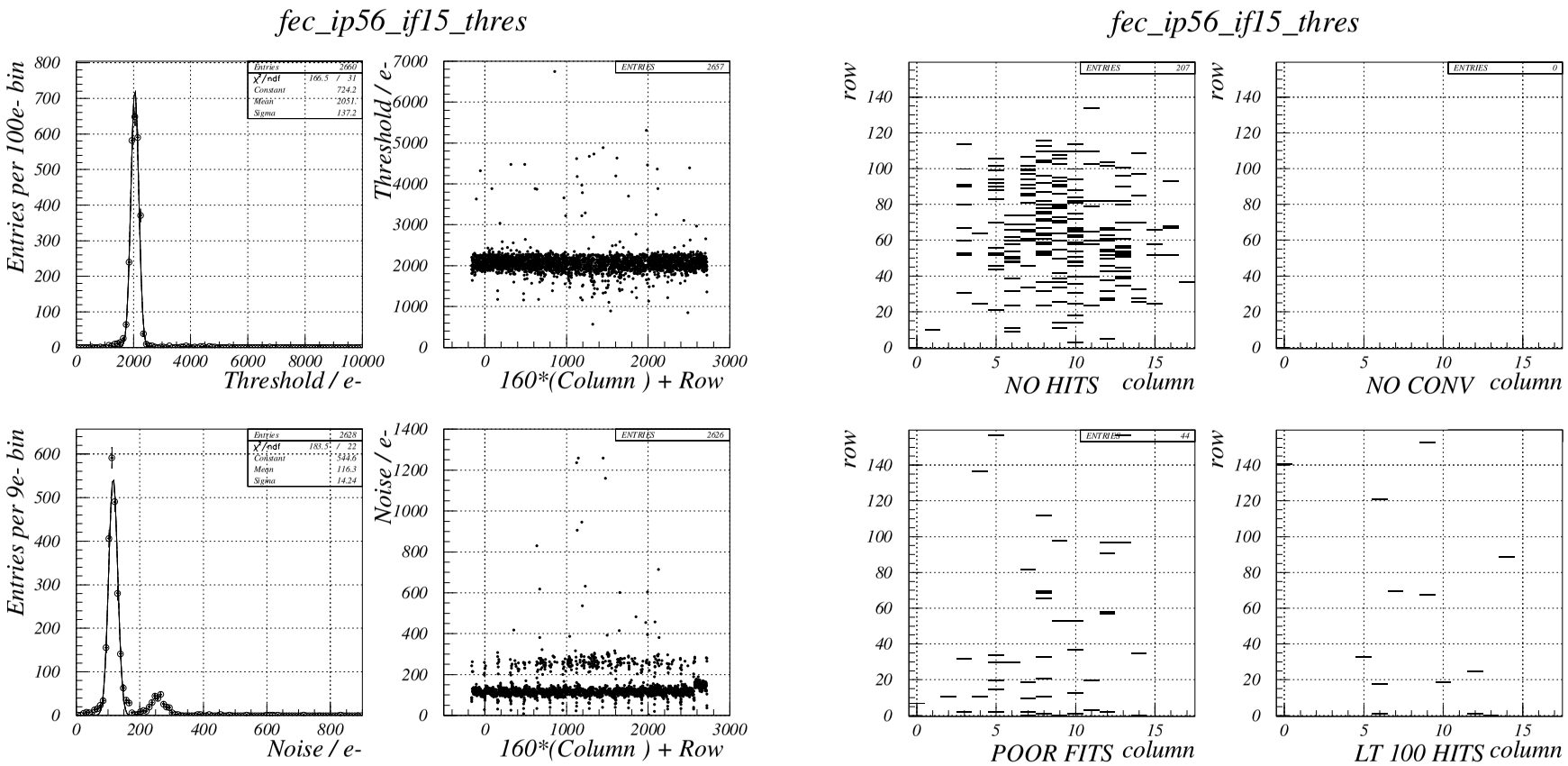
First Measurements of FE-C Single Chip Device (ST2)

Laser Timing Studies of FE-B Single Chips and Modules

Results from IZM-bumped Bare and Flex Modules

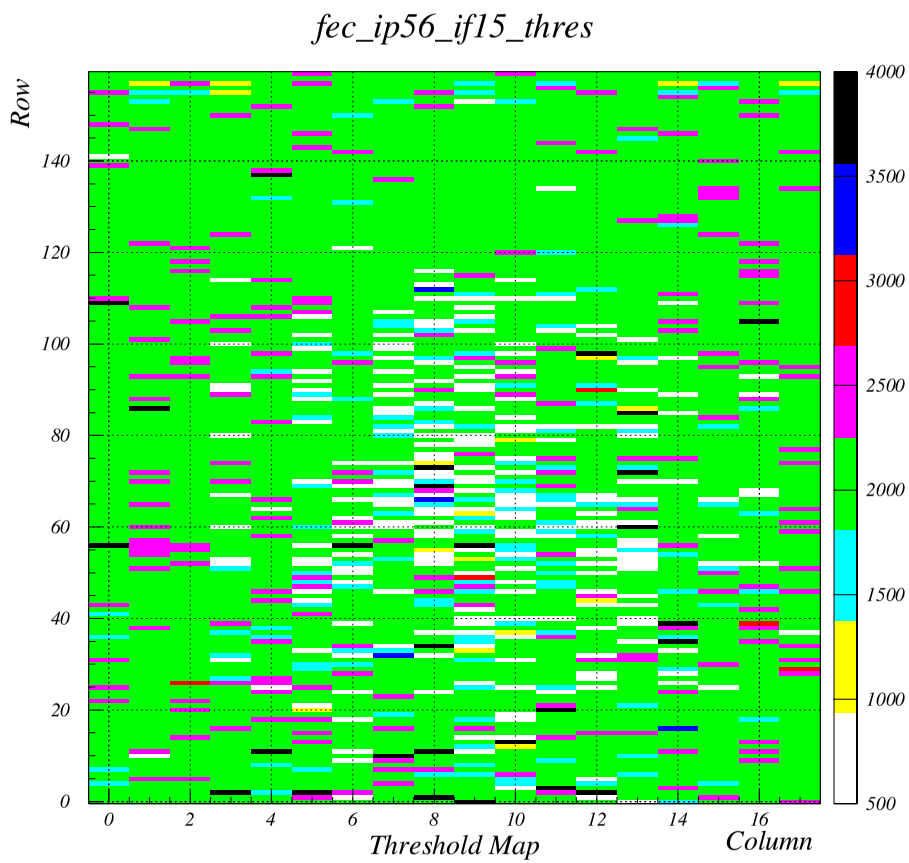
First Detailed Measurements of FE-C at LBL

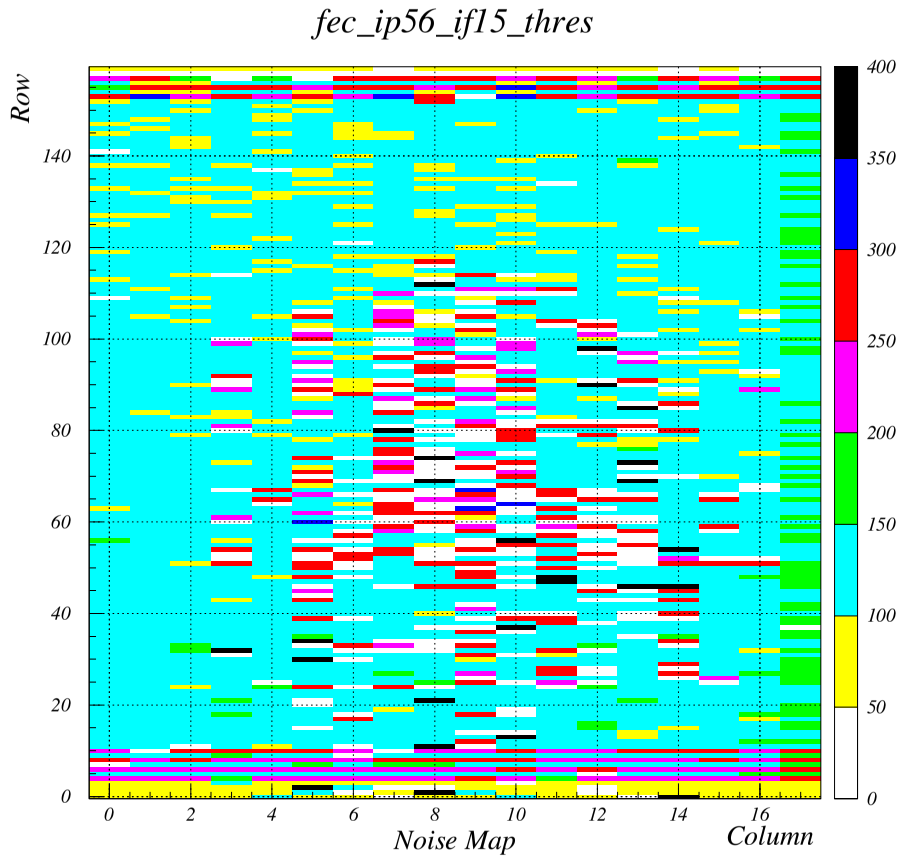
Received an ST2 single chip in March, which had known bump-bonding problems (about 200 dead channels):



- Initially operated chip with optimized settings from Bonn. Note, the large IP setting corresponds to almost 16 μA current through input transistor (too large...)

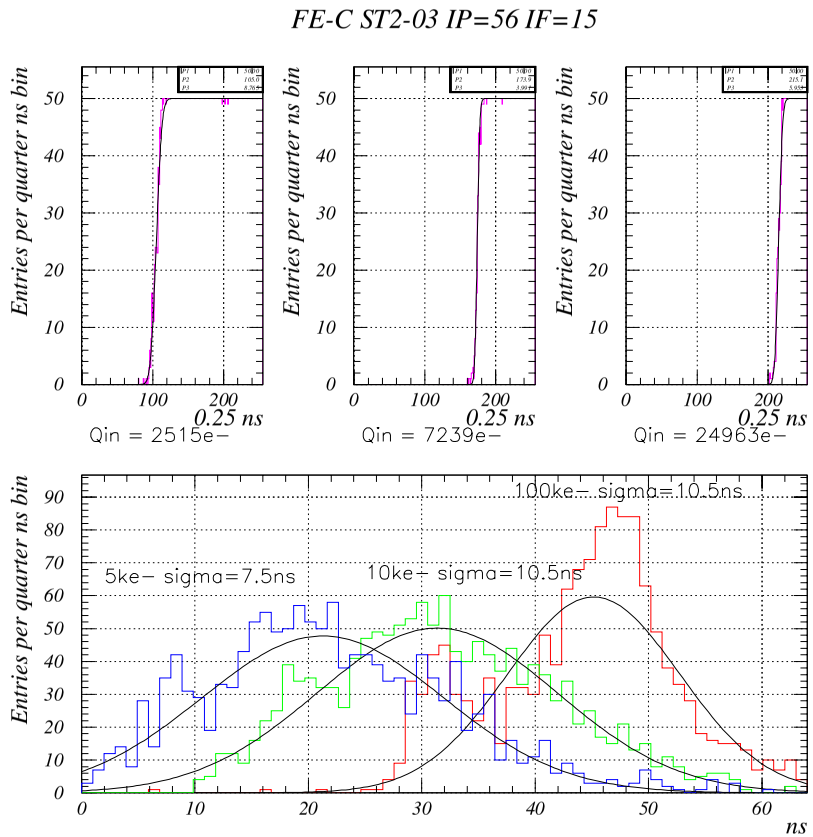
- Initial dispersion was 425e for IP=56, IF=15, ID=16 (slow shaping, large preamp bias, small discriminator bias). Uniformity of working channels looked reasonable:

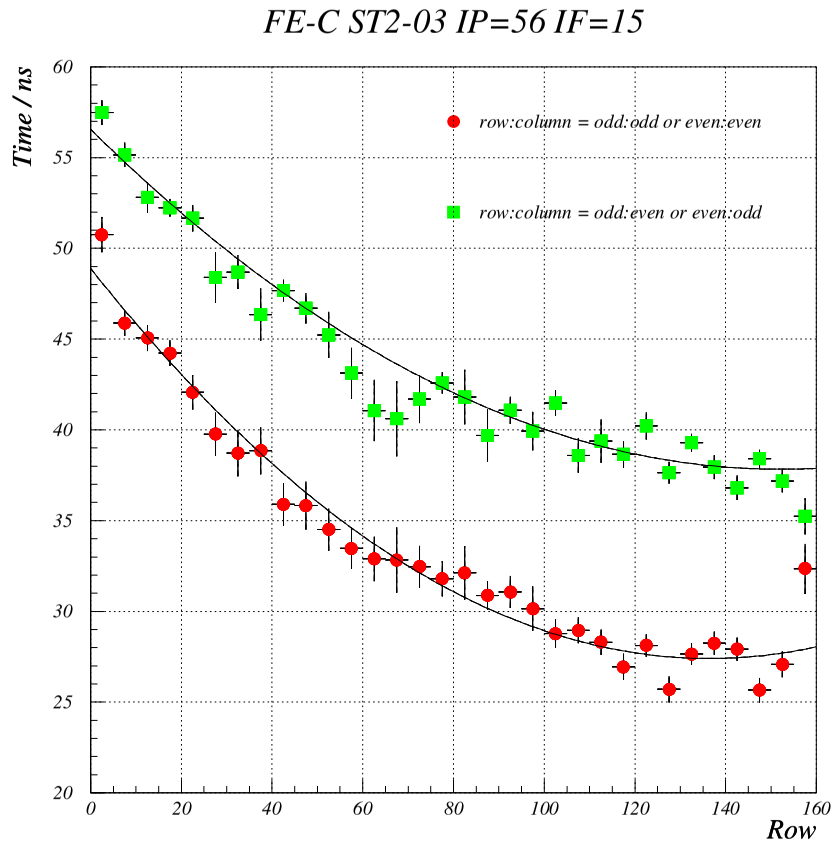




- Proceed to study first absolute timing for large charges (timing dispersion), and then variations in timing for particular pixels as a function of charge (timewalk).

Looked at absolute timing performance for large charges:

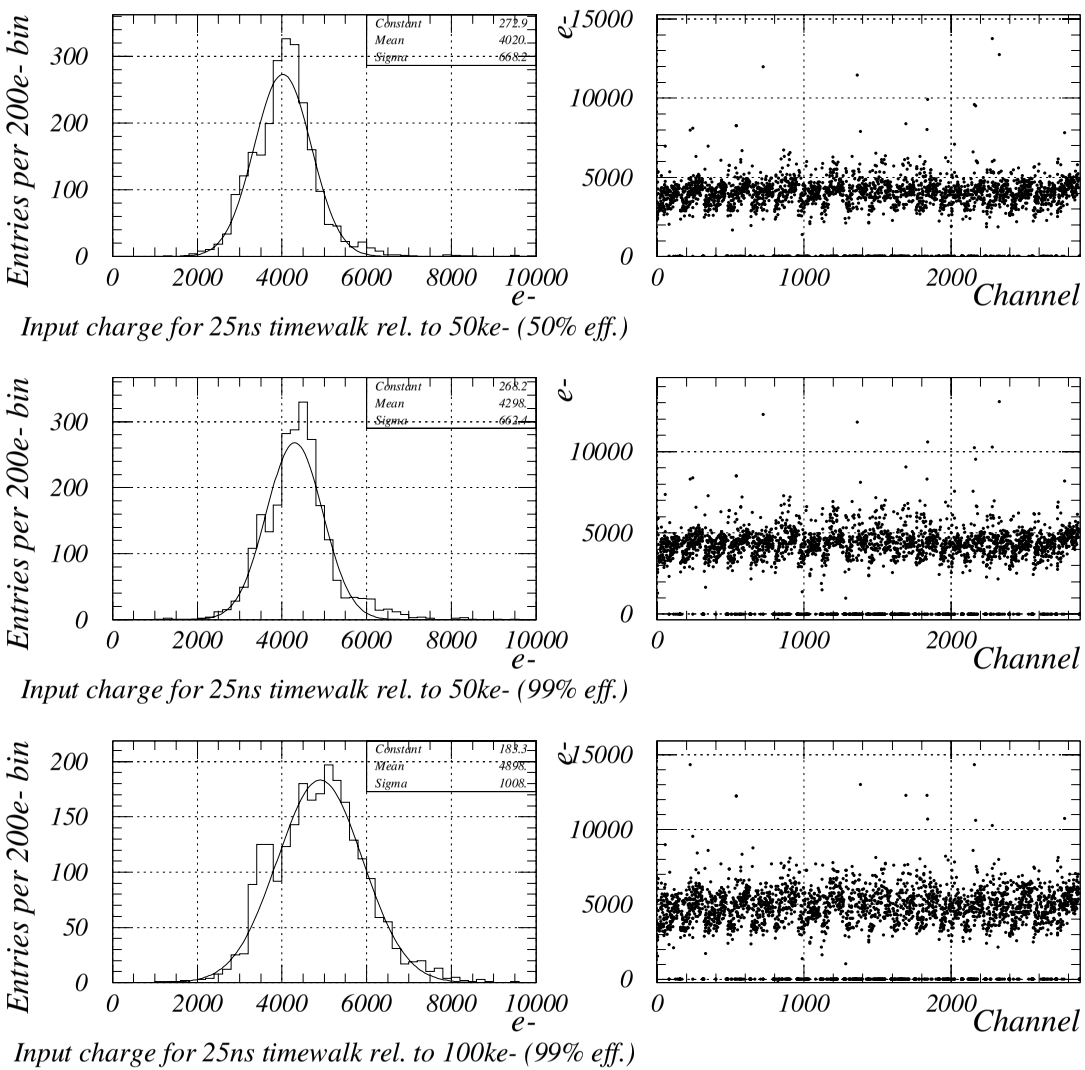




- Injection of fixed charge has large timing dispersion, although individual channels look fine. Measurements use strobe delay scan with PCC and external injection.
- Large systematic timing variation along column, probably related to clock distribution within column. Also a large odd-even effect within a group of 4 pixels. Total variation between extremes is approximately 30 ns !

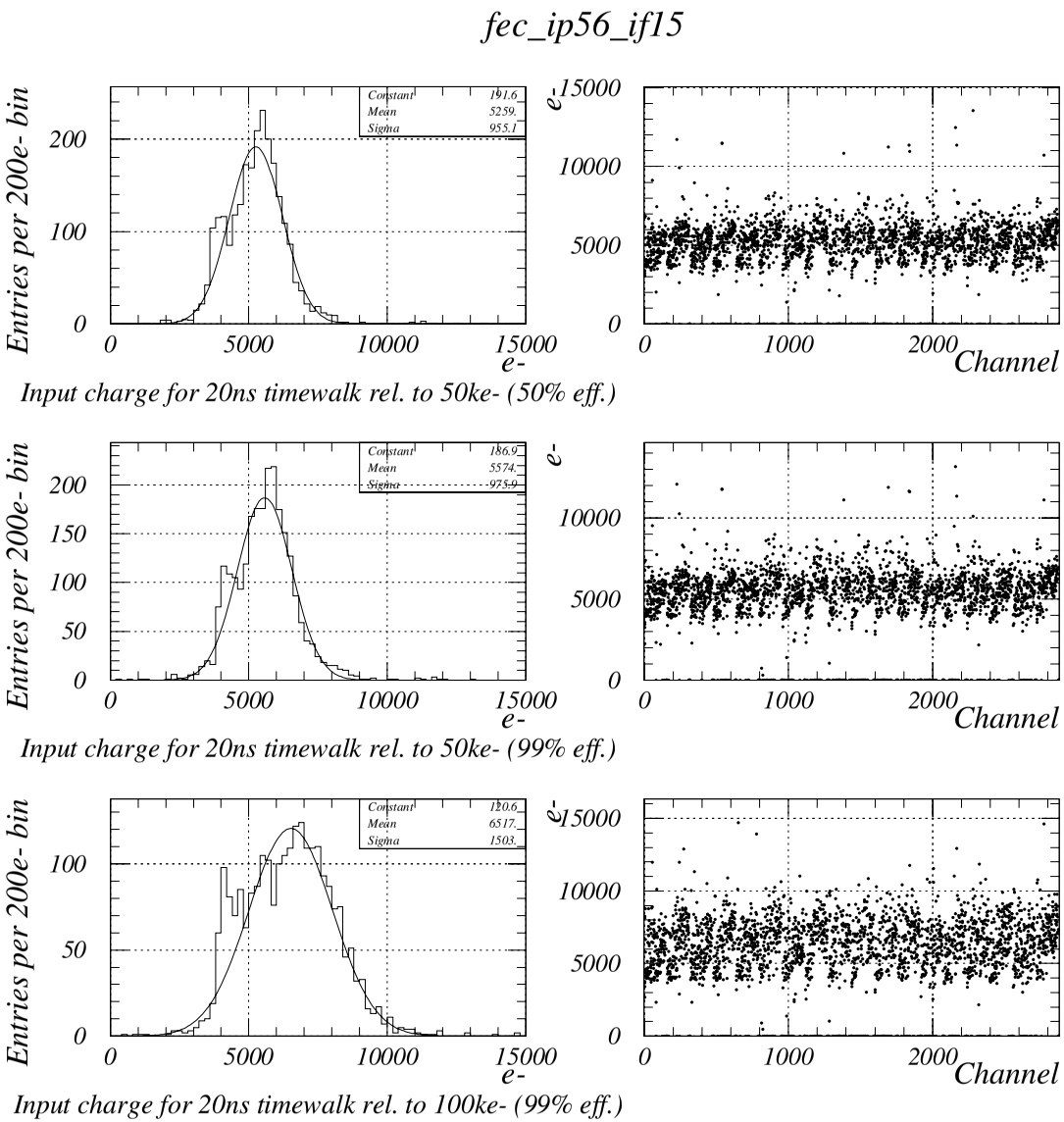
Perform 2-D scans of charge and strobe delay for each pixel and look at timewalk:

fec_ip56_if15



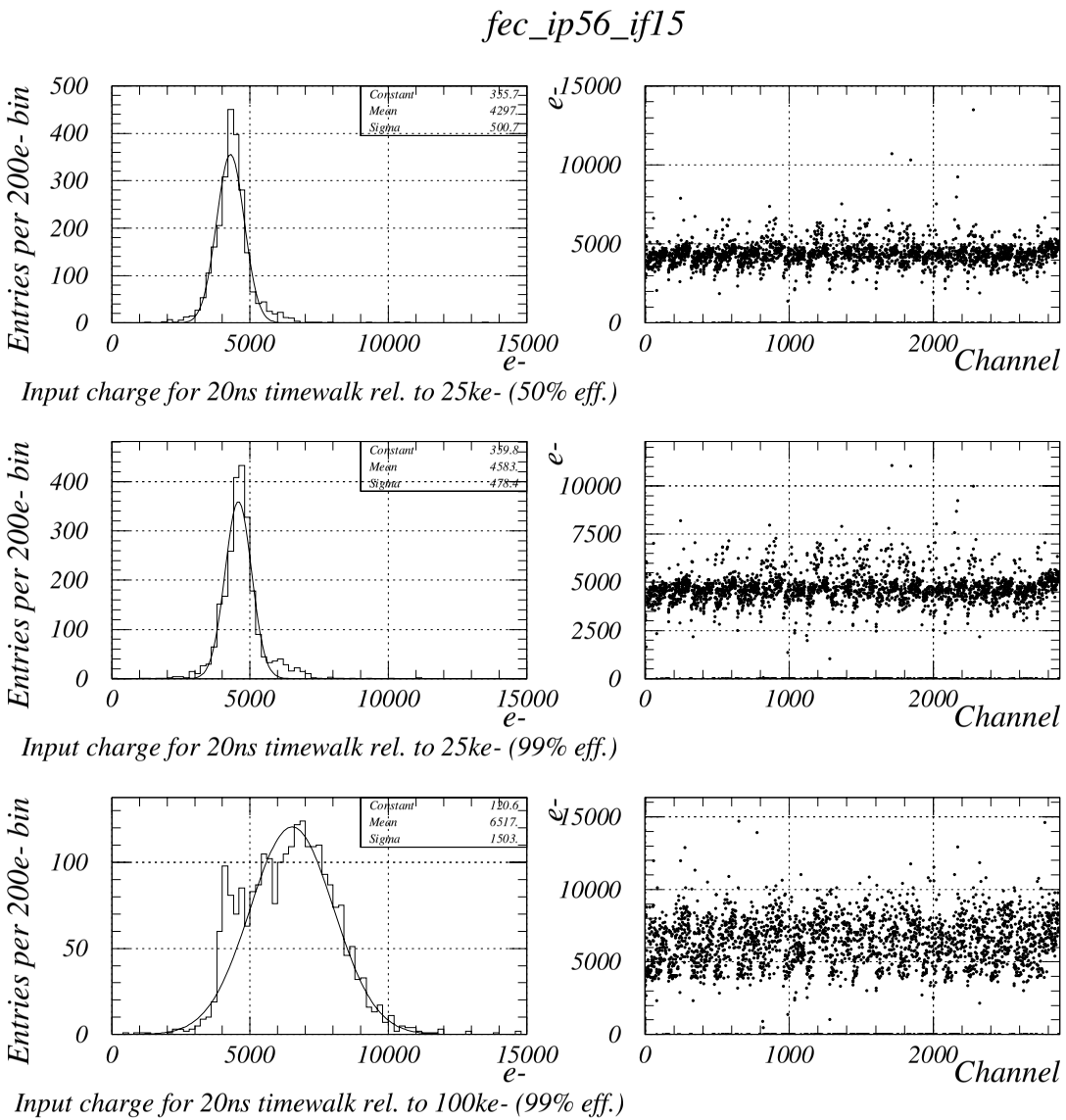
- Make measurements relative to reference “infinite charge” of 50 Ke.
- Find, when comparing 50% efficiency points for 50 Ke, and charge which has timewalk of 25ns, that an excess (overdrive) of about 2000e is needed.
- The dispersion in this “in-time threshold” is large (about 700e).
- Requiring 99% efficiency increases the “in-time threshold” further.

- More reasonable requirement is 20ns timewalk budget for the front-end:



- For this tighter timing requirement, the in-time threshold moves up to 5300e (3300e overdrive).
- Operating with a 2000e threshold is already fairly aggressive, and in this case leads only to a 5.3Ke threshold for single-crossing readout...

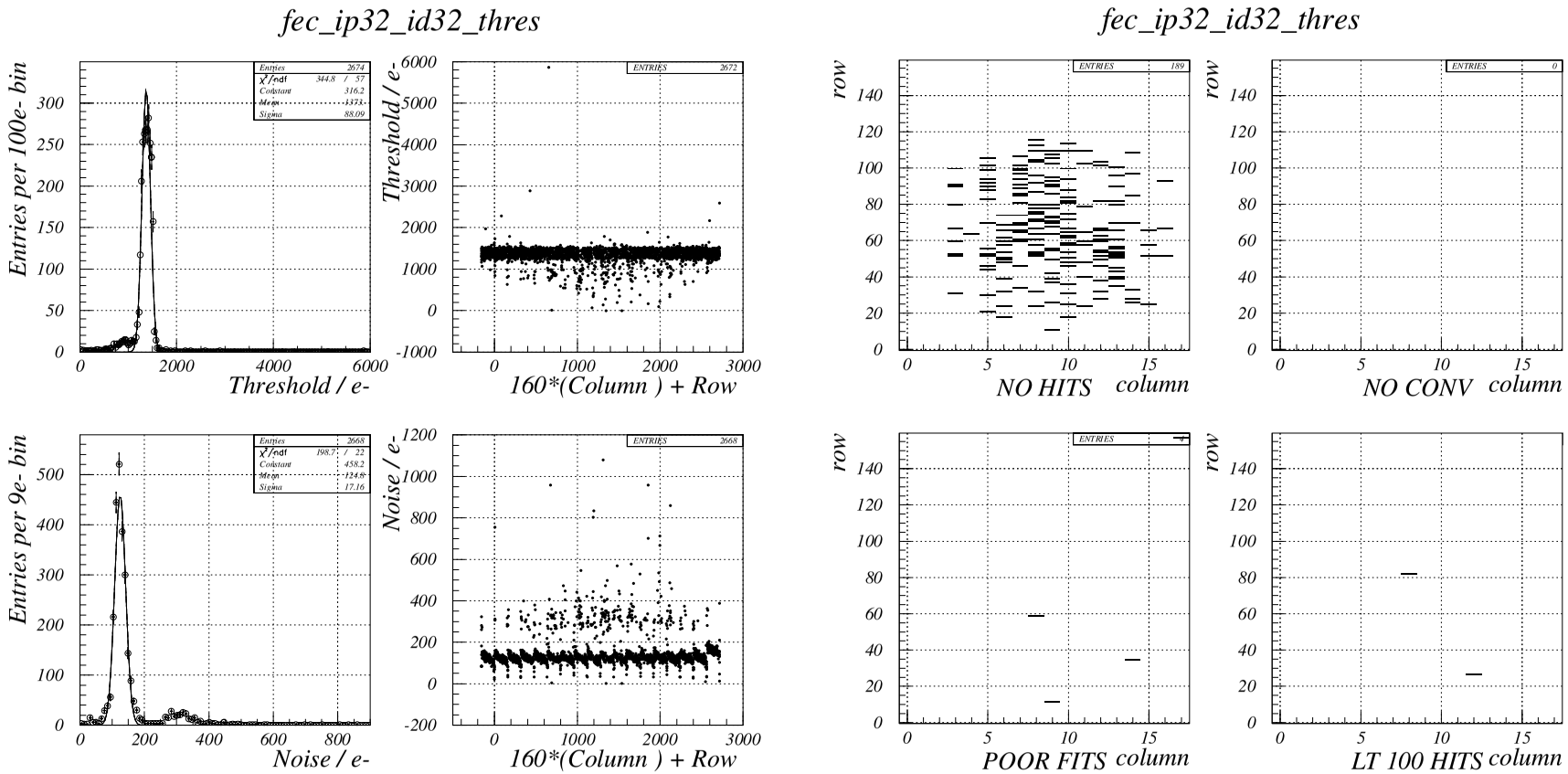
- Could argue that 25Ke reference charge is enough for end-of-lifetime:



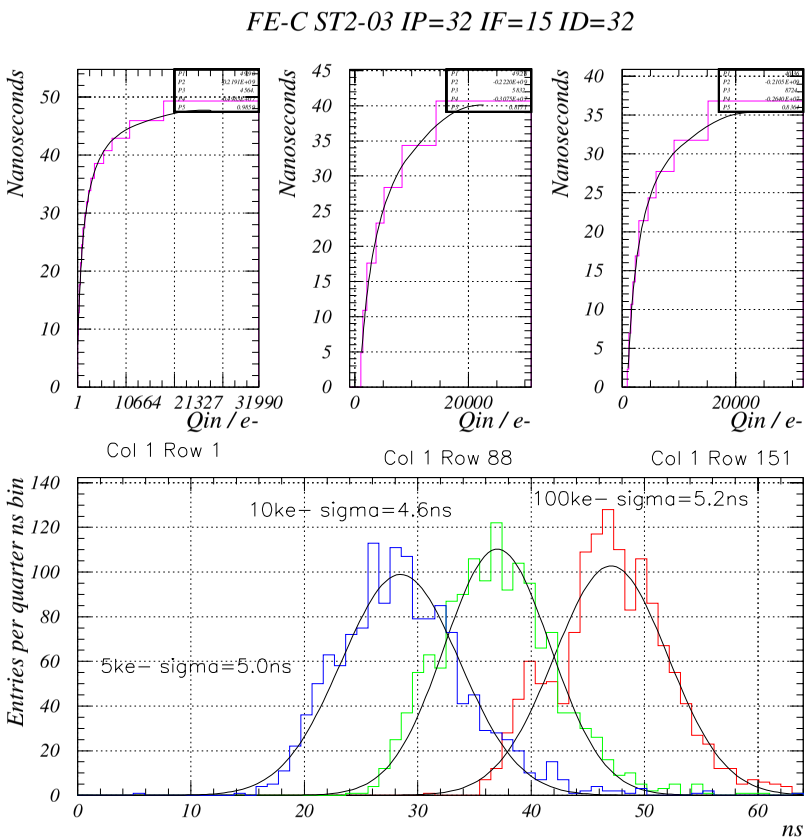
- At the end of the sensor lifetime, when the most probable charge may be 10Ke, charges above 25Ke could possibly be discarded (risky...)
- In this case, the in-time threshold is reduced to about 4300e. This is still rather high for a 10Ke most probable charge.

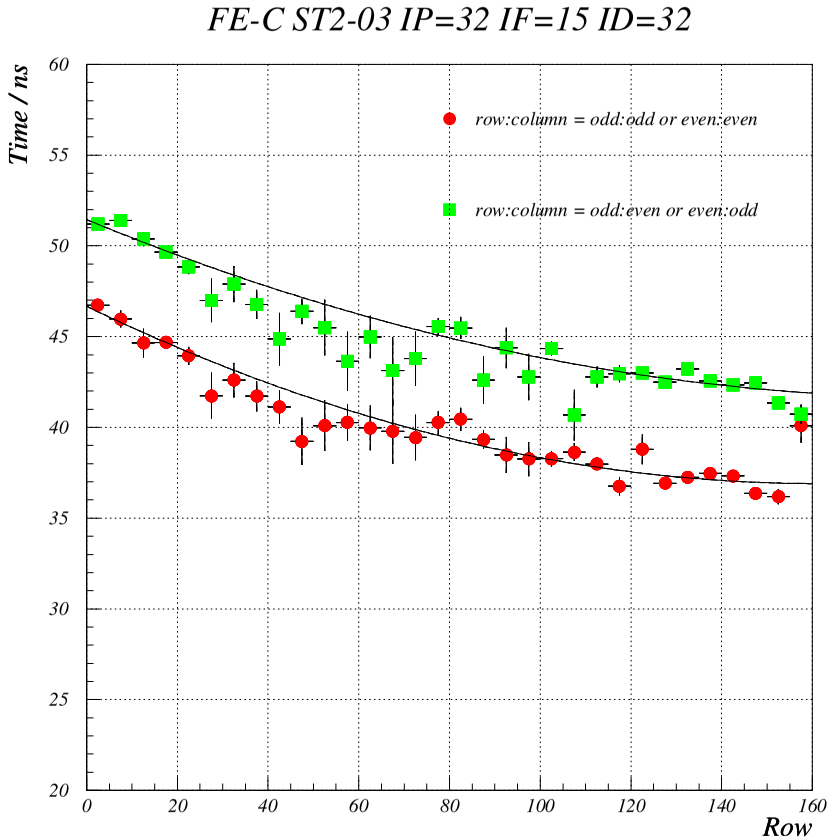
Try different operating parameters (IP, IF, ID):

- Find slight improvement for IP=32, ID=32.
- Note the threshold is much lower for fixed VCCD/VTH, about 1400e:



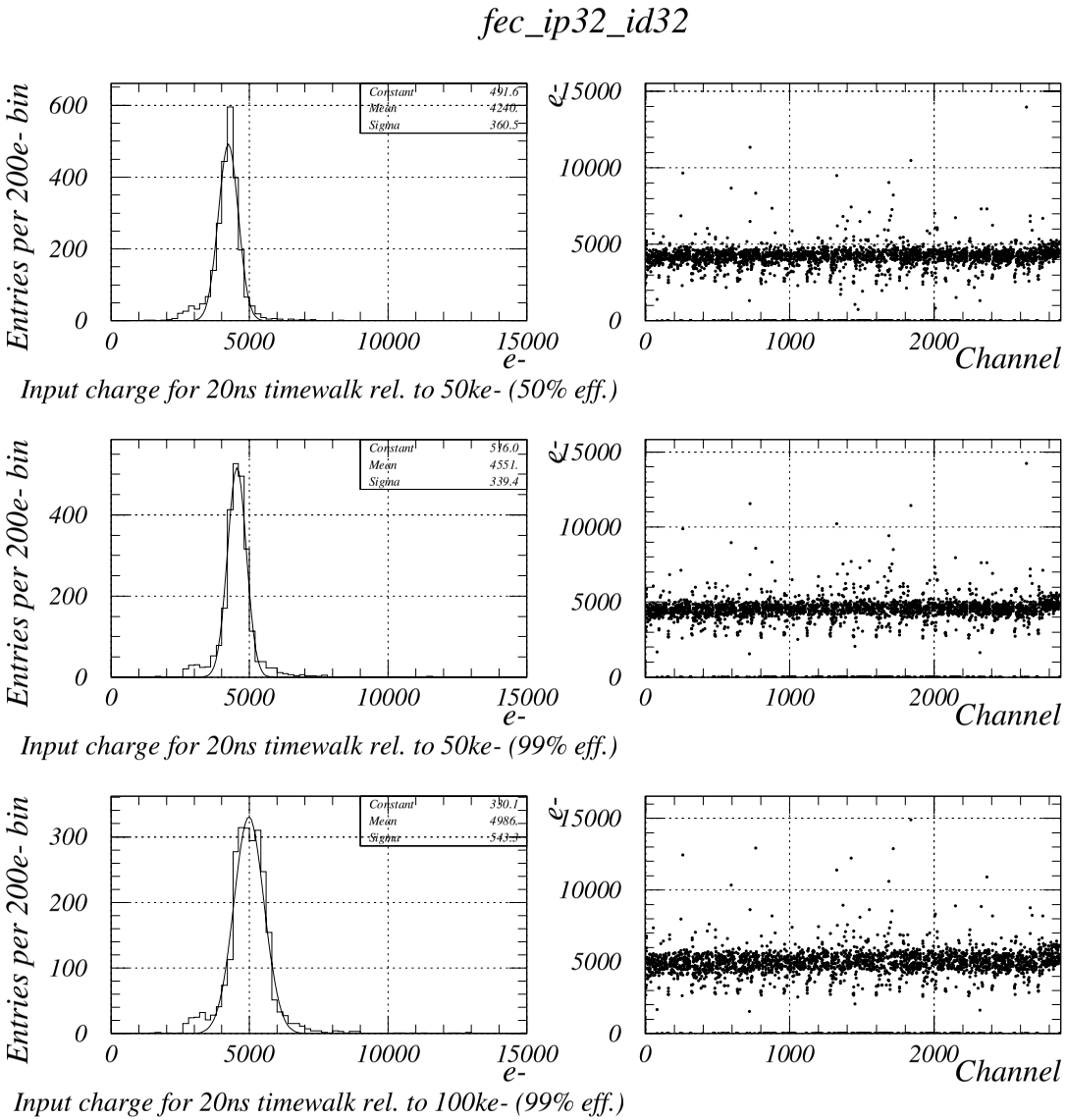
Look at absolute timing for large input charges:





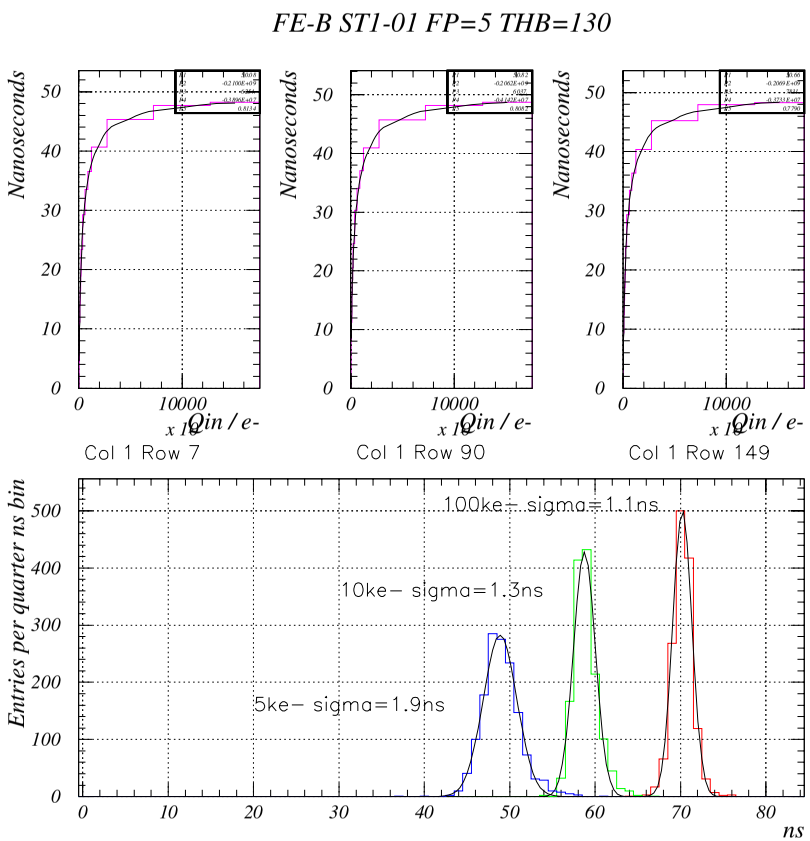
- The overall timing dispersion has been reduced. This is disturbing because it suggests some of the dispersion comes from the front-end.
- The odd-even dispersion is reduced from about 10ns to about 5ns. The maximum variation is reduced from about 30ns to about 15ns.

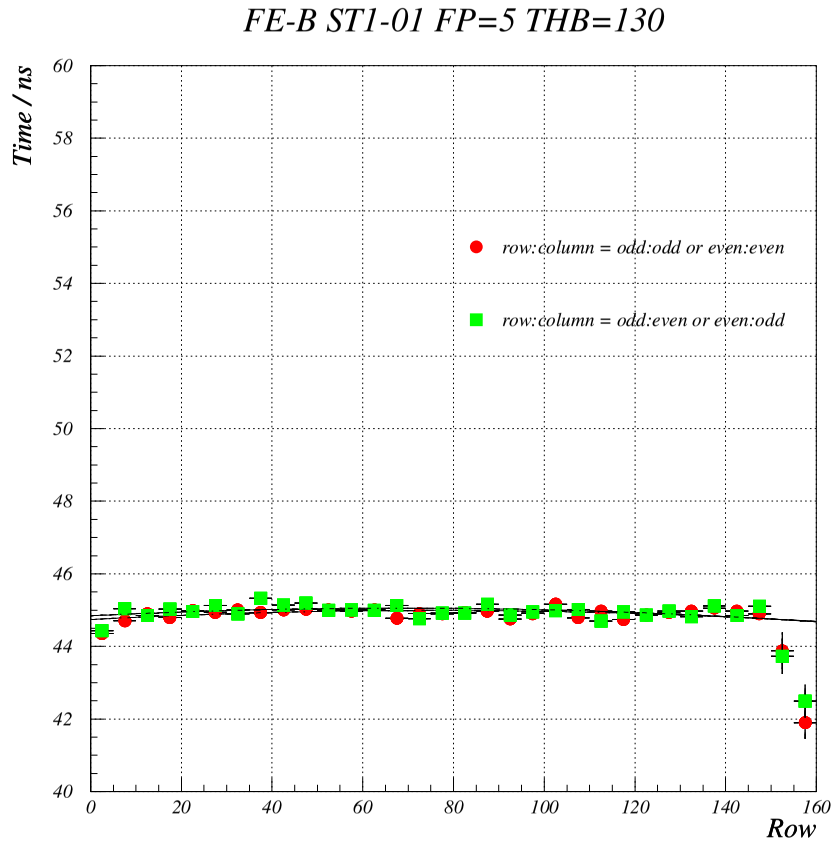
Look at timewalk:



- The plot is referenced to 50 Ke maximum charge, and 20ns maximum timewalk.
- The in-time threshold now requires about 2900e of overdrive, down from 3300e before.
- The dispersion is much lower, about 350e instead of 950e, suggesting that the larger discriminator bias is important.

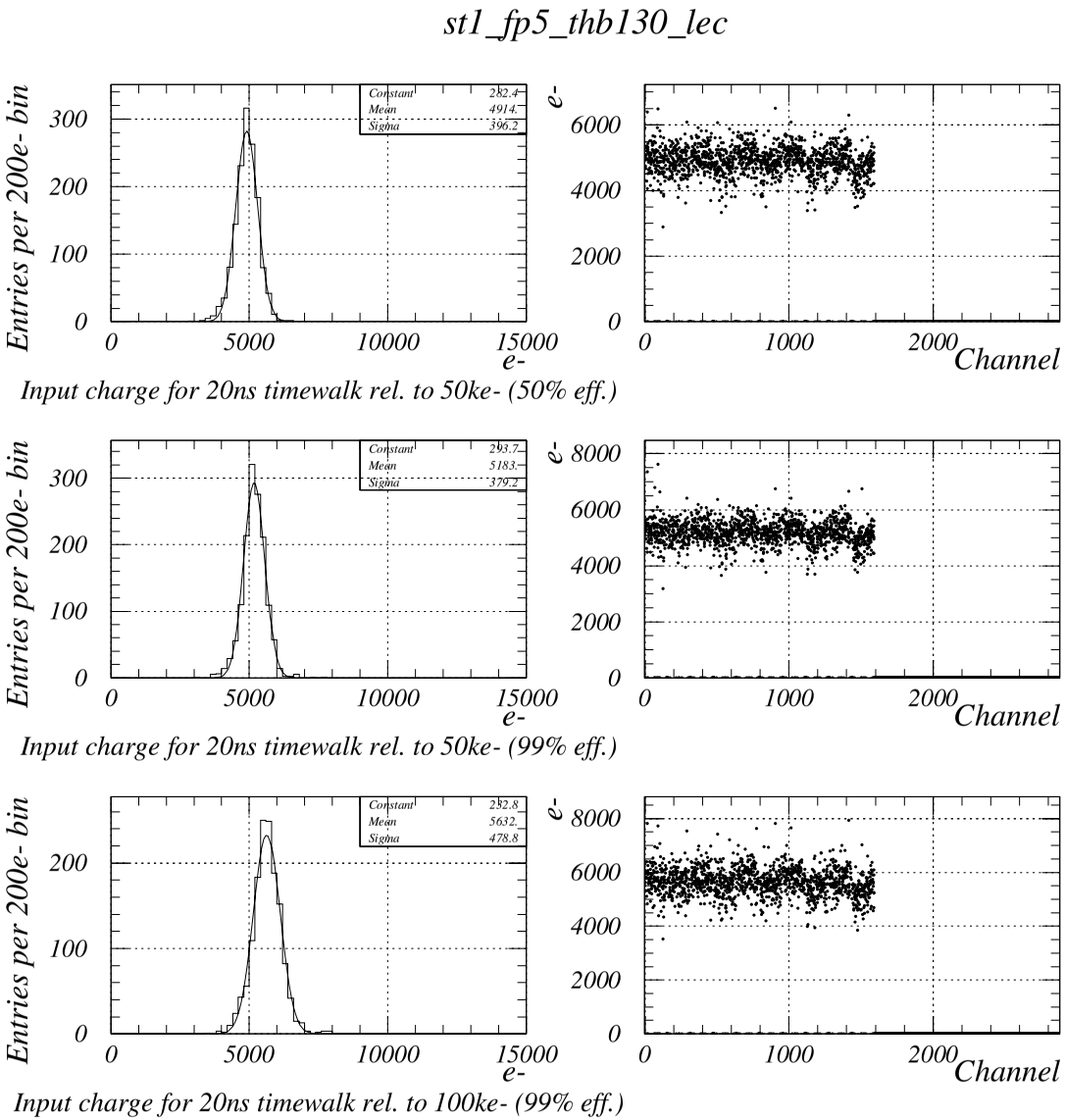
Compare to FE-B results for absolute timing performance:





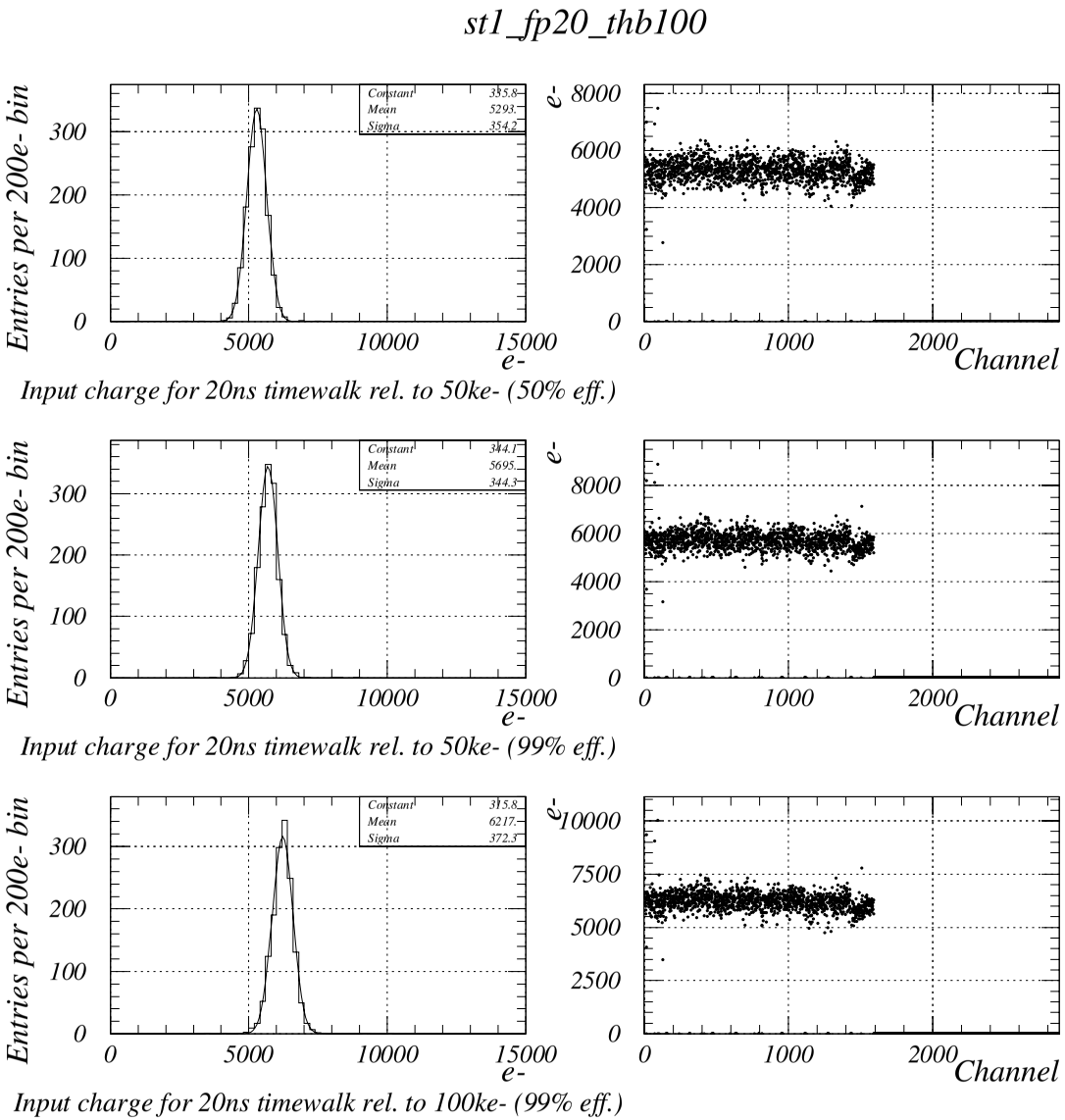
- The timing dispersion is much smaller, roughly 1ns for large charges, compared to 5ns for FE-C with the best biassing conditions.
- There is no indication of odd-even effects or noticable slope along the columns.

Look at timewalk:



- These bias conditions correspond to slow shaping with a threshold of 2200e.
- The in-time threshold is about 2700e higher with a dispersion of about 400e. This is referenced to 50Ke and a maximum timewalk of 20ns.
- It is known that the timing performance of FE-B is poorer with slow shaping due to the longer peaking time of the diff-amp stage.

Look at timewalk with faster shaping:



- This shaping corresponds to about 0.5 µs return to baseline for 1 MIP of charge.
- The threshold was about 3750e.
- In this case, the required overdrive was only about 1600e referenced to 50Ke and a maximum timewalk of 20ns. The dispersion is about 350e.

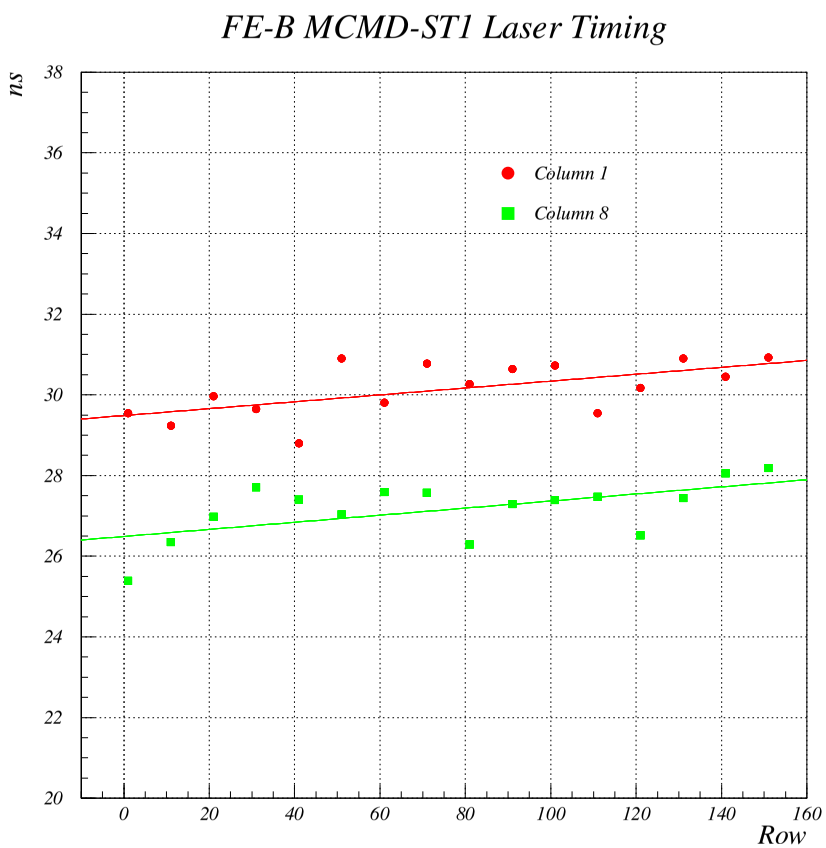
Summary of concerns:

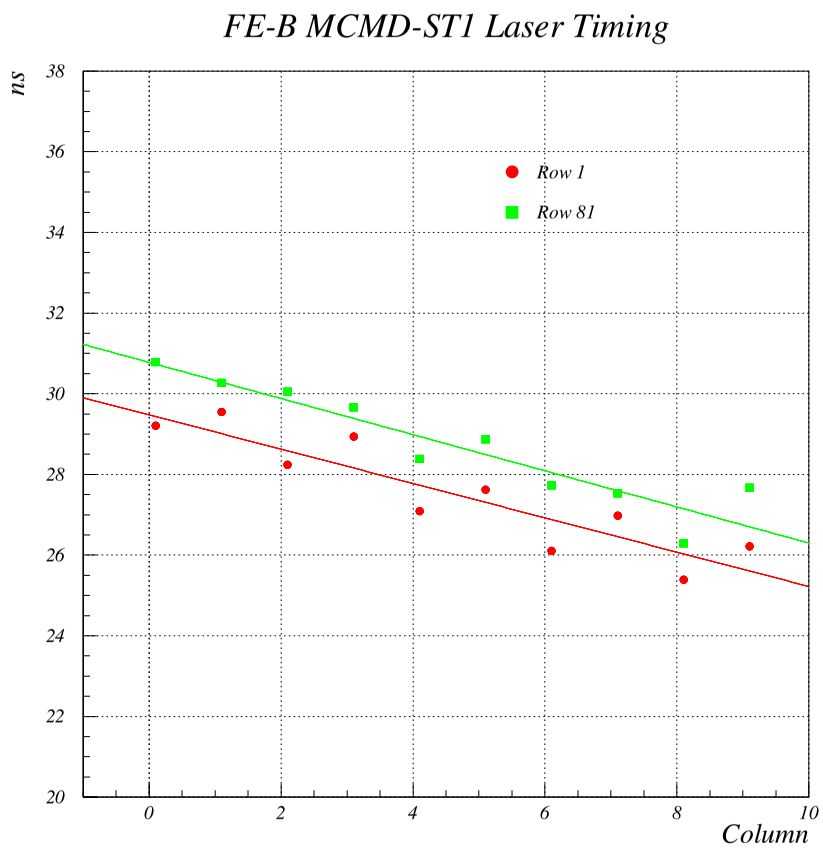
- Large timing dispersion within FE-C readout makes it difficult to look for other timing problems. However, odd-even effects seem to vary with front-end bias, suggesting they may not just be due to the readout circuitry.
- The observed timewalk performance is worse than expected (based on single channel measurements). It is difficult to achieve an in-time threshold less than about 5Ke, referenced to 50Ke and a maximum timewalk of 20ns. This performance was measured for an ST2 sensor, which is a much lower capacitance detector than the one we will actually use. No measurements have yet been done in which leakage current is also present.
- Large TOT variation observed for moderate charges. The variation is monotonic and systematic along the column. This seems inconsistent with the uniform behavior of the noise, since most likely source would be feedback current.
- The “default” operating conditions (VCCD=1.5V VTH=1.4V) correspond to a strong additional shaping in the AC-coupling which further reduces the TOT range and may increase the noise.Trying to operate the chip with reduced AC-coupling shaping (higher VCCD) seems to result in very large threshold dispersions and reduced ability of the TDACs to compensate. This should be better in FE-D...

Laser Timing Studies with FE-B

- All timing studies reported up to now rely on internal injection system to provide charge at preamp. There are distribution problems with VCal that can partially cancel any problems with the timing distribution in the chip.
- The ideal approach is to inject charge at a fixed time relative to XCK for all regions in the pixel array. This was done using an IR laser (1064 nm), focussed to a spot size somewhat smaller than the back-side metal opening (30μ wide).
- During these measurements, we discovered that restarting the Grey counter in FE-B (using WriteLatency) causes random jumps in the timestamps relative to the XCK by up to 1ns. The cause is not known (the Grey generator resynchronizes the internal counter signals with XCK before distributing them).
- Single chip measurements were made without restarting the Grey generator. For module measurements, many measurements were averaged to get a more accurate result.
- Measurements were made using fast shaping (FP=20) to ensure that TOT was always within latency for large charges.

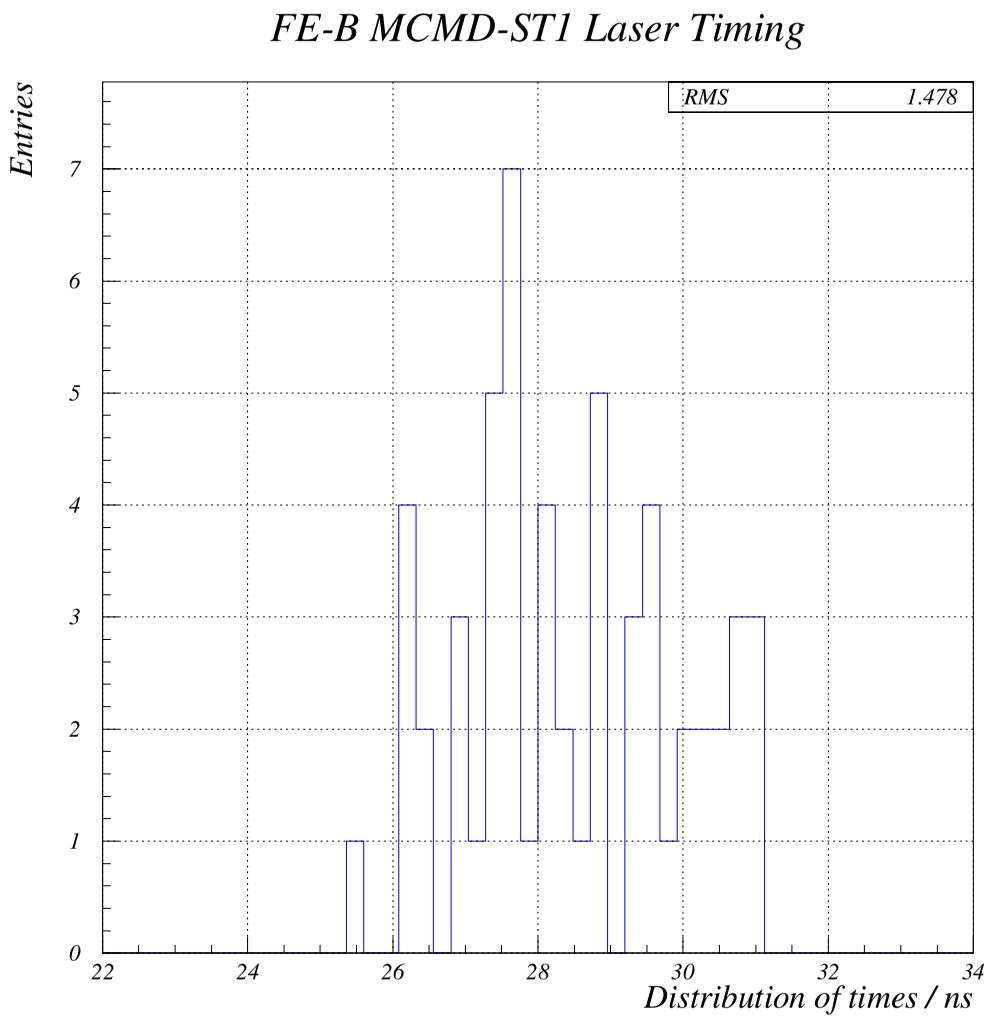
Measure variation in timing versus row and column:



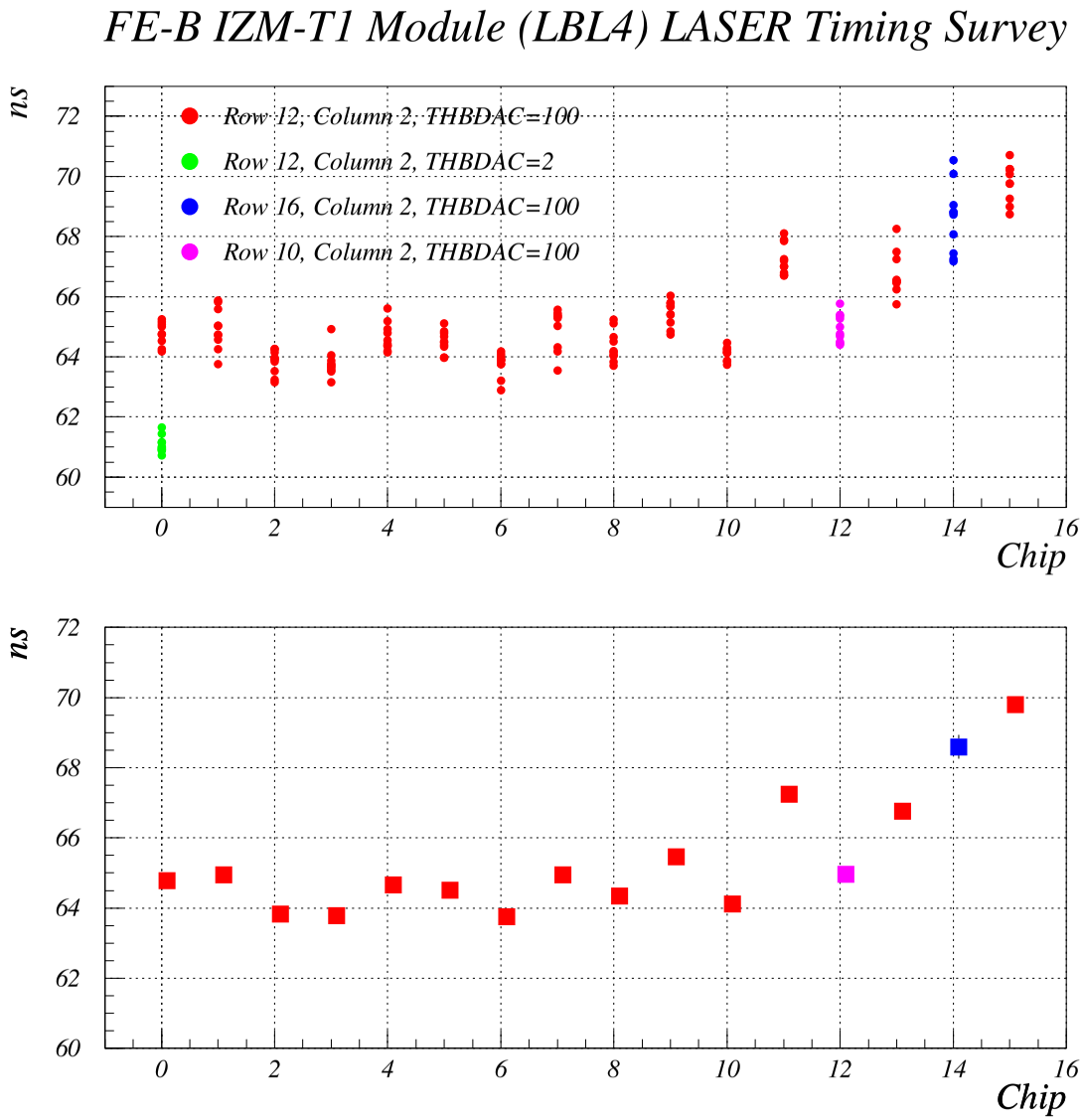


- Observe variation along columns of roughly 3-4ns. Note in FE-B the TSI are distributed from a single large driver block located between column 9 and 10.
- Observe smaller variation along rows of roughly 1ns.
- These variations are similar to, but worse than, predictions of a simple R-C transmission line simulation of the TSI distribution.

- RMS of the observed variations is about 1.5ns, which is slightly worse than would like, but not unacceptable.
- Note observed variations are worse than what is measured using charge injection (1.1ns RMS), which suffers similar distribution issues within 2D pixel array.

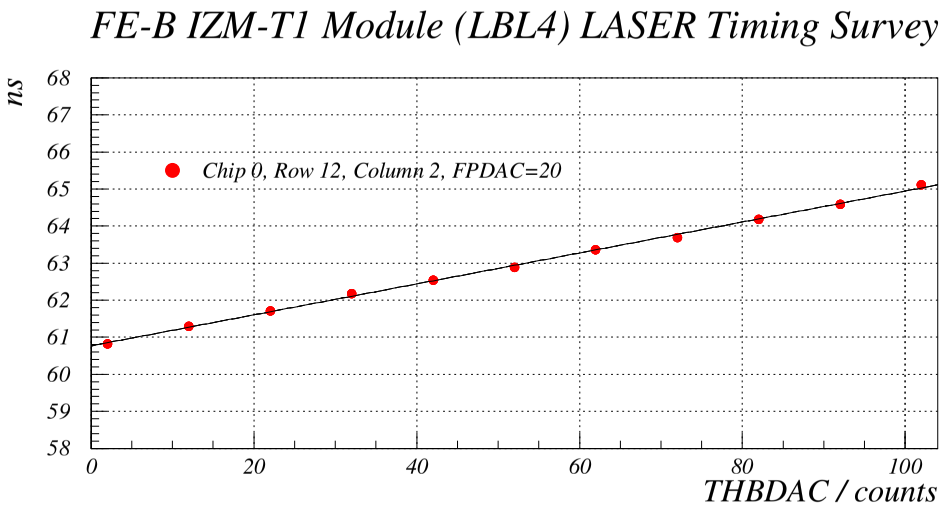


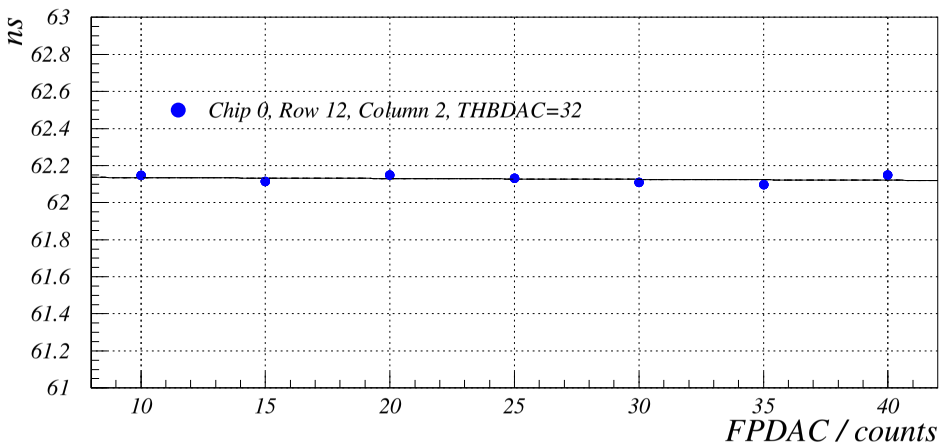
- Have also made systematic studies on bare IZM Tile 1 module. In this case, many measurements are made at each point:



- In bare module, XCK is distributed in U bus from chip 0 to chip 15.
- Individual Picoprobe measurements of two XCK lines confirms rough trend seen here, but measurements assuming FE receivers see “zero-crossing” do not show large magnitude of variation seen near the end of the XCK distribution chain.
- Overall timing uniformity of module looks good except for last 3 chips. Would H bus be better ?

- Have also studied timing of FE chip as a function of some DAC settings:





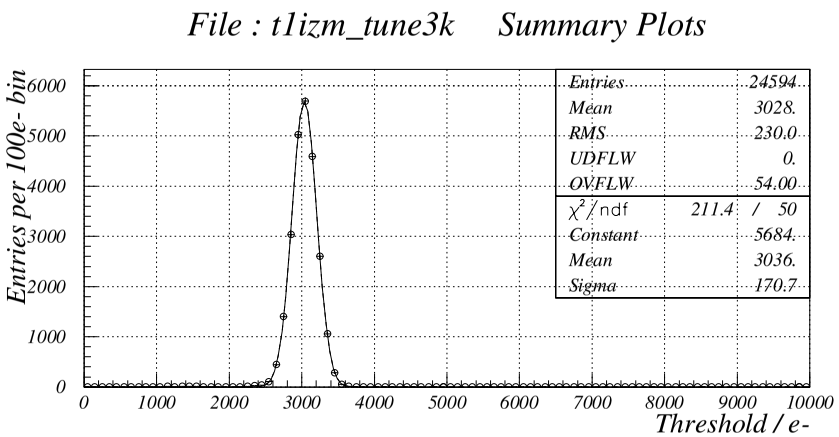
- Transit time not sensitive to feedback current, but it is sensitive to the threshold.
- Do not know if this is a “slew-rate limiting” effect or really a response time effect for the diff-amp.

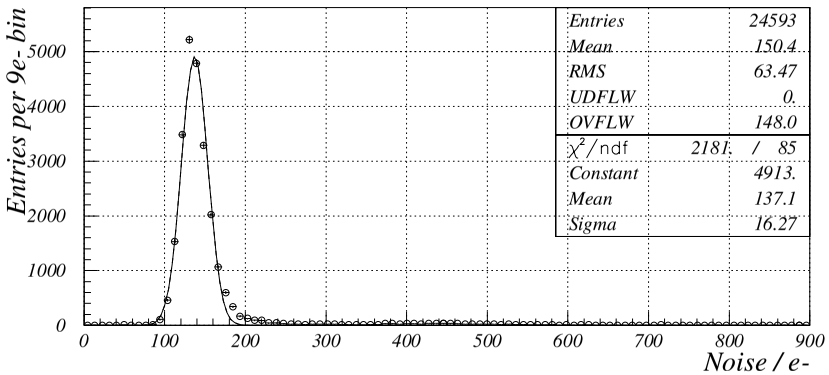
- Note: unfortunately these measurements are not easily possible with Flex mounted on top of sensor...
- Have not managed to get laser measurements to work reliably with FE-C.

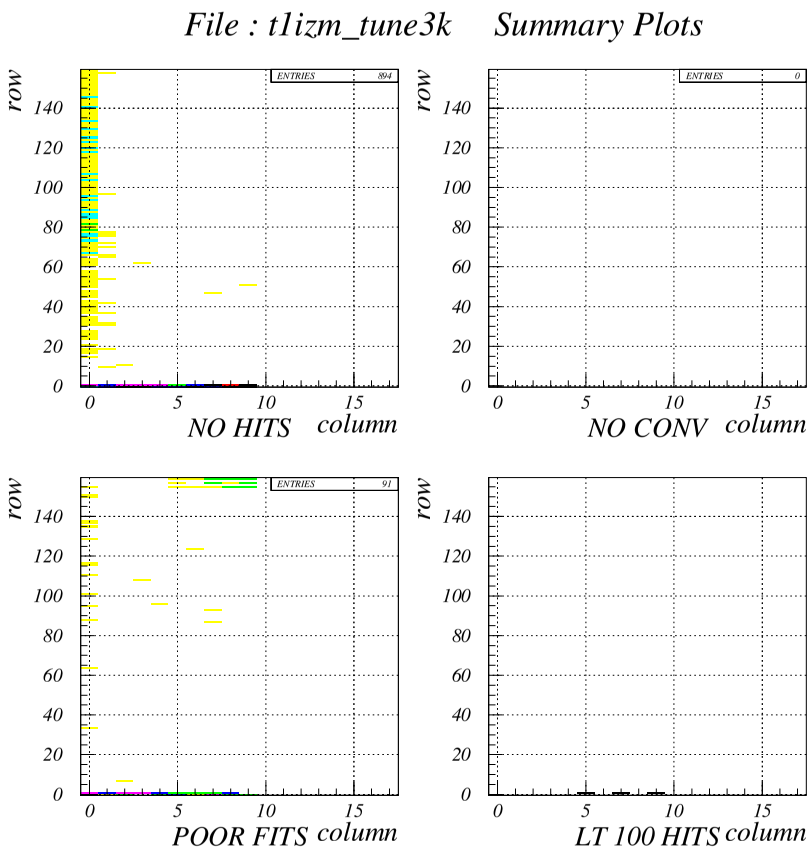
Results from IZM "Bare" Tile1 Module

- Assembled first IZM-bumped FE-B module to new Genova 1a support card in March. This card supports global Hitbus OR for module and better power distribution and decoupling.
- All chips work correctly, but had many problems with wire-bonding of FE chips (they are much more difficult to bond after IZM processing). This will be addressed in future (sensor 2) modules by an additional mask step to protect the pads from under-bump metalization. Many dead channels, beyond those expected from large number of merged bumps observed under X-ray inspection.
- In addition, module suffers from an intermittent short of one side of XCK. When this short appears, one side of the XCK disappears and the digital current consumption goes way down. This problem is almost certainly a fault in one of the vias during the distribution of XCK from the MCC to the module. While at the testbeam, this short became "permanent", and the module no longer operates.
- Threshold scans have been done at several thresholds, including equilization of the threshold of the different chips in the module. The module has been operated in "global self-trigger" mode where the readout of all non-hot pixels has been simultaneously enabled. The module operates well at a 3Ke threshold and a 70 KHz self-trigger rate with a Cd109 source. Threshold scans done with all pixels enabled for readout, and the CD109 source present, show no increase in noise.

Threshold scan results for module:

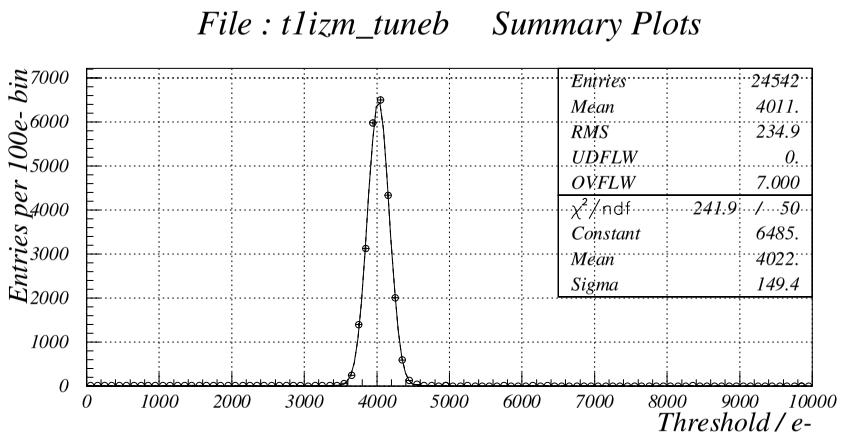


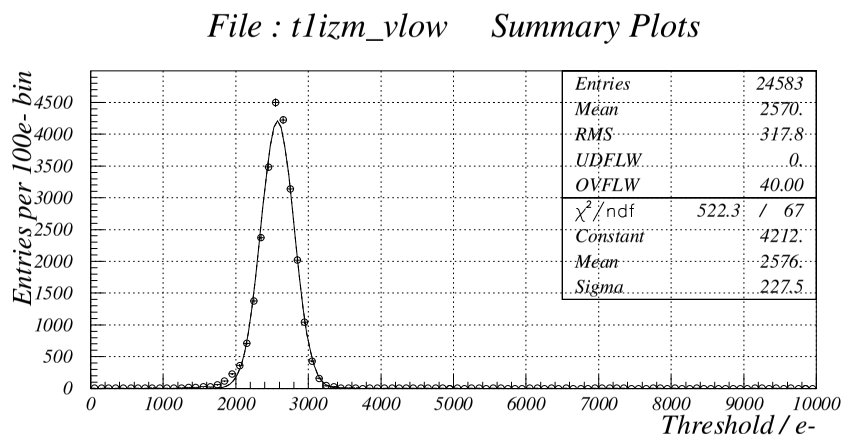


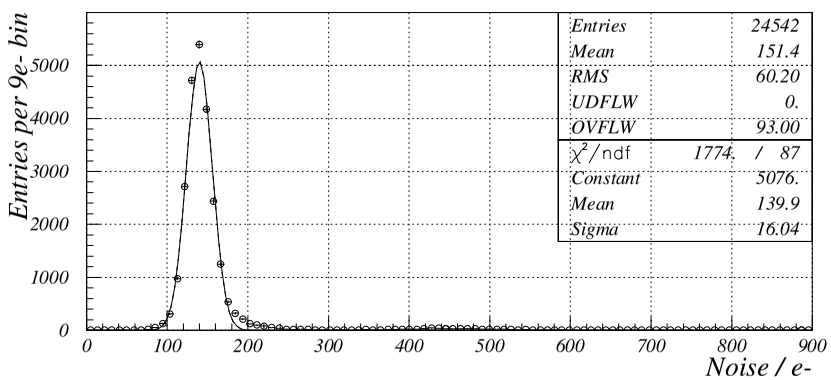


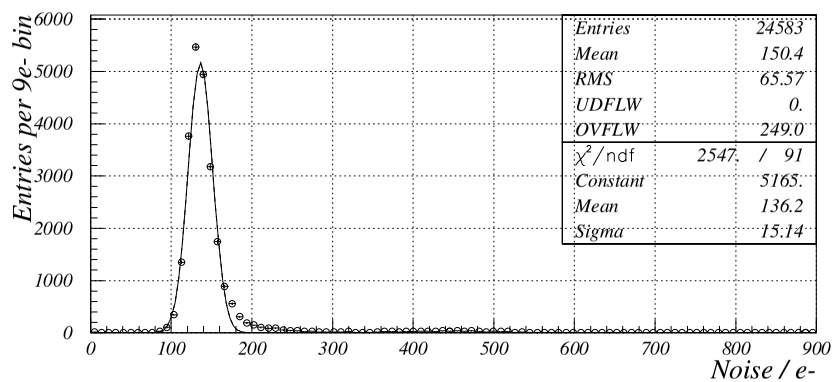
- Excellent threshold dispersion of 170e for complete module, and noise of less than 140e for complete module at 3Ke threshold.
- Observe roughly 900 dead channels (greater than 3%), which is not acceptable. Almost all of the defects are in the edge column 0, claimed to be related to handling of die prior to flip-chipping.

- Initial threshold scan was tuned for roughly 4Ke. TDACs were determined at this stage and then not changed for later scans, so this has smallest dispersion (150e).
- Threshold scan also done at approximately lowest common threshold for all chips, found to be about 2500e. Difficulty in achieving common threshold led to larger dispersion (230e) :

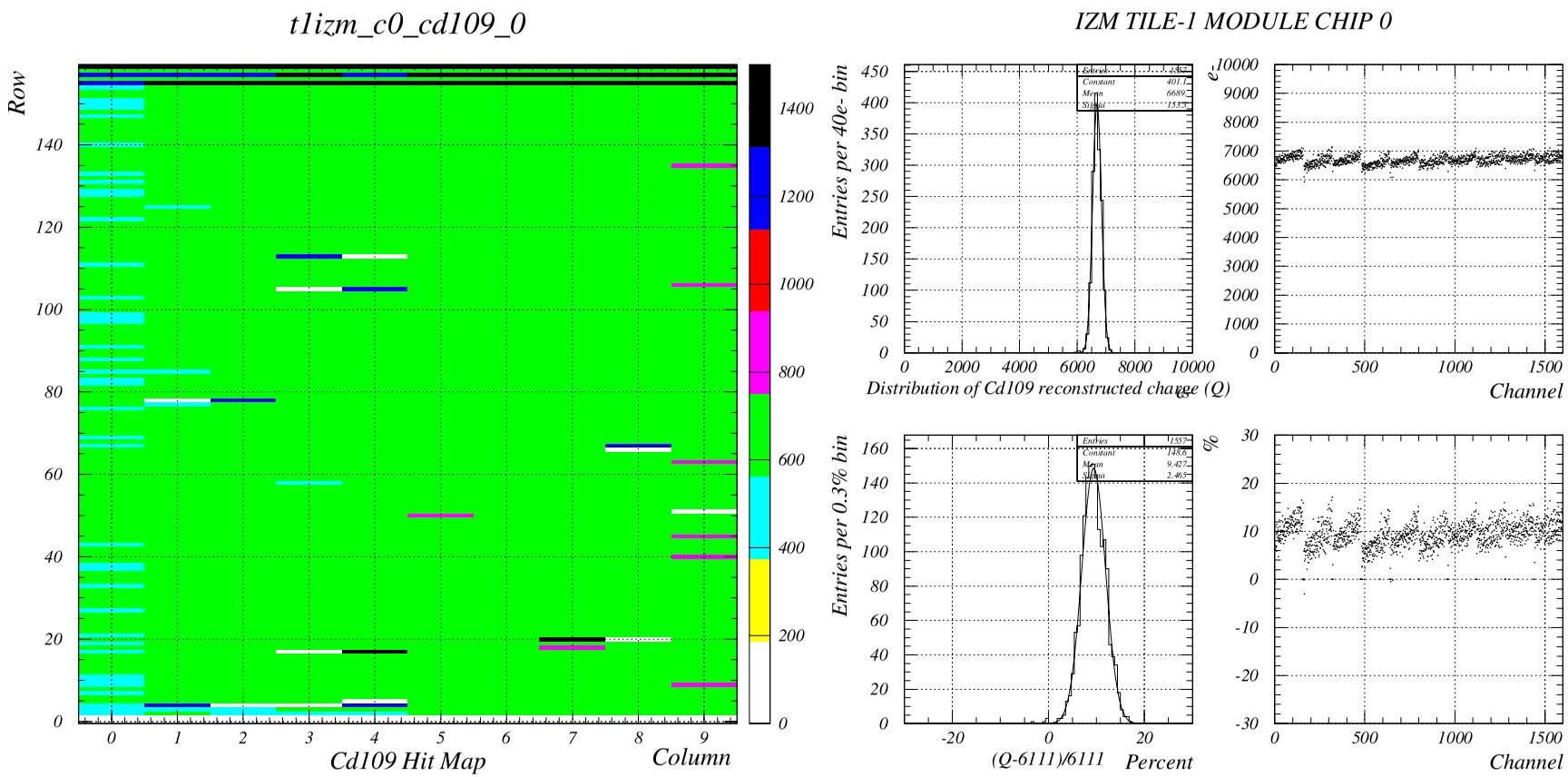








- Have also done source calibration using Cd109 source:

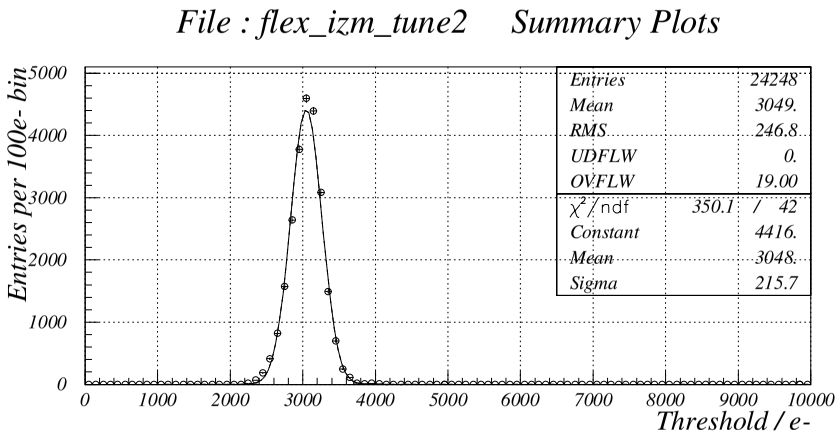


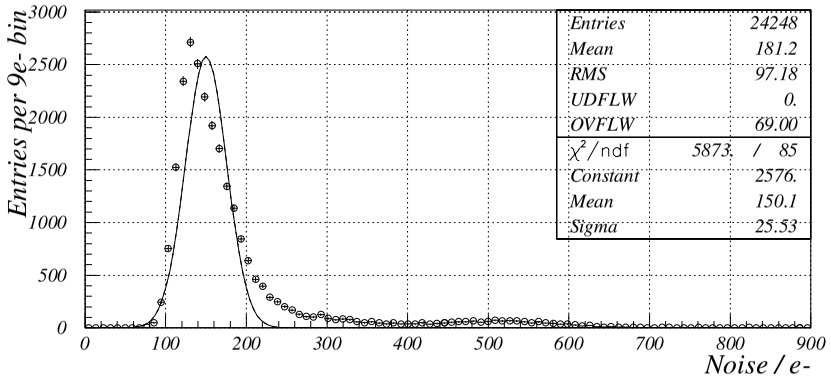
- First acquire 1M self-trigger source events for each FE chip. Then do a TOT calibration, injecting sequence of charges and fitting for individual responses.
- Then cross-correlate fitted source peak for each pixel with TOT calibration for the same pixel to determine an absolute calibration scale factor.
- For first chip, find scale is off by about 10%, with RMS of 2.5%.

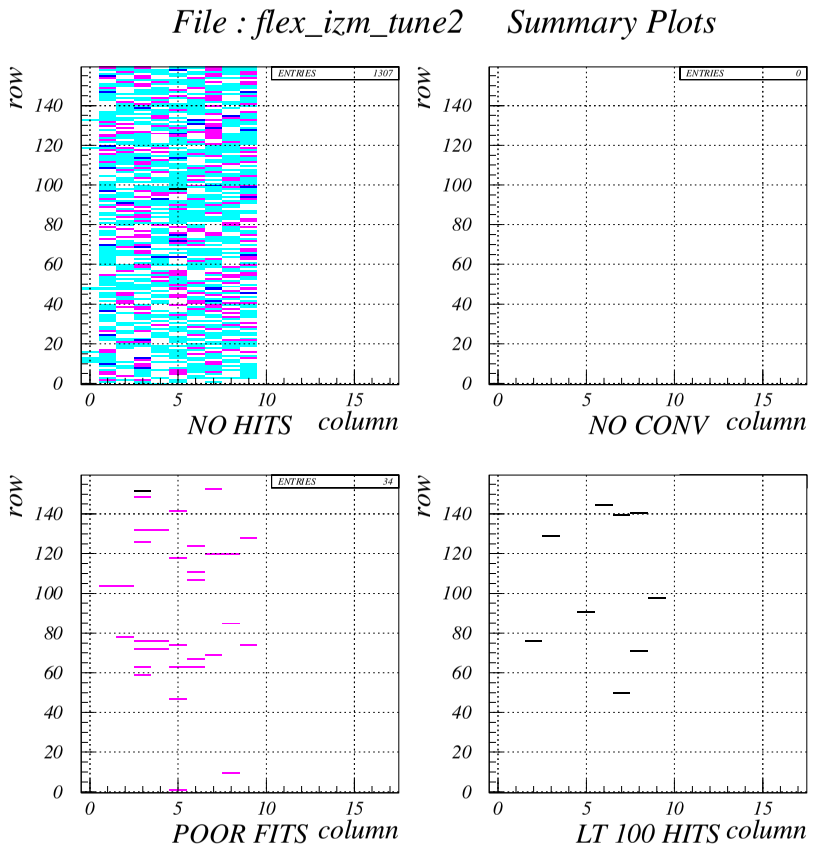
Results from IZM Flex Module

- Received new prototype 1b assemblies shortly before testbeam period. No new Flex circuits or support cards available, so a first module was built by recycling an old Flex and its support card (used for first 4-chip test of Flex and MCC).
- Had great difficulty again in bonding of FE chips, and some difficulty in bonding to Flex (due to poor attachment of Flex using too much Thermagon ?)
- Again, all chips worked. Found in several chips that there were a large number of channels which appeared dead to charge injection in chips with essentially no bumping defects. After some time operating the module, many of these channels would come back to life, and operate normally. Chip 0 was worst, with initially over 600 dead channels. This number varied between 100 and 600 over one week of testing. This is definitely something new, related to some residual film in active region of detector or electronics ?
- The module operated well, but the thresholds were not completely stable (they would vary by a few hundred electrons from one scan to the next). Also, the noise was not completely stable either, and some chips would occasionally show a non-uniform noise distribution with values of 200-300e instead of less than about 140e that would be expected. Note that the Flex 1.0 used for this module has very limited decoupling (0.01μF per supply per FE chip). These features are very different than for the IZM bare module, and could be due to power distribution decoupling on the old Flex 1.0...

Threshold scan results for Flex module:

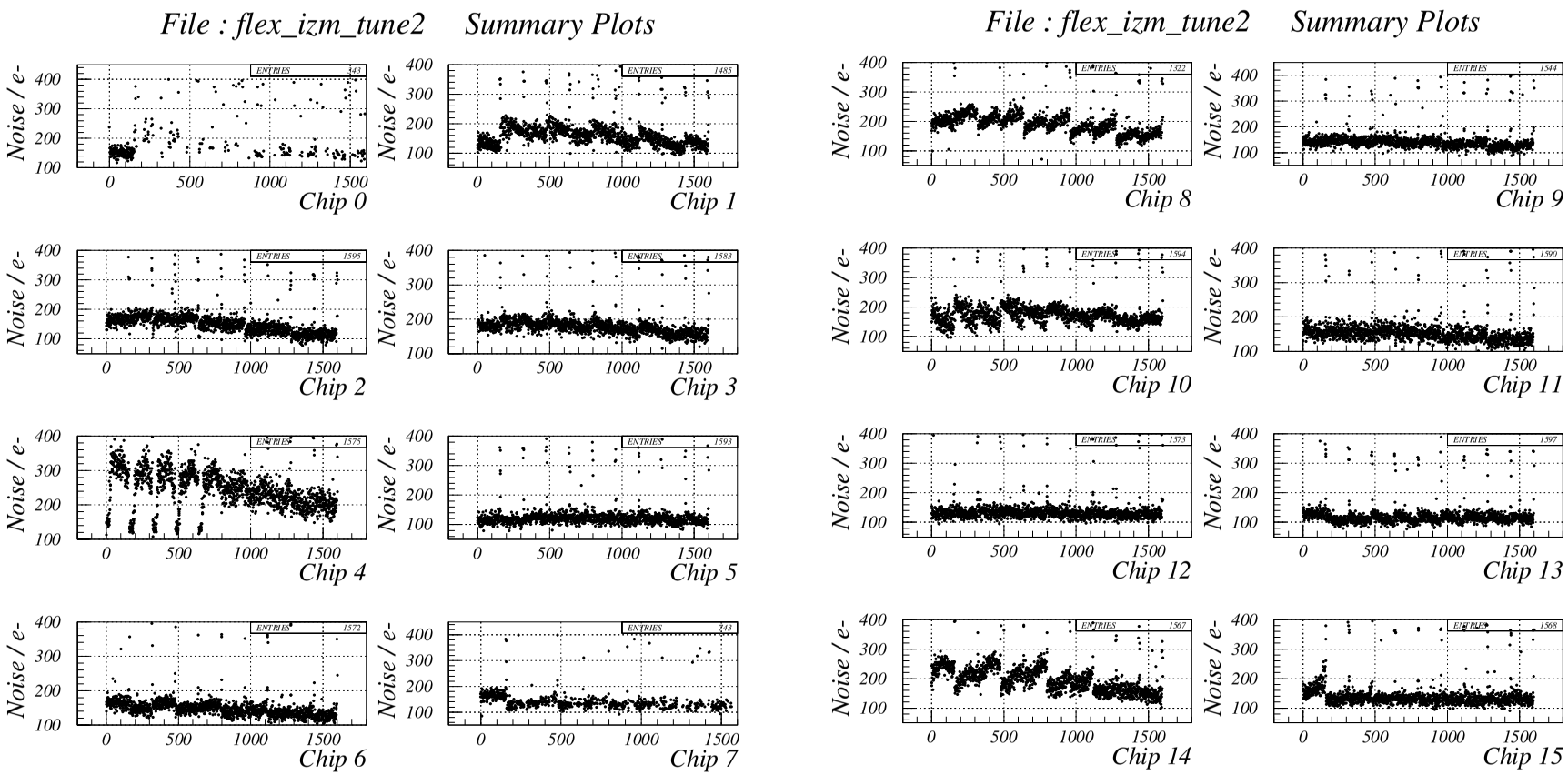






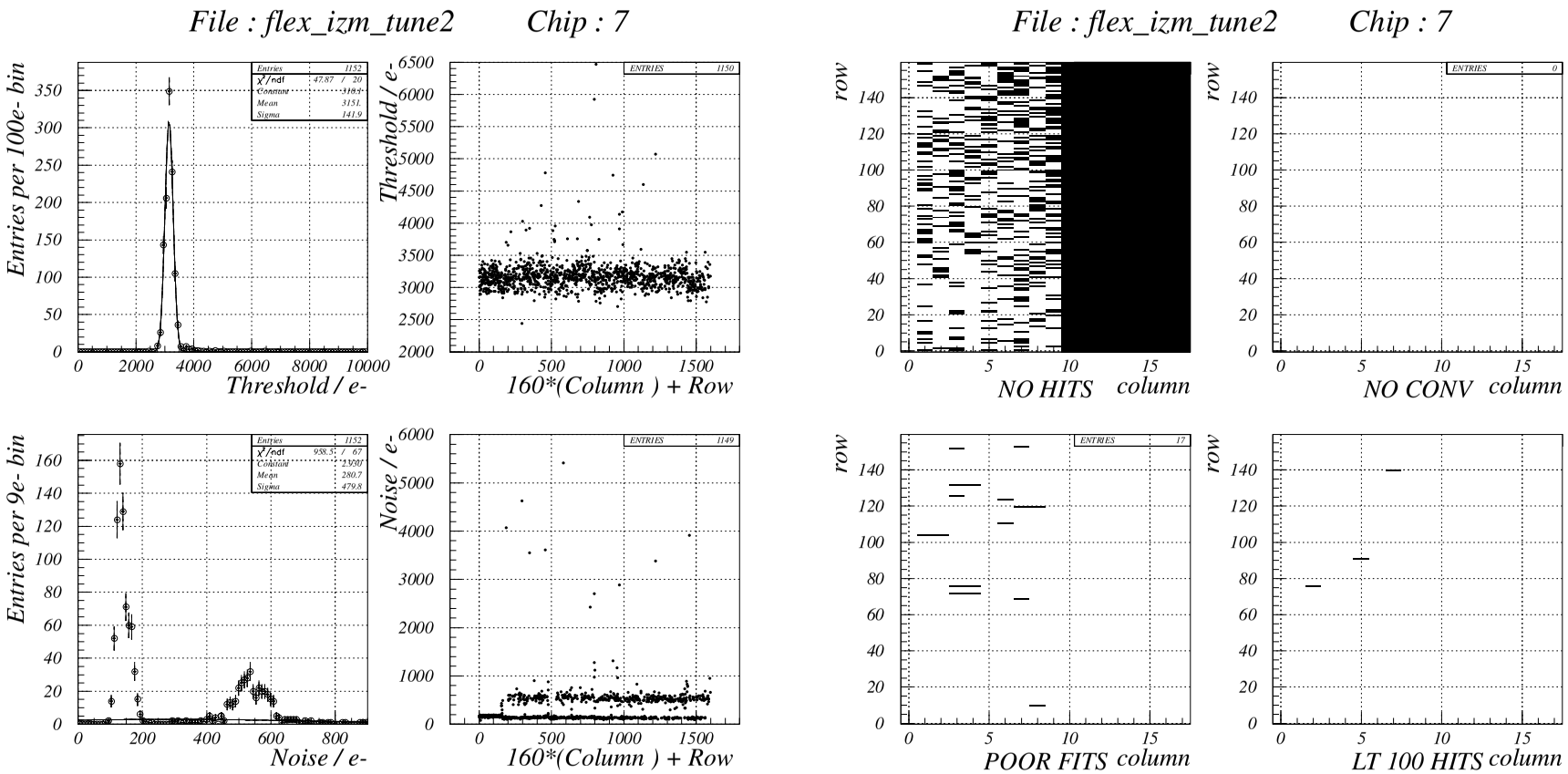
- Dispersion is good (215e) and noise is reasonable (mean about 150e) but has a tail to larger values not seen in bare module.
- Large number of bad channels (about 1300), mainly in chips 0 (600 bad) and 7 (400 bad), found in this scan.

- Looking at noise distributions for individual chips, can see some problems:



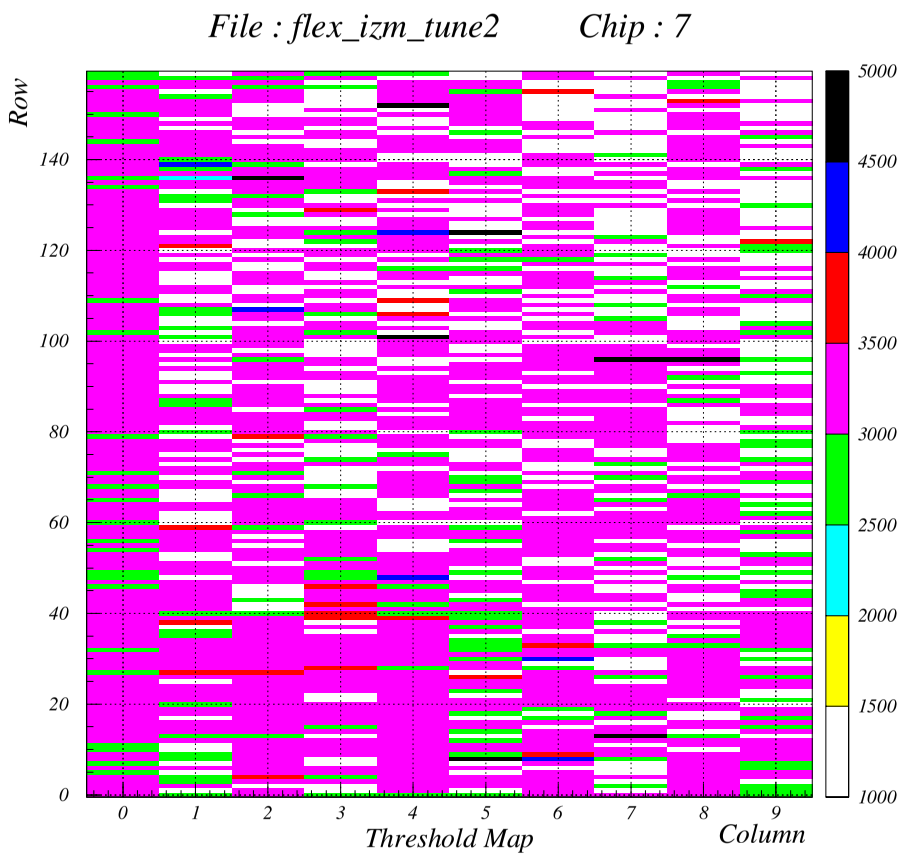
- Chips with large numbers of bad channels show high noise in nearby pixels.
- Some chips (not always the same from scan to scan) show high noise, for example chip 4 in this scan.

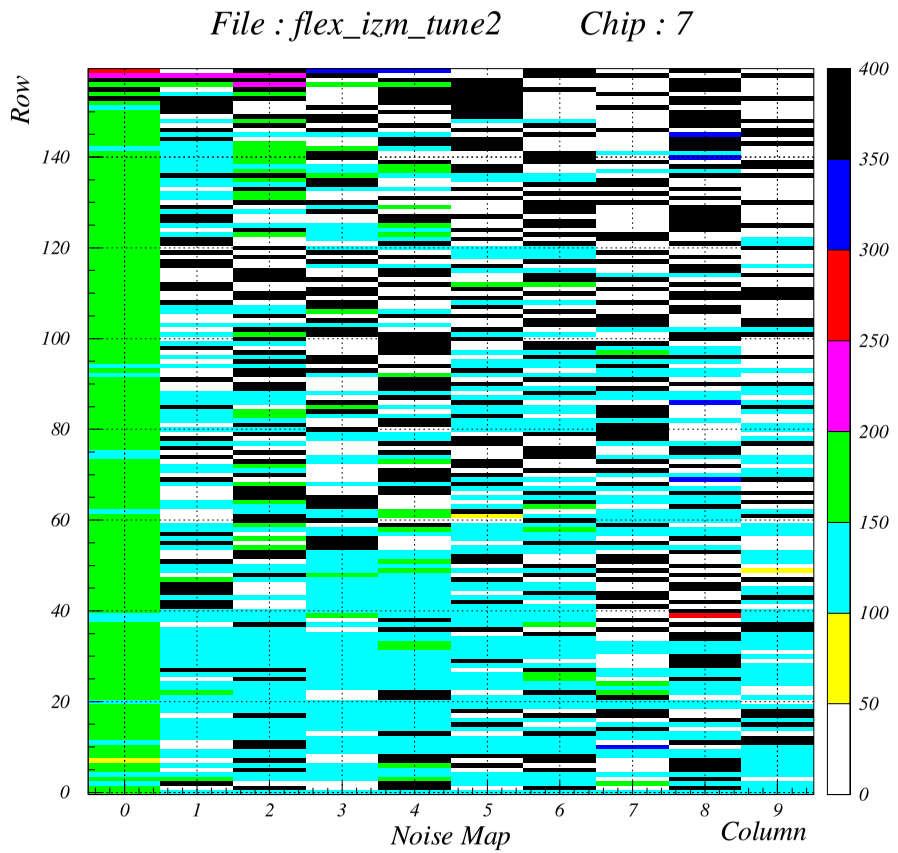
- Look in more detail at one chip which behaved very strangely (chip 7):



- For threshold scan, see large number of bad channels. Also see high noise in channels near those which are dead.

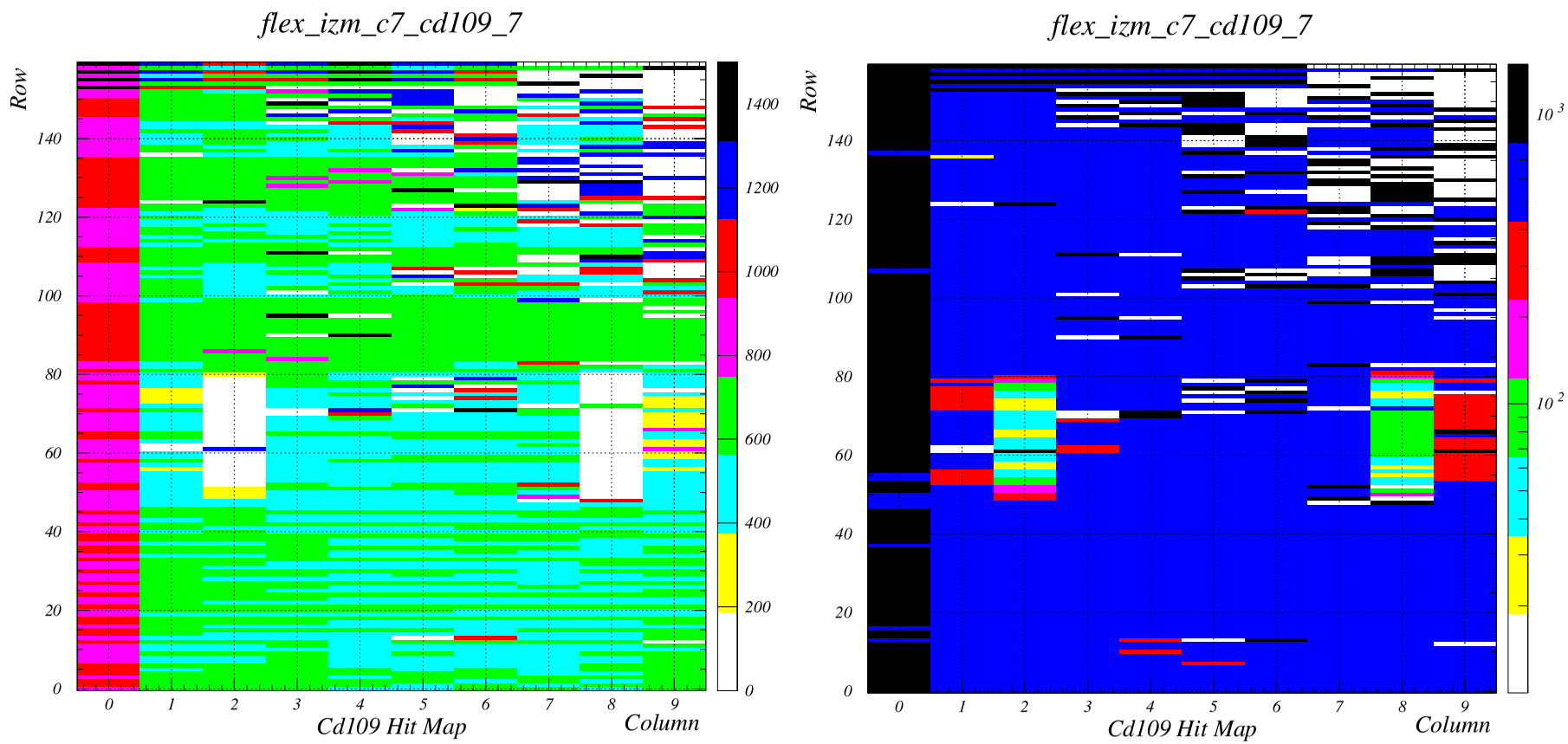
- Look at threshold and noise maps for this chip from this scan:





- See uniform threshold behavior, but anomalous noise behavior occurs in neighbors of “dead” pixels.

- Compare previous dead channel map to results of Cd109 source scan performed about one day later:



- All dead channels cluster in upper right corner, whereas in initial scan, they were distributed throughout the active region (except column 0).
- Note the visibility of individual traces on Flex in the pixel occupancy. It will be difficult to use low energy sources for production characterization of modules...

Summary

Measurements of FE-C performance done:

- Very significant non-uniformities observed in timing performance. Most of these can be attributed to the digital readout circuitry.
- Present timewalk performance does not seem to be good enough. Look forward to measuring more devices to check these results.

Measurements of FE-B devices done with laser:

- Excellent method for characterizing absolute timing performance. Present FE-B looks OK, but horizontal distribution of timestamps could be improved.

Measurements of first “bare” FE-B module from IZM:

- Performance was excellent in every respect, except for number of bump-bonding defects and problems with support card.

Measurements of first FE-B Flex module from IZM:

- Performance was good, but not as good as for the bare module. Now need to understand whether this is related to the particular module, or to the power distribution and decoupling, or something else. Look forward to testing modules with the new generation of Flex and Flex support card.
- In general, bump-bonding quality-control still seems to need work...