

# Electrical Services and System Test Overview

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## **Overview of pixel services from electrical viewpoint:**

- Describe components and their interconnections
- Outline requirements for services
- Detailed implementation will be described in following talks.

## **Summary of initial system test results:**

- Test of six module disk sector with realistic services
- Irradiation of 7 modules with realistic low-mass services

**Have a credible services design matched to our requirements**

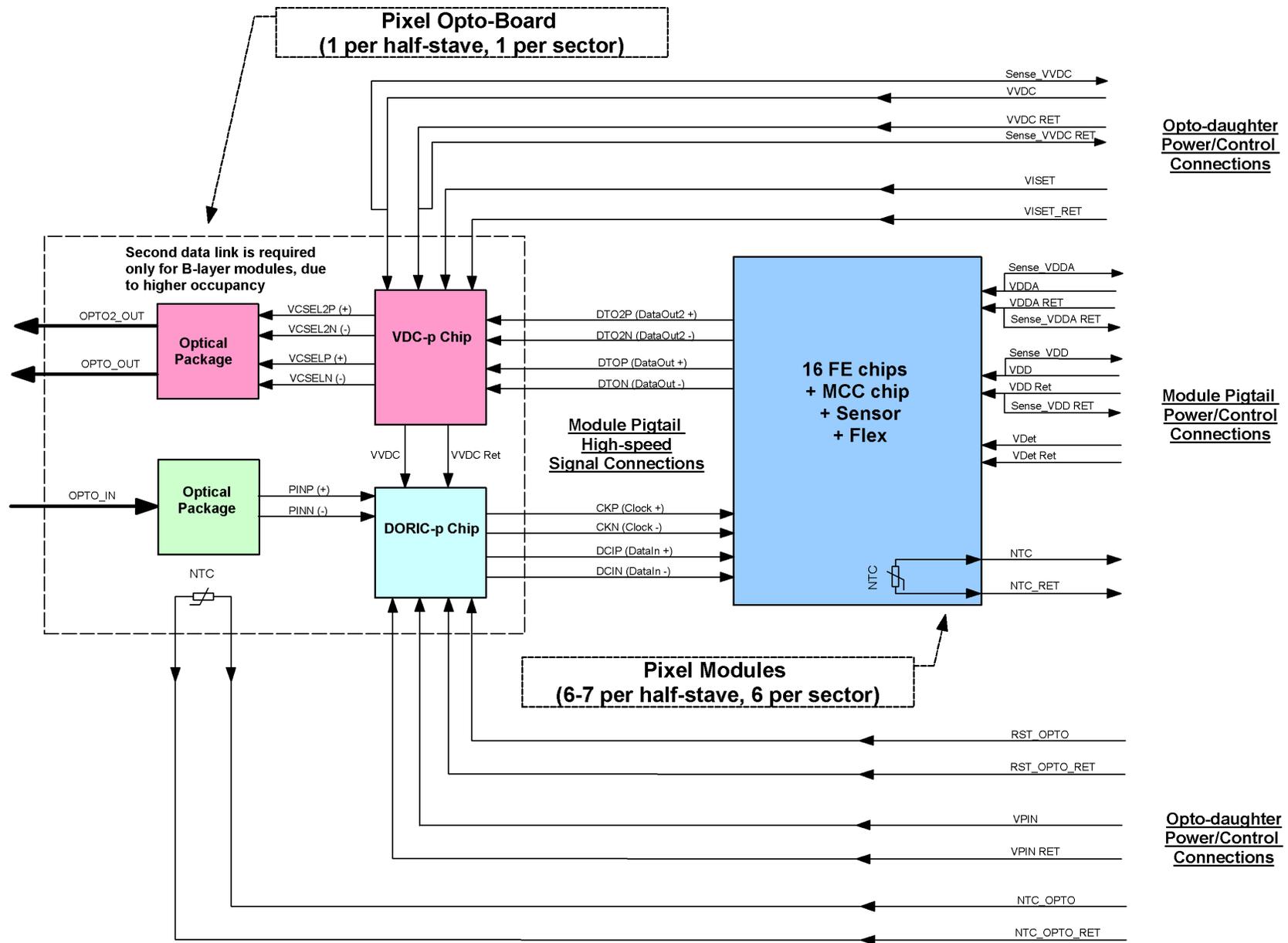
## Electronics components of pixel module:

- **Front-end chip:** Sixteen 7.4x11.0mm die per module, each containing 2880 pixels of size  $50\mu \times 400\mu$ , plus control of internal biasing and readout circuitry.
- **Module Controller chip (MCC):** assembles data from 16 FE chips into single event, and provides module level control functions, interface to opto-electronics.
- **Power requirements:** two low voltages (one analog and one digital) and one high voltage supply per module are required. Present grounding/shielding plan calls for separate floating supplies for each module.
- **Control requirements:** one temperature monitor is provided for each module. The temperature is used as part of the cooling interlock system, as well as for monitoring.

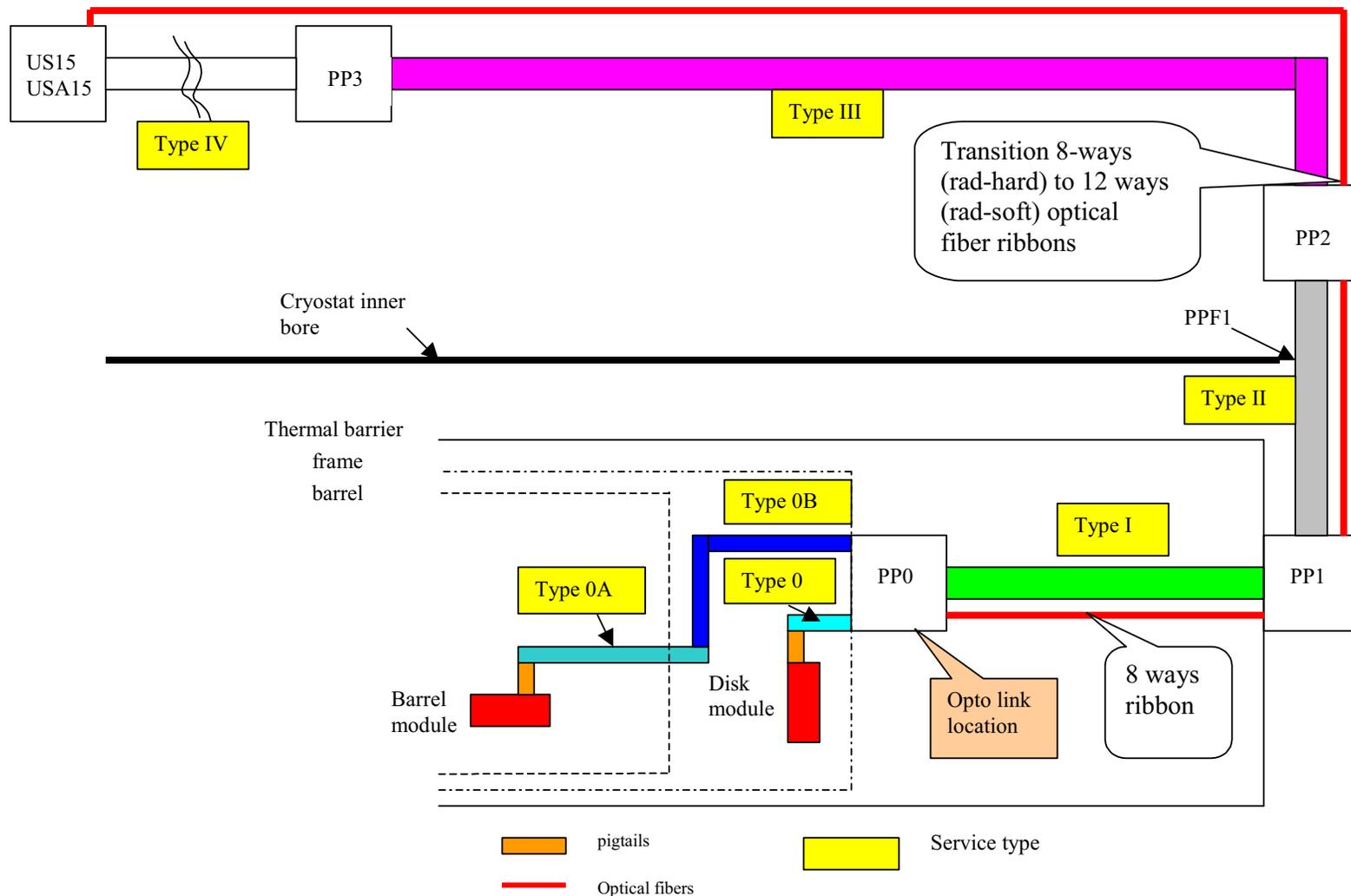
## Electronics components of optical interface:

- Optical interface is implemented as a single opto-board containing opto-links for 6 or 7 modules (disk sector or half-stave). These boards are located at PP0.
- Timing and control information are sent to each module using an individual biphasemark encoded optical stream. Data are returned from each module using 1 or 2 NRZ-encoded links which can run at either 40 or 80Mbit/s.
- **Opto-electronics:** timing and control information are decoded by DORIC chip which processes current from PIN diode. Return data are sent off-detector using a VDC chip to modulate the output of a VCSEL.

- Both opto-chips, as well as the VCSEL, operate from a common supply. The PIN requires separate supply. There is a separate opto-reset and temperature monitor.



# Geography and nomenclature for services:



- PP0 contains Opto-boards. PP1 is passive.
- PP2 contains low-voltage regulators. PP3 contains DCS monitoring and interlocks.

## Power distribution:

- Commercial floating power supplies are located in US15 and USA15, with a worst-case cable run of 140m from pixel detector.
- Power supply concept was originally based on “complex channels”, in which all supplies for a module were collected together into a single complex channel with a common interlock (like SCT). However, this limited vendor choice and proved too expensive, so there are now three types, LV module, HV module, and Opto.
- Present assumption is that from 2 to 6/7 modules are operated from a single power supply to reduce channel counts. The service implementation brings out individual module cables to provide maximum flexibility, but services are bundled into 6/7 module groups within individual cables.
- Each opto-board operates with its own independent power supplies to provide redundancy. Loss of even a single opto-board would be viewed as severe problem.
- Local rad-tolerant voltage regulators are placed at PP2 (roughly 12m from modules) and operate using remote sensing to compensate for large voltage drops on low mass cable plant and provide controlled LV for DSM electronics.
- The regulators are used for the high-current low-voltage supplies in the system (VDDA, VDD, VVDC). These are the only supplies which have significant AC currents, and hence need regulation as close to the detector as possible.
- All other supplies are quite static, and are driven directly from US15/USA15. The Opto\_Reset signal is treated as a floating power supply also.

## Module Power Budget:

- Original budgets were based on early prototypes in 0.8 $\mu$  processes with much more limited functionality.
- Based on significant experience with operating 0.25 $\mu$  technology modules, the typical values observed during operation for the digital current have increased. In addition, the digital current is sensitive to the noise occupancy, so if the thresholds are not tuned, IDD can move up towards 1000mA. Note however that this is a transient condition, not an operating condition.
- Operation of irradiated modules with sensor at -7C results in typical IDD = 750mA and IDDA = 800mA. The IDet sensor current is about 1mA, but can increase towards 2mA if the temperature control is poor. First testing of the final FE-I2 chip has shown that a new bias compensation feature increases IDDA more than expected, and could lead to IDDA = 1100mA. This needs further study.

<b>MODULE BUDGET</b>									
	SUPPLY TYPE	SUPPLY VOLTAGE (V)	SUPPLY CURRENT (mA)	NOMINAL VOLTAGE (V)	NOMINAL CURRENT (mA)	NOMINAL POWER (mW)	WORST VOLTAGE (V)	WORST CURRENT (mA)	WORST POWER (mw)
Layer B,1&2 Disks	VDDA	14	1500	2	970	1940	2.5	1290	3225
	VDD	14	1000	2	500	1000	2.5	800	2000
	VDET	600 (1)	2	600	1	600	600	2	1200
	<b>TOTAL</b>					<b>3540</b>			<b>6425</b>

## Opto-Board Power Budget:

- Budget is based on experience with previous generation of opto-chips.
- Experience with 0.25 $\mu$  chips gives lower values. Typical currents are DORIC (75mA for 4 ch) and VDC (15mA/ch for 10mA drive current), with worst case VDC (25mA/ch for 20mA drive current).

<b>OPTO-BOARD BUDGET (7 LINKS)</b>									
	SUPPLY TYPE	SUPPLY VOLTAGE (V)	SUPPLY CURRENT (mA)	NOMINAL VOLTAGE (V)	NOMINAL CURRENT (mA)	NOMINAL POWER (mW)	WORST VOLTAGE (V)	WORST CURRENT (mA)	WORST POWER (mw)
LAYER 1&2 DISKS	VVDC	14	581	2	280	560	2.5	490	1225
	VPIN	20	20	5	-		20	20	400
	VISET	7	30	1	-		2	30	60
	<b>TOTAL</b>								<b>1685</b>
B-LAYER	VVDC	14	931	2	420	784	2.5	770	1925
	VPIN	20	20	5	-		20	20	400
	VISET	7	30	1	-		2	30	60
	<b>TOTAL</b>								<b>2385</b>

## Comments on using 0.25 $\mu$ chips for on-detector electronics:

- Nominal maximum operating voltage for the chosen process is 2.7V. This is for reliable operation over lifetime of 10 years (100K hours).
- Maximum transient voltage is limited by multiple effects, including hot carrier effects and oxide breakdown effects. These effects can significantly shorten the lifetime, or modify the device performance for supply voltage much above 2.7V.
- The most severe issue are the breakdown and sustaining snapback voltages, above which short-channel NMOS devices can enter, and remain in, a high current, negative resistance regime, potentially leading to thermal destruction. This voltage is approximately 4.0V sustaining, and slightly higher for breakdown.
- Conservative design would ensure that chips could never see voltages close to this limit. In our services design, we have chosen worst-case round-trip voltage drops which should avoid sustained voltages above these limits. For the module voltages VDD and VDDA, have chosen worst case voltage drop from PP2 of 2V. For the opto-board voltage VVDC, have chosen worst case voltage drop of 1V.
- However, it is possible that given multiple time constants in our system of regulator plus long power leads, transients could appear with higher voltages. For this reason, have included overvoltage protection inside individual chips in module.
- The proposed system is not conservative. Extensive system testing will be required to ensure that it is reliable and meets all pixel detector requirements. Initial system test results are very encouraging (see later).

## Power Supply and Miscellaneous Connections

### Supplies required at module level (supplied by pigtail):

- One HV supply to bias sensor.
- One Analog LV supply for FE chips, with remote sensing to Pigtail.
- One Digital LV supply for FE chips and MCC chip, with remote sensing to Pigtail.

### Supplies required at half-stave/sector level (opto-board):

- One Digital LV supply for VDC and DORIC, with remote sensing to opto-board.
- One Analog LV supply for PIN diode bias. Very low current.
- One Analog control voltage (VISET) to adjust the VCSEL bias, low current.
- One Digital control voltage (Opto\_Reset) to reset DORIC in case it mislocks.

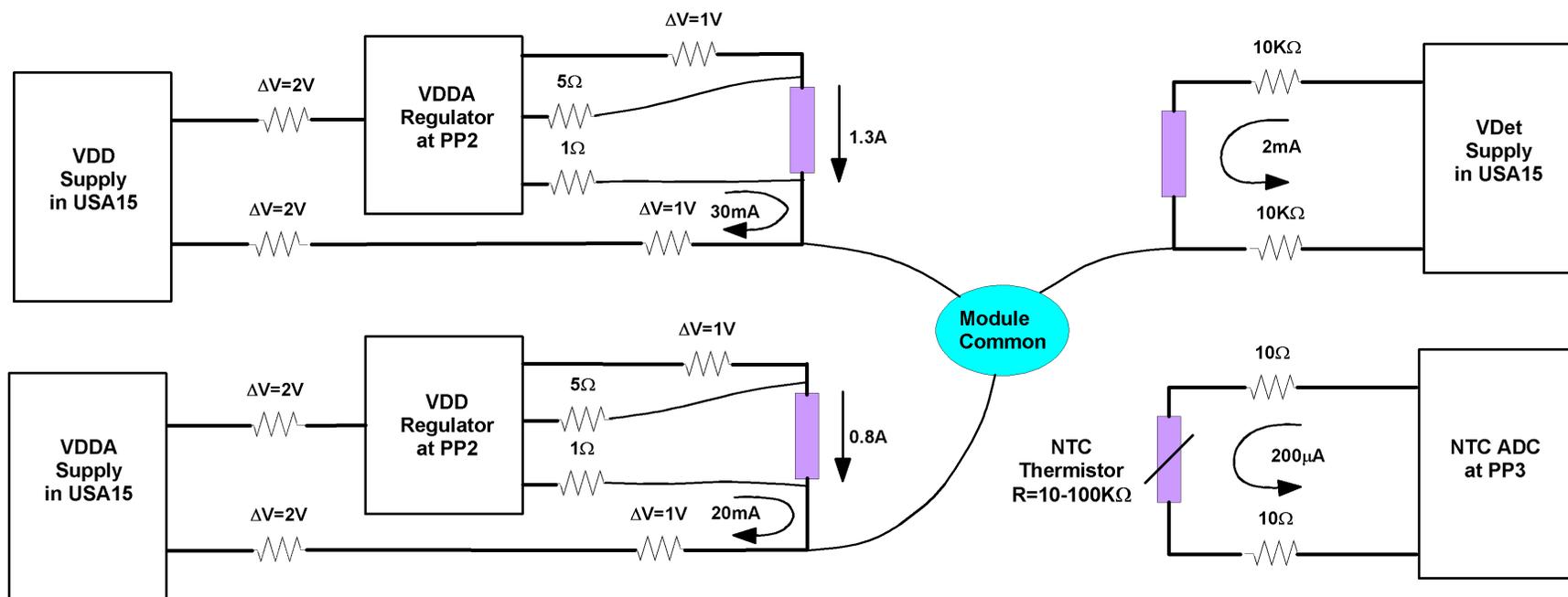
### Additional DC signals in module interface:

- **NTC** and **NTC\_Ret** are connected to a precision (1%) 10K $\Omega$  NTC thermistor used to monitor the module temperature (0603 part attached to Flex near module center). These signals are sent out at the module level, and are sampled by the I-box and digitized by the DCS system, both located near PP3.

## Service Connections for each Module:

- **Power (3 pairs):**
- VDD/VDD\_Ret, VDDA/VDDA\_Ret, VDET/VDET\_Ret
- **Sense (2 pairs):**
- Sense\_VDD/Sense\_VDD\_Ret, and Sense\_VDDA/Sense\_VDDA\_Ret
- **Temperature (1 pair):**
- NTC/NTC\_Ret
- **Optical (4 pairs):**
- XCK+/-, DCI+/-, DTO+/-, DTO2+/-
- **Test (1 signals):** VCal (Vcal appears as single wire on Type 0 cable for testing)
- **Comments:**
- This list includes a separate return for the NTC. This is preferred because the NTC measurement is made at PP3 in a hardware interlock, and hence needs to simple (no corrections required). The only other ground reference available at this point would be the VDET\_Ret, and sharing this is not the preferred solution.
- Have also chosen to route electrical connections for two data links per module everywhere. Strictly speaking, this should be necessary only on B-layer modules.
- Sense returns are sized like supply lines due to high regulator quiescent current.

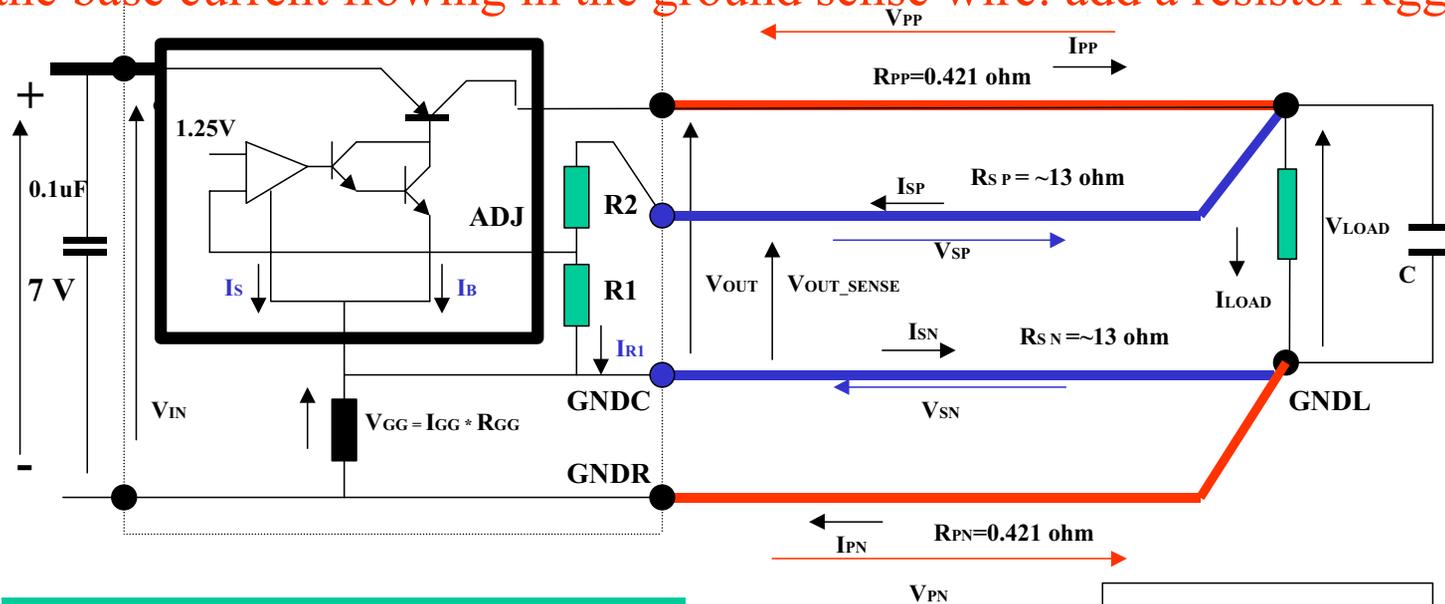
## Concept for power supply connections to module:



- Ideal situation is to have the Module Common point as the only commoning point for the current flows in the regulator error amplifiers. The NTC ADC (operating in voltage excitation mode with a 2V supply) would be isolated. Both sides of the HV supply are isolated by series resistors (may need to common return line).
- Present L4913 regulator has significant current flowing in the sense return line (about 2% of load current) used to control pass transistor. In this case, coupling the sense return lines at the module and at the regulator (20-30mV voltage difference under full-load conditions) will allow current variations in one supply/regulator to couple directly to the sensing network for the other supply/regulator.

- For this reason, we have prototyped, and will use, a scheme suggested by Jarron to compensate for the regulator quiescent current:

**Basic idea:** Use the voltage drop in the power wire to generate a current opposed to the base current flowing in the ground sense wire: add a resistor  $R_{gg}$



$$\beta = \frac{I_{LOAD}}{I_{BASE}} = \frac{R_{gg} + R_{SN} + R_{PN}}{R_{PN}}$$

13 m from Patch Panels to FE

GNDC - ground chip  
GNDL - ground load  
GNDR - ground return

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- With this scheme, there is essentially no effect of voltage drops in the sense return line, so the load regulation is much improved. We are using an  $R_{GG}$  of about  $20\Omega$ .

## Service Connections for Opto-Card

- Major concern for opto-card is reliability. Global failure on one opto-card will kill 6-7 modules. Some compromise necessary, but no data on expected failure modes.
- Intend to use series resistors to partially isolate VASET for different chips. Do not believe that shorting of VVDC is likely failure mode.
- Current working design has modularity of 1 for all supplies, with all VVDC for a given opto-board connected on PP0.
- **Power (1 pair):**
  - VVDC/VVDC\_Ret
- **Sense (1 pair):**
  - Sense\_VVDC/Sense\_VVDC\_Ret
- **Analog Control (1 pair):**
  - VASET/VASET\_Ret: voltage with 1V providing default VCSEL drive of 10mA.
- **Analog Power (1 pairs):**
  - VPIN/VPIN\_Ret
- **Temperature (1 pair):**
  - NTC\_OPTO/NTC\_OPTO\_Ret
- **Opto Reset (1 pair):**
  - RST\_Opto/RST\_Opto\_Ret

## Voltage Drop Budgets

- Relevant only for the high-current low-voltage supplies VDD, VDDA, and VVDC.
- For low-mass part of services (PP2 inwards), general guideline for high-current supplies was to allow a 4V maximum regulator output due to maximum 0.25 $\mu$  process voltage limits (discussed previously).
- For the module supplies, this implies a 2V maximum drop. For the opto-boards, this implies a 1.5V maximum drop.
- Require a minimum of 1V available for drop across regulators, and then add 1V of safety margin.
- Detailed allocation of voltage drops was done in such a way as to minimize the amount of material in critical parts of the detector (small  $\eta$  region).
- Additional voltage drop across Type 3 cables back to US15 and USA15 is limited by the allowable power dissipation in the cavern, and reflects an optimization between the extra power supply cost for higher output power, and the extra cable cost for lower voltage drop. Our present studies have led us to chose a 10V maximum supply output and a 3.5V voltage drop budget for Type 3 cables.

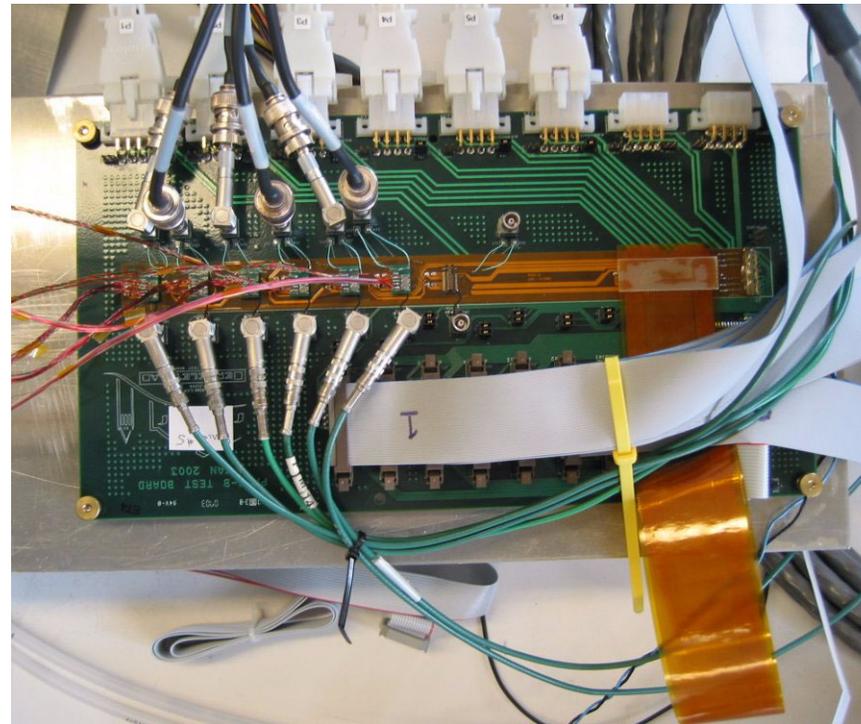
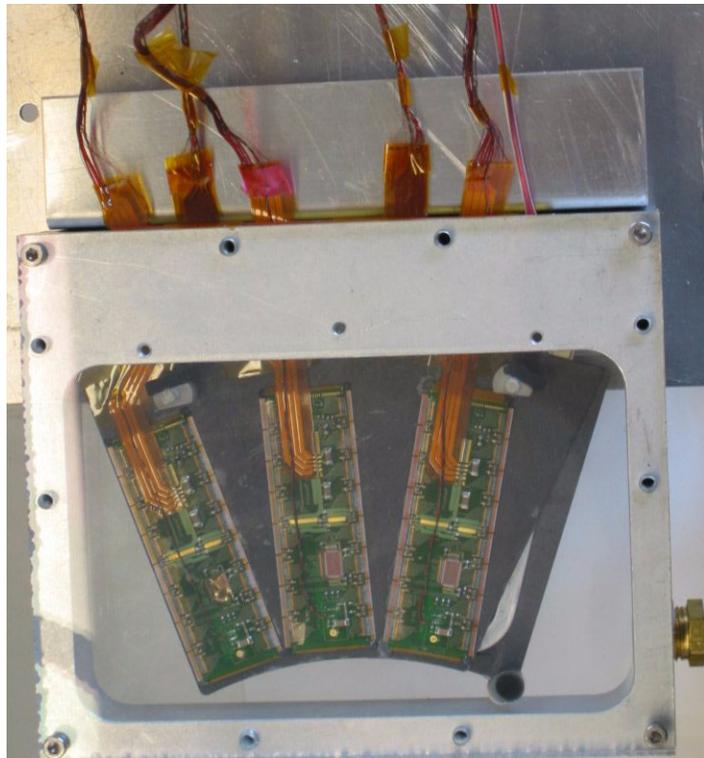
•Voltage drop budgets used as a basis for services design:

NAME	REGION	MAX LENGTH (m)	VDD/VDDA VOLTAGE DROPS (V)		VVDC VOLTAGE DROPS (V)
			Barrel module	Disk module	
Flex circuit	On module	-	0.1		-
Opto board	PP0	-	-	-	0.1
Type 0a (*) barrel	Along the stave	0.45	0.4 (1)		-
Type 0b barrel	End stave – PP0	0.75	0.15		
Type 0 (*) disks	Disk volume	0.35		0.2	-
Type I	PP0 – PP1	2.8	0.3 (1)		0.5
Type II	PP1 – PP2	9	0.85		0.85
<b><i>SUBTOTAL</i></b>	<b><i>Module-PP2</i></b>	<i>13 (barrel) 12.15 (disks)</i>	<b><i>2</i></b>	<b><i>1.65</i></b>	<b><i>1.45</i></b>
Voltage regulator Dropout	PP2		1		1
Type III	PP2 – PP3	20	0.5		0.5
Type IV	PP3 – USA15/US15 (2)	120	3		3
<b>GRAN TOTAL</b>	<b>Module-power supplies</b>	<b>153</b>	<b>6.5</b>	<b>6.15</b>	<b>5.95</b>

- Note there are no longer Type 0a and 0b cables, they are a single long micro-cable.
- Also recent detailed routing studies for disk Type 0 cable indicates that the present design will have a voltage drop similar to that for the barrel.
- Finally, note for low voltages, Type 3 and Type 4 have been combined (no PP3).

## System Test and Irradiation Results

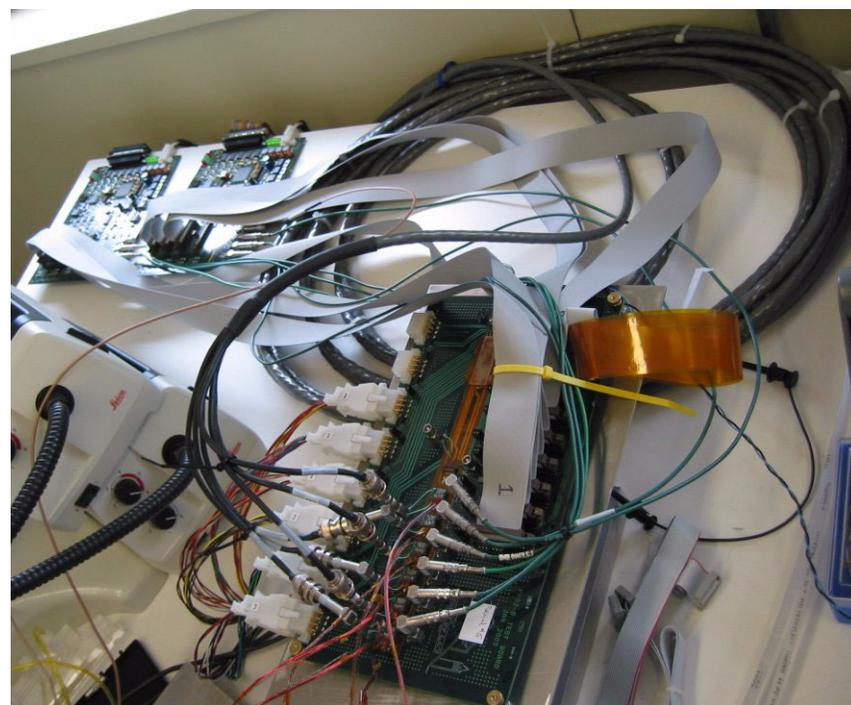
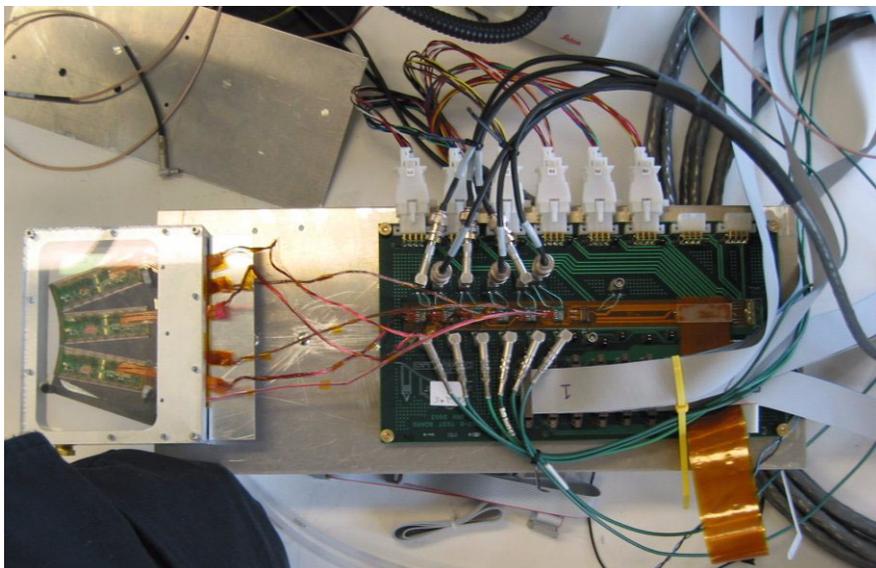
- Disk sector with six disk modules mounted (left) and connected to PP0 Support board (right) with all services for operation:



- Five of the disk modules are of the older “pigtailed” variety. LBL\_15 and LBL\_16 are the new “pigtail-less” variety. Length is about 30cm, shorter than in final detector.
- The PP0 Support board provides connections for LV, HV, VCal, and the TPCC connections for readout, roughly equivalent to PP0/PP1 functionality.

## Readout setup

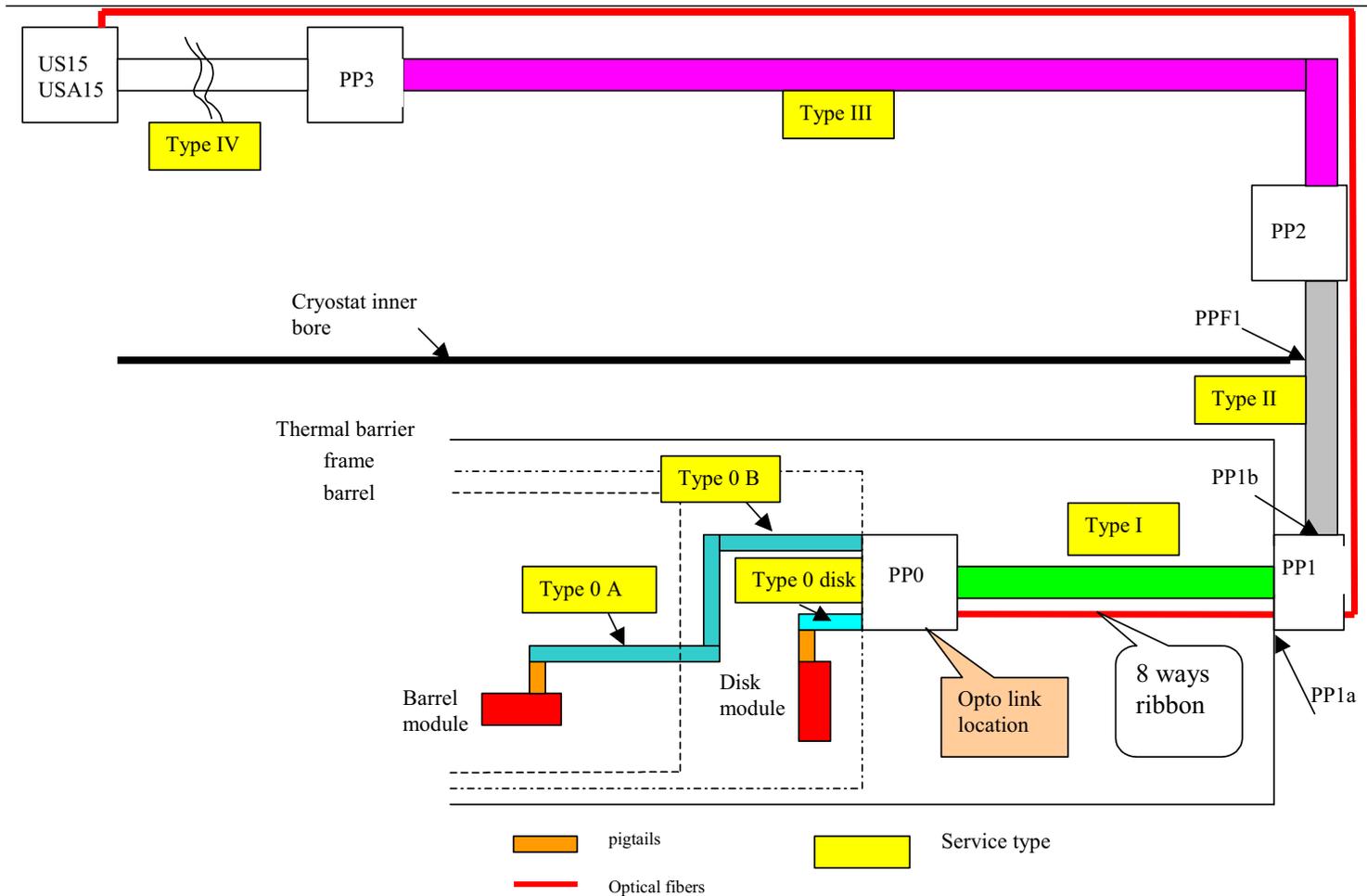
- Top three modules were read out with one TPLL/TPCC. Bottom three modules were read out with a second TPLL/TPCC. However, both TPLL were in the same VME crate, and were read by the same PC. A Desktop Manager (Flash Desktop) was used to provide multiple desktops for running multiple copies (two) of TurboDAQ.



- Due to resource conflicts, this did not allow true, concurrent, multi-module readout of both sides of the sector. It does allow generating concurrent activity in modules on same side of the sector (hits, triggers, and output data). RODs needed for final multi-module testing.

## Services setup

- Services setup is intended as a realistic electrical representation of the final services scheme, with reasonable wire lengths and gauges.



- PP0 is represented by the PP0 Support board. Type 1 and Type 2 cables are combined into a single 12m cable. Type 3 and Type 4 are combined into a single 140m cable.

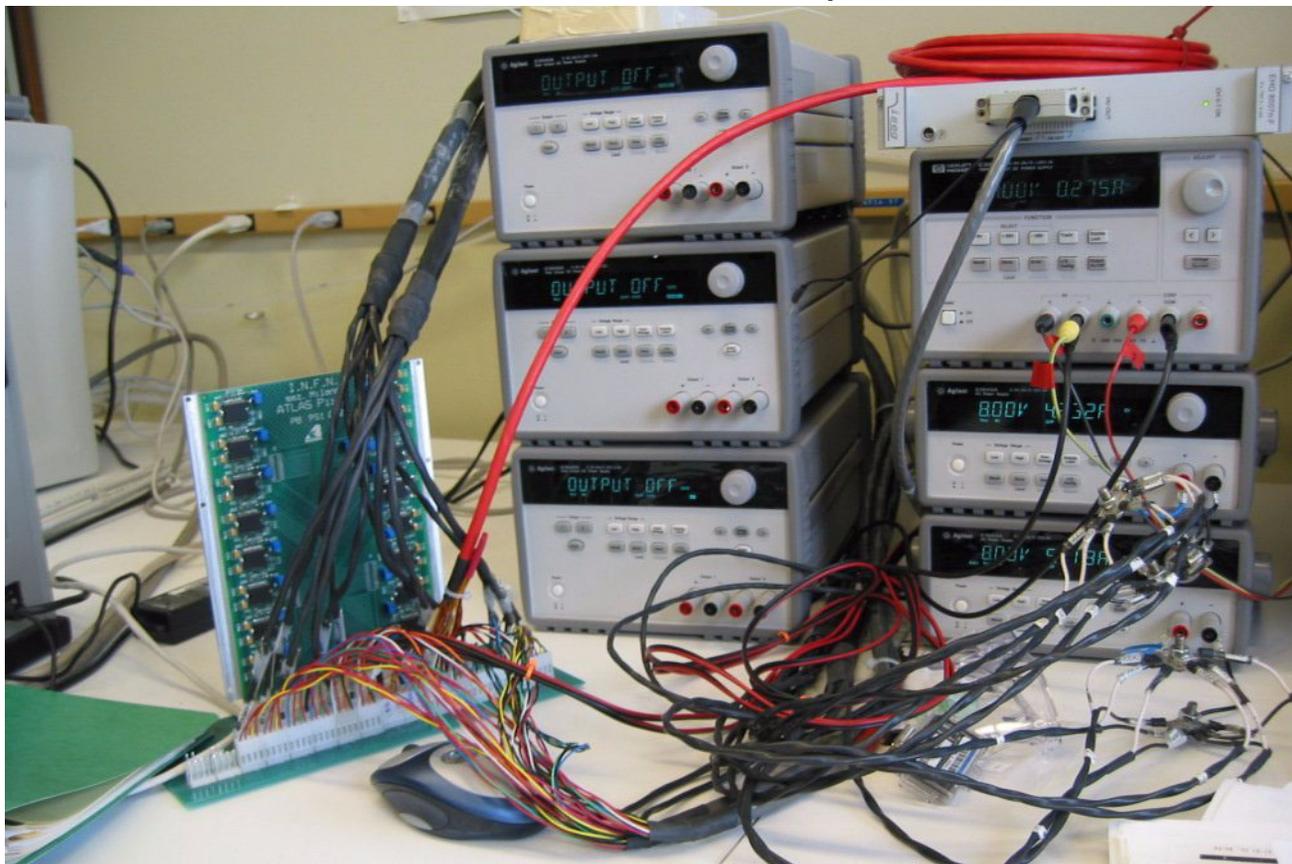
## Cables:



- On the left are two large rolls for 140m 6-pair AWG16 twisted-pair Type 3 cables (total mass about 100kg), connecting the Agilent LV supplies with the regulator board. One cable is for VDD and one cable is for VDDA.
- On the right is a roll for 150m 6-pair AWG24 twisted-pair Type 3 cable for the ISEG HV supply. The chosen wire gauge was the smallest with an acceptable voltage rating.
- Also visible is a chiller for cooling the sector (monophase liquid cooling).

## Regulators:

- Used first prototype ST regulator board from Milano. Regulators were operated in remote sense mode, but without “current compensation”:



- In this case, individual 8A supplies were used to power all six modules simultaneously, with one supply providing VDD, and the other VDDA.
- Used 8V output voltage to conservatively guarantee correct voltage at module.

## Low Voltage:

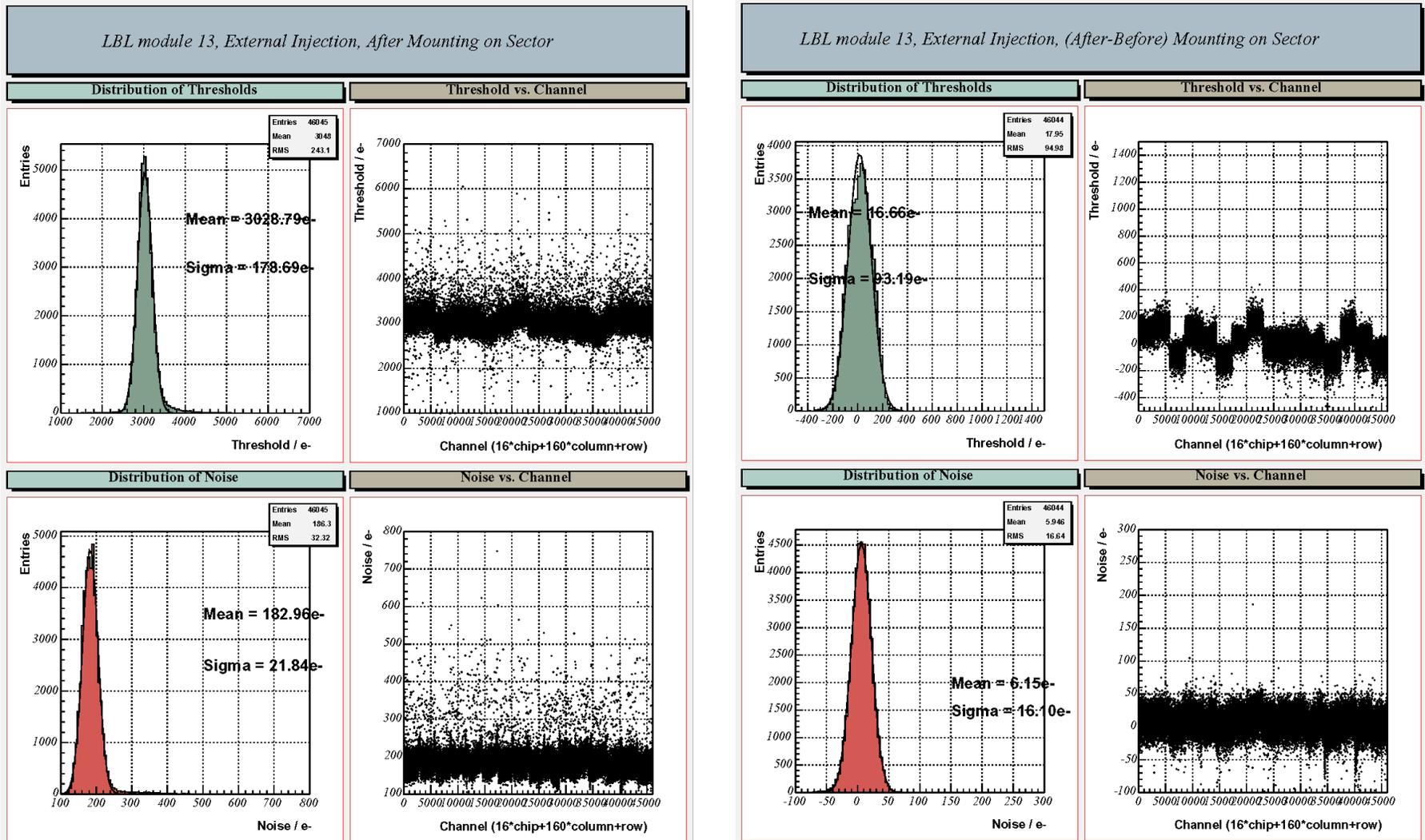
- Agilent lab supplies used for LV. Have tried multiplicity one (three supply pairs used to operate three modules), multiplicity three (one supply pair for three modules), a mixed multiplicity three for the top three modules and multiplicity one for the lower three modules, and finally, multiplicity six with all modules operating on a single supply pair.
- Regulator board always supplied one module per channel pair. Multiplicity n was implemented by connecting the long cables together at the supply end, just as it would be with our baseline detector using multiplicity one services and multiplicity up to six power supplies.

## High Voltage:

- A single ISEG supply was used to control the HV, with multiplicity = 1. This was not very realistic, but ganging of HV channels would be difficult due to the complex connector on the ISEG module.
- The control of the high voltage was implemented in TurboDAQ. Unfortunately, the DLL from the vendor is not reliable, and causes TurboDAQ to crash on a daily basis.

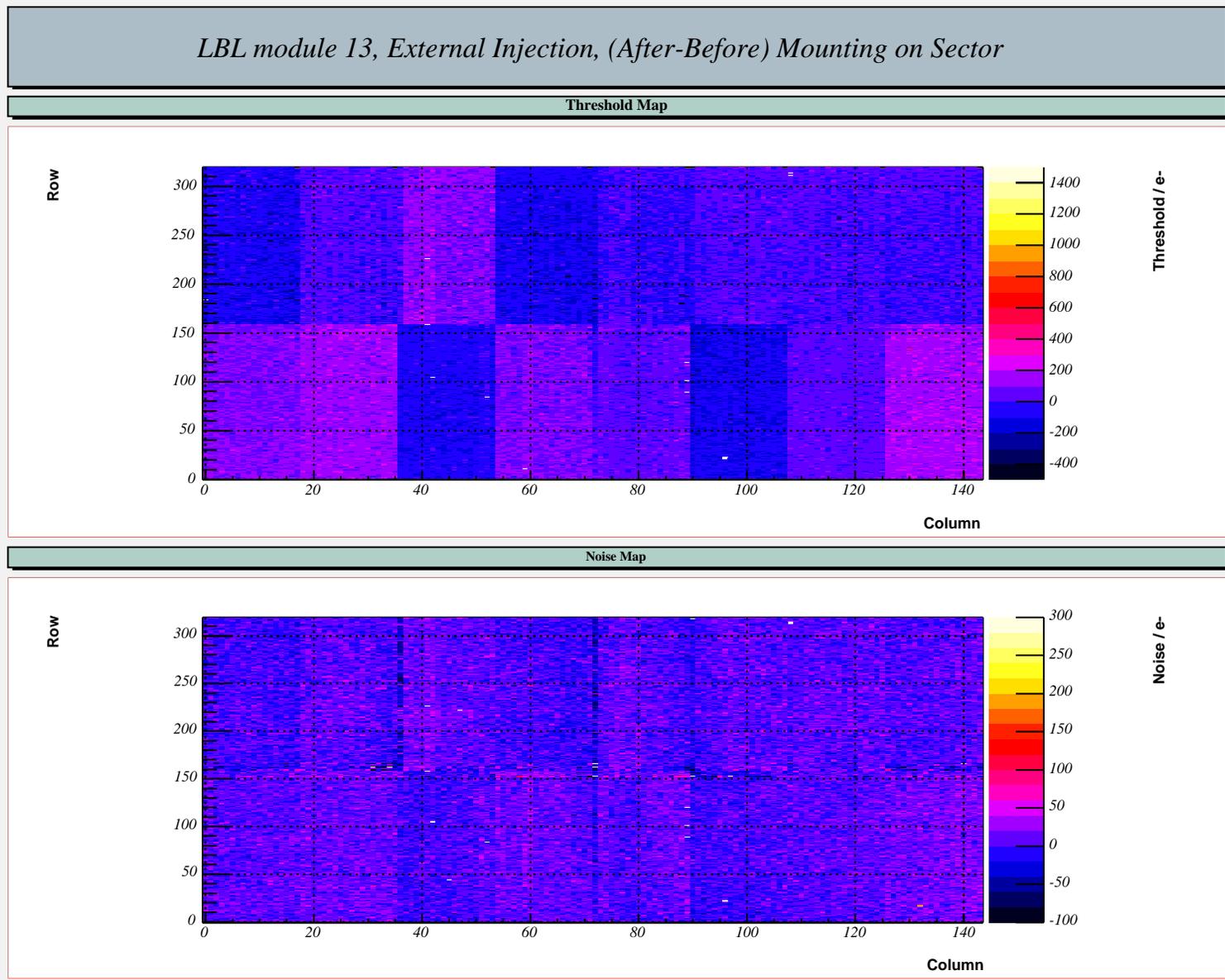
## Performance of Six Module Sector

- Compare threshold scans made with single modules in the lab and with modules mounted on sector. LBL\_13 shows similar noise, increased dispersion due to  $\Delta T$ :



- Left plot shows scan on sector, right plots show difference (after-before).

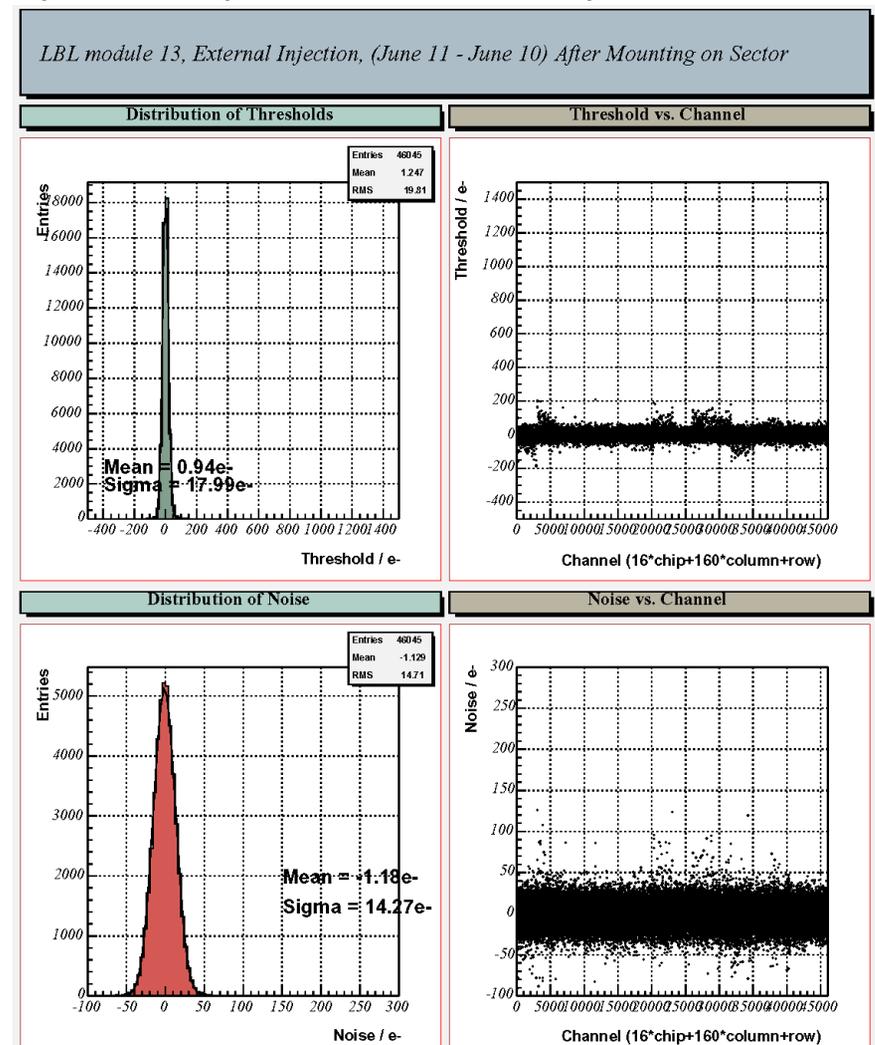
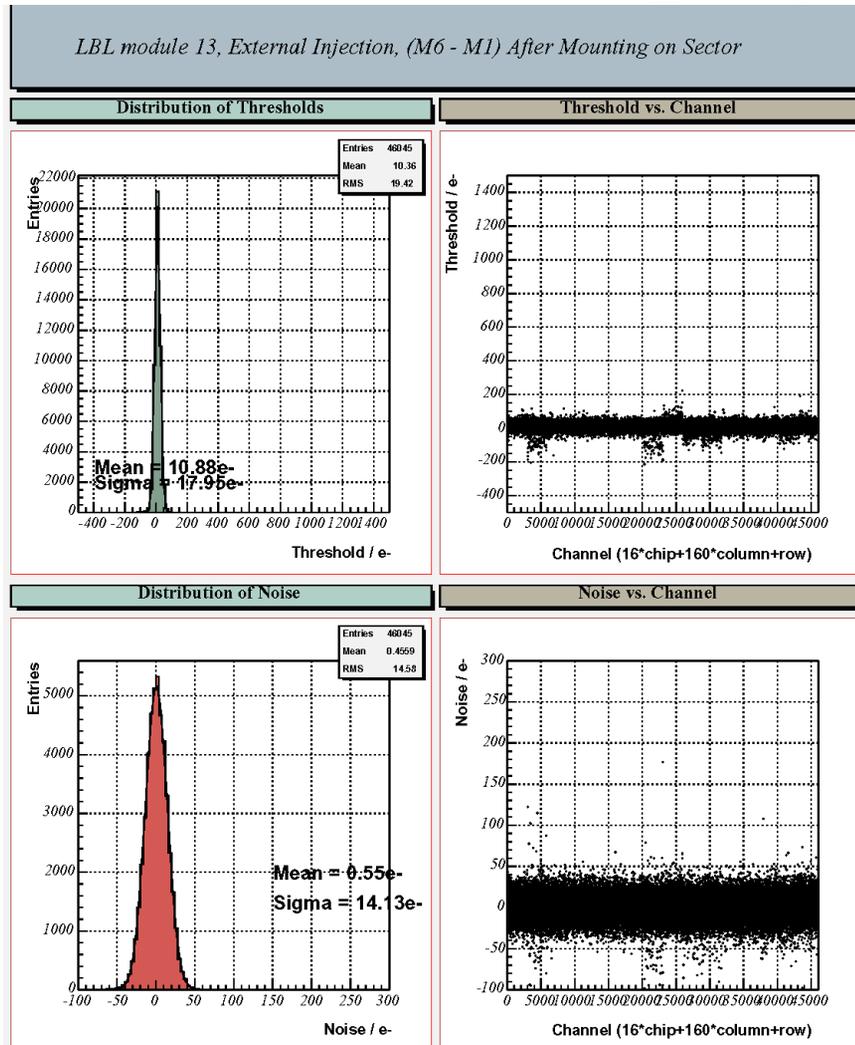
•Map of differences for LBL\_13:



•No significant differences seen.

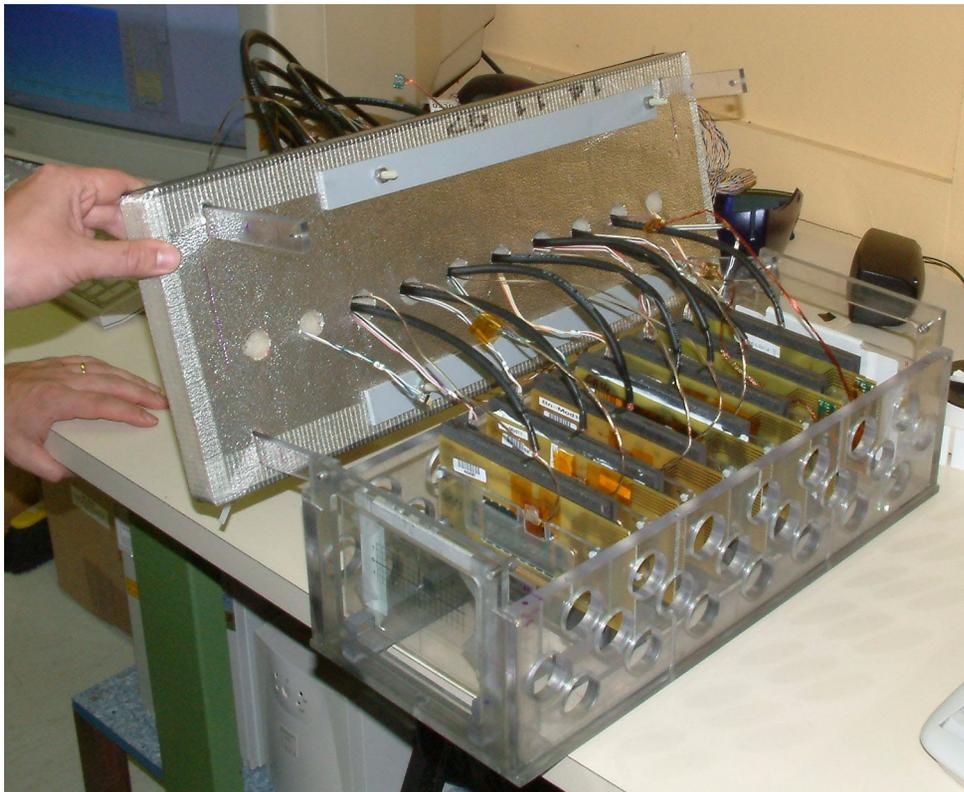
# Comparison of Operation with Supply Multiplicity of Six

- Compare LBL\_13 behavior on sector with multiplicity one and six. Also, compare two different scans of LBL\_13 separated by one day to check stability.



- No significant changes observed. Note all three modules on bottom of sector strobed and triggered simultaneously during these scans.

## PS Irradiation setup:



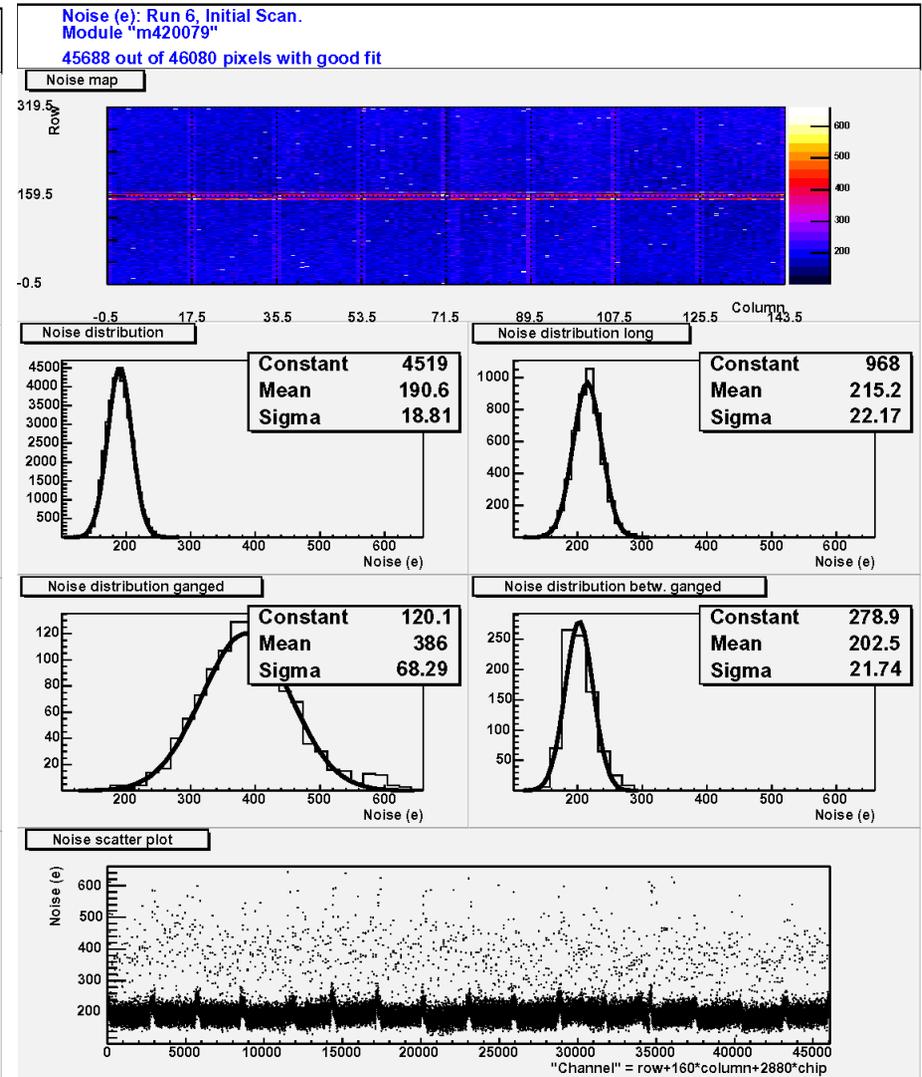
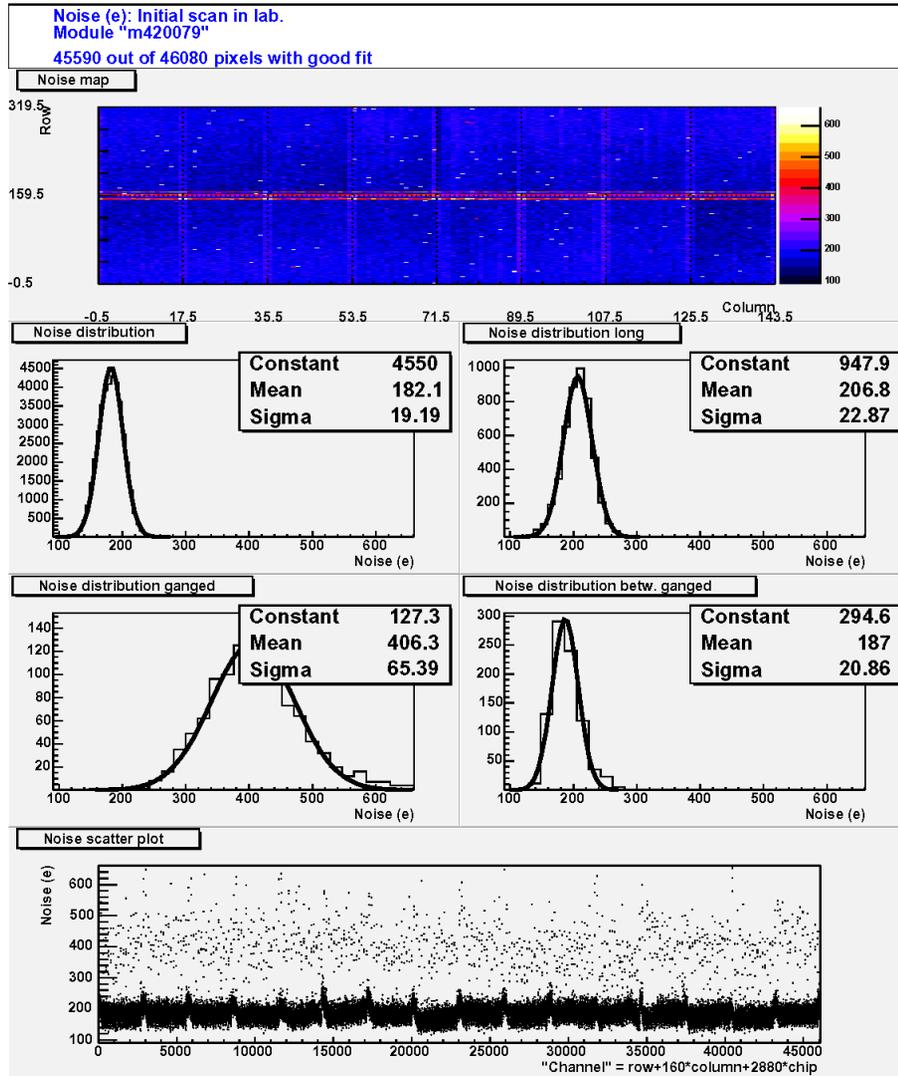
Modules are located in plastic basket, which is suspended from top of box.

PP0 Support card on top of box is crosspoint for electrical services. Type 0 is 60cm long.

Cooling valves are at lower right in beam.

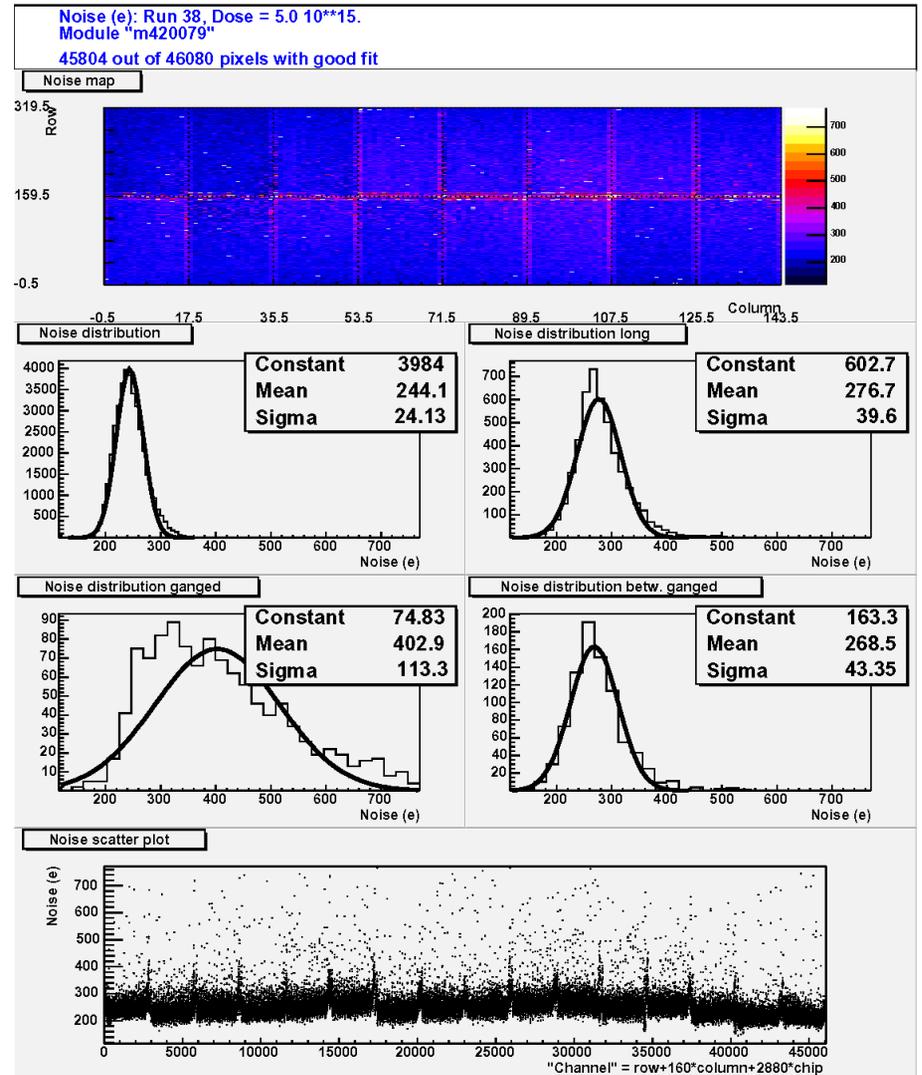
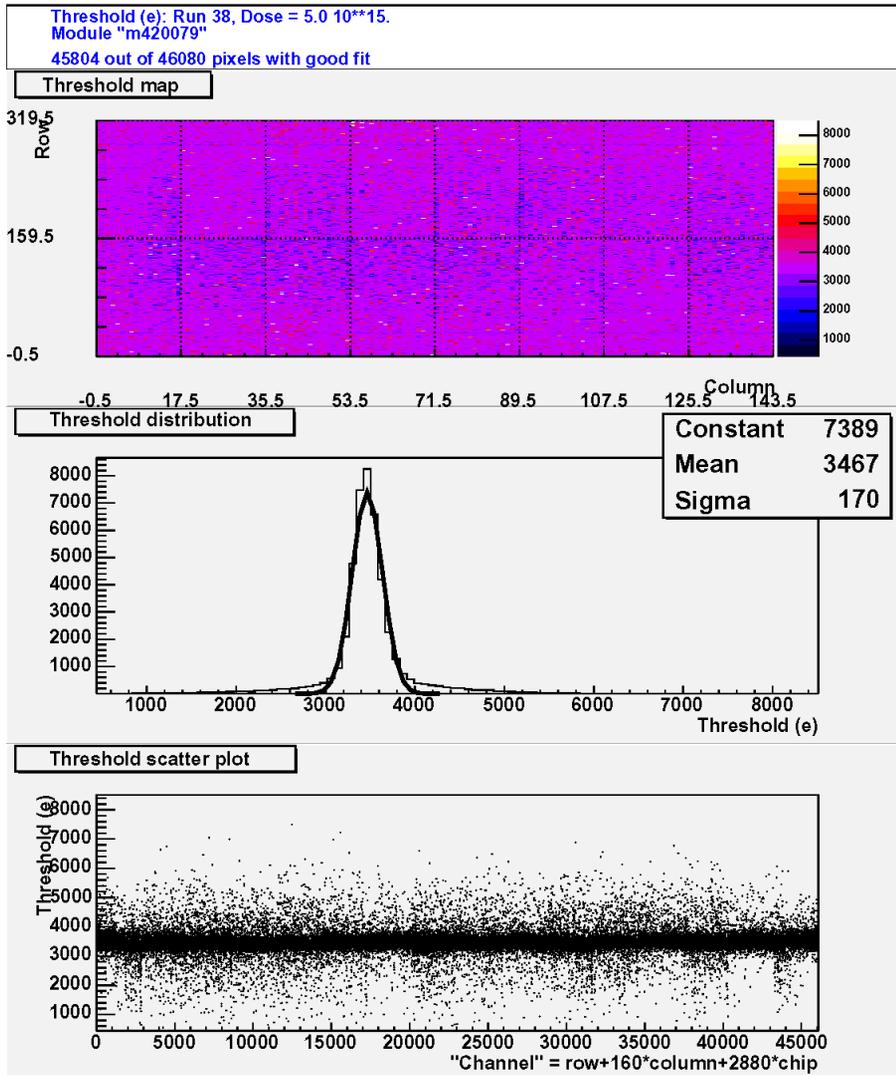


- Noise performance, using regulators and remote sense with low mass services, was almost identical to that in the lab (left in LBL lab, right installed in T7 at -7C). For example, normal pixels had mean 182e on left, 191e on right):

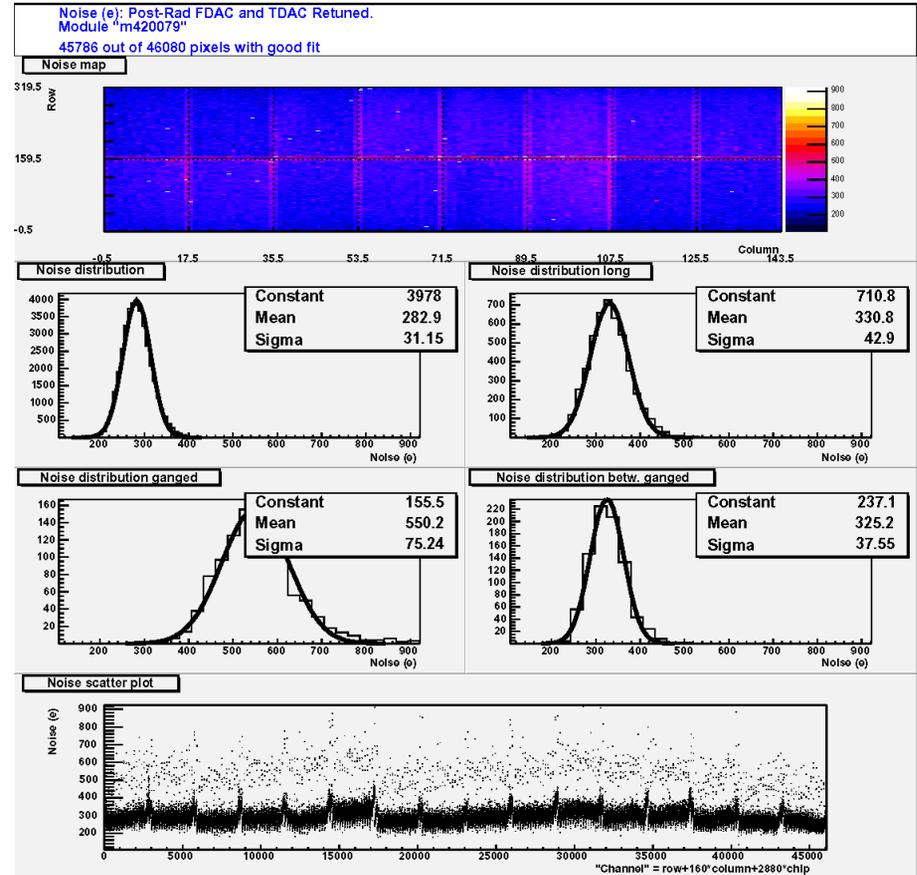
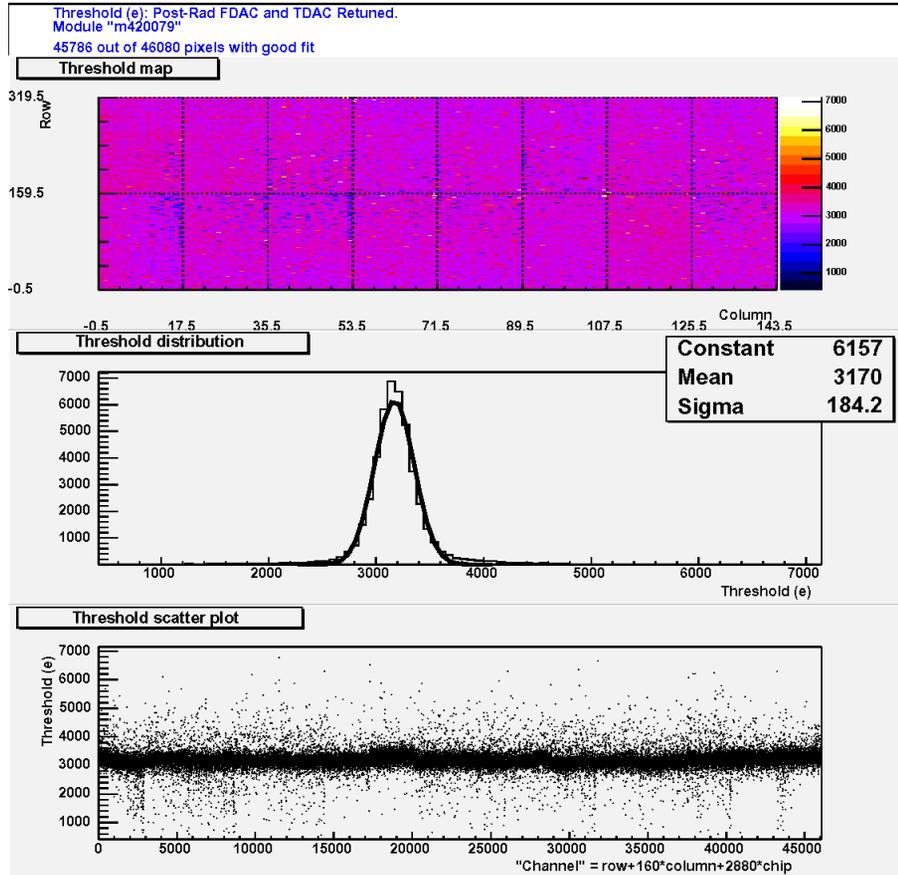


- Note PS regulator board used "current compensation" scheme without problems.

- After acquiring about half of the total dose (about 20MRad), two modules were chosen for re-tuning. Retuning was performed in situ, and results of confirmation scans are shown below, indicating that the modules continued to work well with realistic low-mass services:



- Performance in lab after irradiation to an average dose of about 30MRad, with modules operating in -25C environment to achieve -7C on sensor, and using the same remote sensing regulators and low mass services as at the PS, looks good:



- Noise has increased to 282e for normal pixels due to leakage current after estimated average dose of 30MRad (dose in module center closer to 50MRad). Measured leakage was about 20nA per pixel on average.

## Summary

### Overview:

- Presented basic electrical requirements for pixel services, based on current budgets for on-detector electronics. These budgets are conservative for the opto-services, but less so for the module services.
- Introduction of 0.25 $\mu$  electronics into pixel detector places stronger constraints on delivery of voltage to modules. Introduction of Rad-Tol regulators at PP2 looks essential, but raises reliability and stability issues that require significant testing.

### Test Results:

- First round of limited-scale system tests using the full services chain have been successful. Larger scale tests (multiple staves) are in preparation. Further aggressive studies remain, including examining bad grounding schemes and injecting noise into the cooling structures and cables.
- Similar service chains have also been used in recent PS irradiation, demonstrating that the services model also works for irradiated electronics.