

Status of Upgraded PLL Test System

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Focus on testing of FE-I chips and modules

- Overview of system components
- How are production needs covered
- Present status of boards
- New support cards
- Plan for FE-I Testing

Components of new system:

New PLL with improvements in several areas:

- Upgraded FPGA to allow continued code development.
- Increased SRAM (16MB in stead of 2MB) to allow module histogramming.
- Addition of programmable XCK generation over range 15-110MHz, and inclusion of FIFO's between present PLL core and output cable to decouple speed of PLL and speed of communication with device under test.
- Addition of support for DTO2 (second serial link from MCC).
- Support of HitBus operation as alternative to digital readout via DTO.
- More NIM outputs for more flexibility (XCK, STR, LV1).

New PCC with minor improvements:

- Support for diagnostic HitBus mode without XCK to device under test.
- Include on-board 16-bit chopper for VCal with settable VLow and VHigh.
- Include support for DTO2 (minor modification to 50-pin connector pinout).
- Include support for temperature measurement with 10K NTC thermistor on module (minor modification to 50-pin connector pinout).

New PICT module (Pixel IC Tester):

- Include PCC core for basic functions.
- Provide direct interface to probe card using new 100-pin MDR connector and shielded flat cable for good high frequency performance.
- Provide fully programmable generation of all output signals (control delay, width, and amplitude) and on all input signals (control delay, width, and threshold) using Pin Drivers and comparators.
- Signals under detailed control are: CMOS inputs (CCK, LD, DI, RSTb), addresses (GA0-GA3), LVDS inputs (XCK, STR, LV1, SYNC), and LVDS output (DO/DTO and DTO2). In addition, provide MCC input (DCI) to support either direct interface to single chips or interface to module via MCC.
- Provide Monitoring functions for all critical voltages and currents. All DAC currents and MonRef are measured as currents across small resistor. Power supplies VDD, VDDA are measured using local sense to correct for voltage drops. Currents $I(VDD)$, $I(VDDA)$ are measured with small series resistor and two ranges, one for single chip, one for module.

Probe Card Adapter:

- Contains minor active circuitry for PICT operation (decoupling, buffers for returning LVDS: MonHit, DTO, DTO2, and generation of XCKR).

Production and Lab Testing Configurations

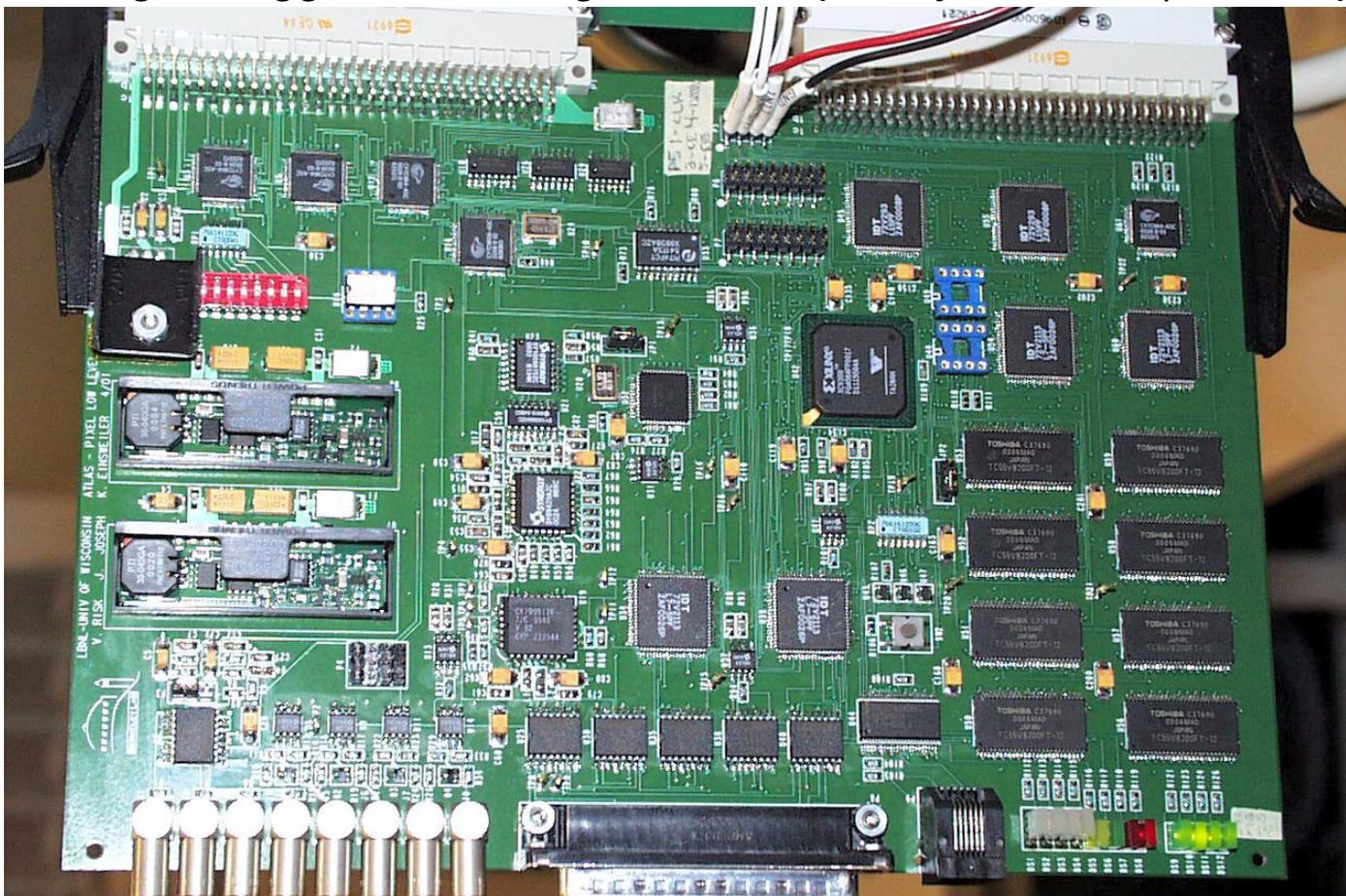
Summarize various configurations needed:

- Design characterization and production Wafer Probing (PLL+PICT+adapter card): In this case, a later generation of probe card could include active components directly. Start with simple adapter card for testing.
- Bare module production probing (PLL+PCC/PICT+special probe card): If we want to interface to the “double probe” concept under development by Milano, need to define mechanism to select which of two chips is sent back to PLL.
- Single chip and module characterization (PLL+PCC+existing support card): Modified 50-pin connector pin assignments are backwards compatible, so this is the present method of operating in the lab and testbeam. Will need to make a new support card for FE-I for new pinout and reduced operation voltage.
- Production module testing (PLL+PCC/PICT+mini-support card): Have prototyped a new “mini-support” card for this interface for Flex2. This will evolve as Flex3, module carrier concept, and production tooling develops.
- Production burn-in testing (PLL + special PCC): The needs for this are not yet well-defined, but system would be based on a PCC core, and including the monitoring capability of PICT. Would nominally support 16 modules, connected using test connector or pigtail connector. Full I/O from only one module would be multiplexed back to PLL for evaluation, but XCK and possibly LV1/VCal would be supplied to all modules.

Status of Components

PLL Status:

- Have components for 10 boards. Fabricated 3 PC boards, and loaded two. First board being debugged, but was given lower priority than 0.25μ testchip work.



- VHDL Upgrades completed to operate board with FE-B/FE-D. Will need further upgrades to support FE-I and new MCC-I.

- So far, no major errors encountered. Clock synthesis is working up to 100MHz, and can access basic VME registers. Very little time spent because of urgency of understanding the TSMC Analog Test Chip.
- Plan to work on debugging after we complete the IBM irradiation (June 21).
- If there are no major revisions to the board, we will begin to fabricate the full 10 board set of the initial production. Plan for eventual production of 20 cards.

Compatibility with existing hardware:

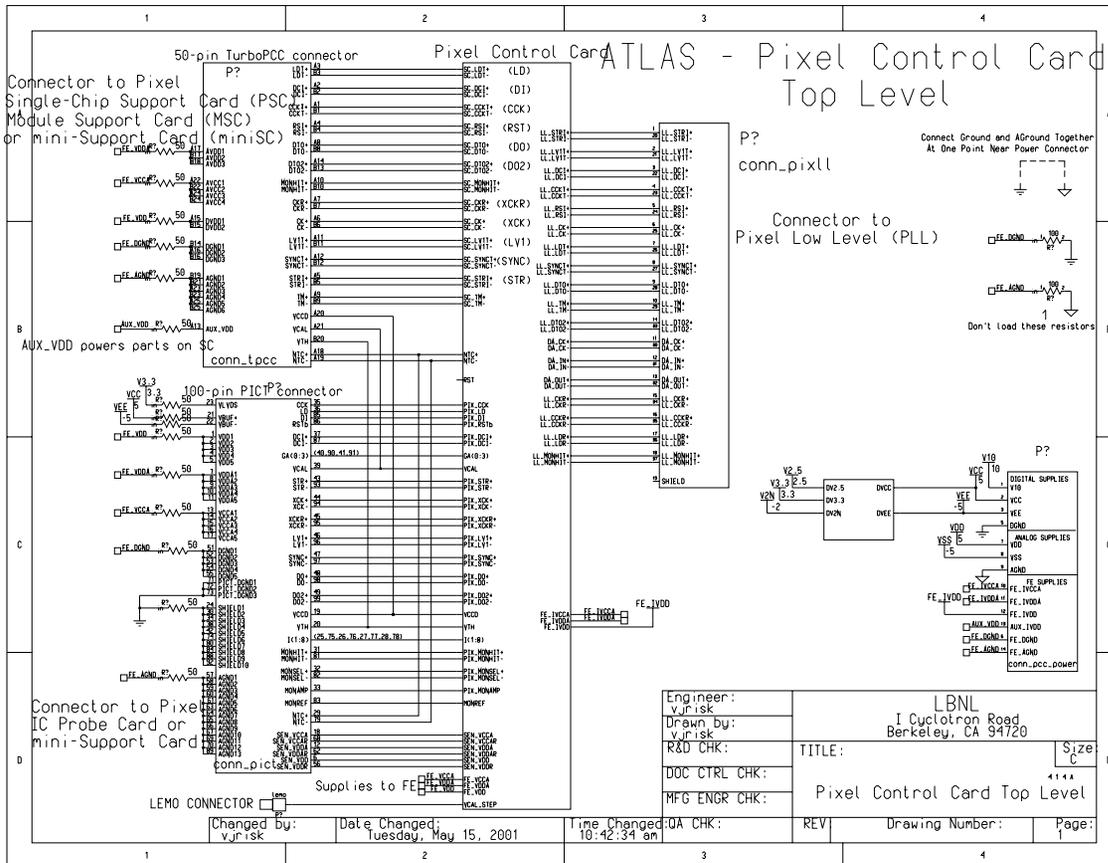
- Supports additional DTO2 line by removing PCC_RESET. Otherwise, interface to PCC is identical. Therefore, it will work with the old PCC if we retain the old firmware for slow control communications with the PCC.
- However, we intend to use an improved protocol for communication with the new PCC and PICT, because there are many more, and more complex, commands for the PICT. The old protocol (adapted to the 68K controller chip on the Siegen PCC) is VERY slow (about 100 Kbits/sec).
- We will have to see how long we can maintain PLL firmware and PixelDAQ software compatibility with the old PCC's. Hope this is not needed for long...

Reminder of advantages of new PLL:

- Full module scan possible in on-board SRAM.
- Variable clock speed testing from 20MHz to 100MHz is possible.

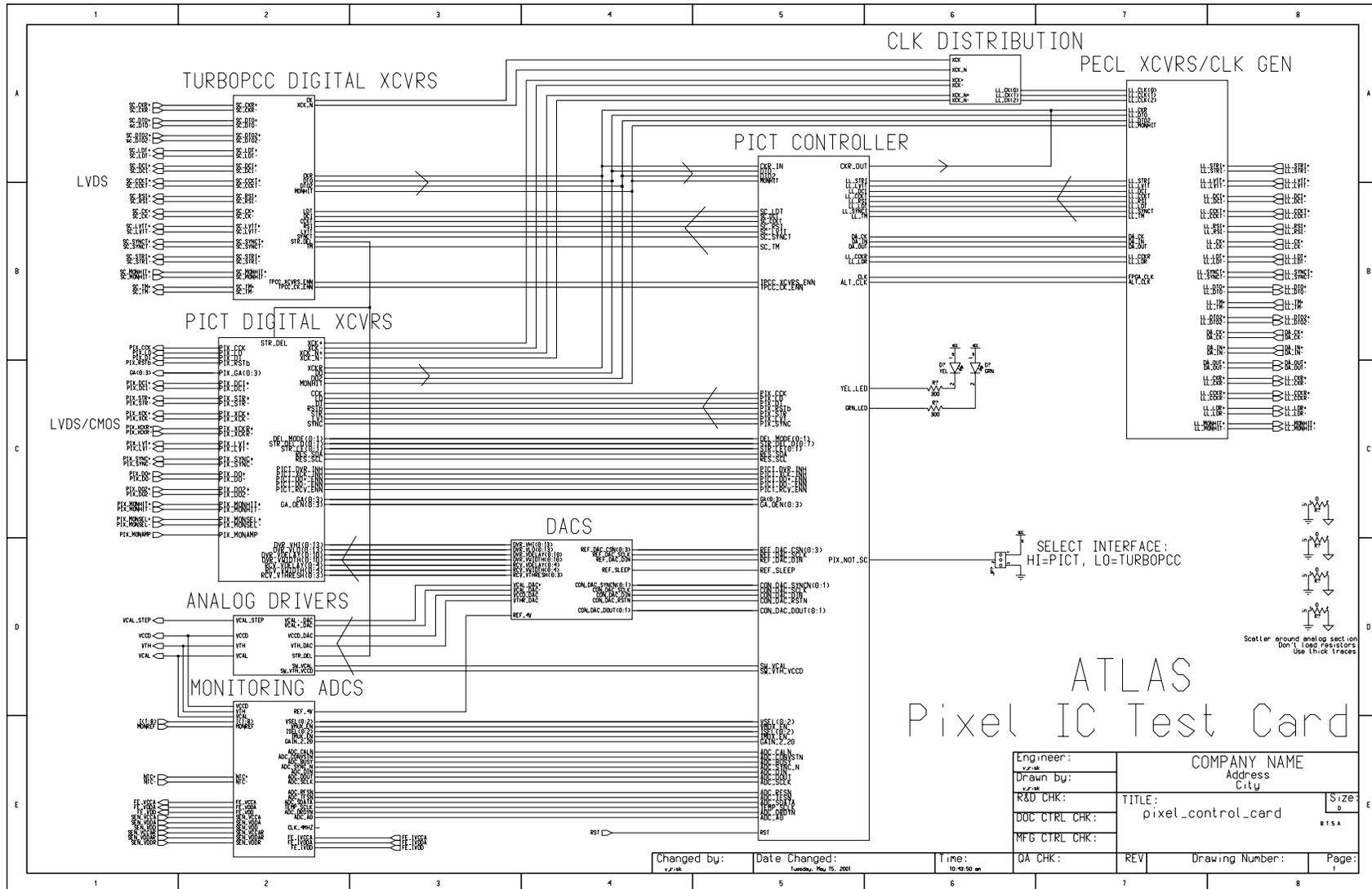
PICT Status:

- Component orders for 5 boards completed.
- Schematics completed, but minor modifications required for evolving FE-I design. Plan to drop backwards compatibility with FE-D testing (VCCD/VTH generation, non-multiplexed DAC outputs, and MonSel), but keep compatibility with FE-B/FE-D operation (second analog supply).
- Board layout has started, and would expect to fabricate the board in early August.



Top level schematic showing core plus three major connectors (PLL, PCC-like, and PICT).

•Next level of PICT schematic:



- After PICT is finished, will extract subset of schematic and make new PCC. The new PCC should support most lab/testbeam module testing. Included features are Str delay, VCal chopper, temperature measurement, but no I/V monitoring.

New Support Cards for FE-I

- With the change in operating voltages and pinout, all presently existing support cards must be updated.
- Present plan is to use PCC 50-pin connector interface for everything except probe cards. However, cards could be built with PICT 100-pin connector also.
- The PICT interface includes remote voltage sensing, extra supply pins to power active buffering on support card, and direct access to all pins on the FE chip (including GA and Mon pins). Intended for high speed (100MHz) chip testing.

Probe Cards:

- For the wafer probe card, initially plan a simple adapter card to carry the needed circuitry for the interface to the PICT, and then would use a standard rectangular probe card with card-edge interface.
- Bonn plans to implement a higher performance custom wafer probe card for high-quality testing. This may not be needed right away, but should be developed soon, to allow complete characterization of the 0.25 μ chips.
- For bare module probing, use of new PCC should be adequate for testing, but would like to understand the interface. For a double probe card like that developed by Milano, which sequentially probes two chips, one on each side of the module, need a mechanism to select which chip is probed. There are presently no extra lines from the PCC for this purpose...

Single Chip Support:

- There is a minimum amount of glue logic needed. This consists of four LVDS->CMOS converters for DI, LD, CCK, and RSTb, plus 3 LVDS->LVDS buffers for DO, MonHit, and XCKR.
- Unfortunately, there are no commercial LVDS parts rated for operation at 2V digital supply voltage. Can use a separate 3.3V supply and commercial parts (LV048 followed by LVC4245 level-shifter for LVDS->CMOS, and LV048 followed by LV047 for LVDS->LVDS). This requires PCC to provide 3.3V as AUX_VDD, so it is not compatible with old PCC's.
- We can define packaging for our LVDS Buffer chip and use it for rad-hard cases, or just use it for all cards (advantage: same drivers/receivers as MCC-I).
- Assuming that the buffer chip works properly, have a slight preference for this solution (simpler...)

Module Support:

- Assume that there will be a new generation of “mini-support” cards that will use the PCC 50-pin interface. However, all details will depend on the module carrier developed for production assembly and testing. Possible that these carriers could interface directly to the PCC, as very little circuitry is needed.

Plans for FE-I Testing

Wafer Testing:

- This will be shared between LBL and Bonn, since it requires 200mm probe station capability. It has the highest priority in the preparations.
- With 12 wafer order, there will be enough wafers so that MCC could have one for commercial IC tester evaluation of MCC-I. A second wafer would most likely be rapidly diced in order to harvest DORIC, VDC, and LVDS Buffer chips.
- Probe card schematic is simple, and could be implemented as a simple adapter card that plugs onto standard card-edge interface, or as a custom card. This needs to be agreed with Bonn.
- First PICT systems will be distributed to Bonn and LBL for wafer testing by September at the latest.

Testing of single chips:

- For single chips, plan to develop a new single chip support card.
- Testing of single chips would be compatible with the existing PCC. We will produce a new PCC, better matched to present testing needs, but this has lower priority than completing the PICT (but schematic is almost rigorously a subset).
- For single chip testing, could probably also use old PLL. However, PixelDAQ will evolve rapidly to support new MCC-I and PICT, so this is not a long term solution.

Testing of Modules:

- This will require significant new coding in PLL for the new MCC-I. This will only be done for the new PLL.
- The firmware in the old PLL will not be upgraded in any significant way.
- Testing of present FE-B and FE-D modules should be done with the current generation of PixelDAQ/PLL/PCC...

Testing of multiple modules:

- Presently, Milano and LBL (and Bonn ?) have managed to do this in a brute-force way using multiple PLL/PCC with simple modifications to the PixelDAQ software to allow addressing one PLL and initializing one module at a time.
- It would be easy to provide simple multi-module support in the new PCC, by providing, for example, 4 output 50-pin connectors and multiplexing support. Control would involve analog MUX for NTC connections, individual enables for XCK, and separately for other output signals, and digital MUX for return signals. Are all 4 module power supplies hardwired to common inputs, or are there 4 sets of supply inputs ? Major issue would be PixelDAQ support for configuration data.
- Longer term solution is to use ROD prototypes. This involves considerable overhead (9U crate plus ROD and TIM), so only a few system-test setups could be built. We could implement a simple PCC-like Back-of-Crate card to provide an initial copper link to modules. Longer term, we clearly need to evolve to use PP0-like interface, with opto-cards and a real Back-of-Crate card for the ROD.