

Overview of 0.25 μ Design Effort

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Goals of submission

- Front-end chip FE-I: feature list and pinout
- MCC
- Opto-chips
- Test chips: Analog Test Chip, LVDS Buffer Chip, PM bar

Common engineering run

- Processing decisions

Present Status

- ATLAS design review
- Schedule

Changes implemented in 0.25 μ FE chip

Analog Front-end:

- Implement improved threshold control using 8-bit current DACs instead of previous 5-bit voltage DACs.
- Implement two stage design to allow better optimization for timewalk performance.
- Extended present 3-bit TDAC (threshold trim DAC in pixel) to 5 bits, and added a 5-bit FDAC for feedback current trim in pixel. This should allow improved threshold control and trimming of TOT non-uniformities.
- Dropped second analog power supply to simplify services.
- Implemented improved charge injection design using local chopper and dual injection capacitors. Previous steered current design had problems with risetime.

Digital Readout:

- Implement all static design for both storage cells and logic blocks.
- Implement more synchronous and “top-down” design, and use standard cells and automatic place and route for logic blocks wherever possible.
- Increase timestamps (TSI) from 7 to 8 bits, increasing maximum latency to 6.4 μ s
- Implement column-based TOT calculation to allow digital timewalk corrections.
- Design for operation at 2V, therefore simulate 1.8V and 2.5V as worst and best cases. Compromise between lifetime/safety margin and performance.

Feature List for FE-I

Design is largely a conversion of FE-D and FE-H designs.

Analog Front-end:

- The FE uses a DC-feedback preamp design which provides excellent leakage current tolerance without changing the shaping, close to constant-current return to baseline for TOT, and very stable operation with different shaping times.
- It is followed by a differential second amplifier stage, DC-coupled to the preamp. The reference level (VReplica) is generated in the feedback block, and should match the DC offset of the preamp with no input. The threshold control is applied using two currents to modify the offsets on the inputs to the second amplifier stage, allowing a large range for threshold control.
- The two-stage amplifier is followed by a differential discriminator which provides the digital output sent to the control logic.
- The control logic provides a 5-bit threshold trim capability in each pixel, plus a 5-bit feedback current trim capability for tuning the TOT response. There are four control bits, including Kill (shut down preamp), Mask (block entry of hit into readout logic), HitBus (enable output to global FastOR) and Select (enable injection of charge for testing). The HitBus bit also controls the summing of a current proportional to the feedback plus leakage current in the preamp, allowing monitoring of the feedback current, and of the leakage current from the sensor.

- A global FastOR net is created using all pixels enabled for this type of readout, and provides a self-trigger and diagnostic capability.
- All critical bias currents and voltages on the chip are controlled by internal DACs. There are 11 8-bit DACs for the analog front-end, and an additional DAC for the charge injection. The current DACs are referenced to an internal CMOS current reference.

Digital Readout:

- It uses an 8-bit Grey-coded 40 MHz differential “timestamp” bus as a timing reference throughout the active matrix. All pixels measure their leading and trailing edge timing by asynchronously latching this reference in RAMs.
- Hits (address plus LE/TE timing) are transferred from the pixels as soon as the trailing edge occurs, using a shared bus structure in the pixel column pair. This bus operates at transfer rates up to 20 MHz in order to meet our requirements. Differential signal transmission and sense amplifiers are used to achieve this.
- Significant buffering is provided in the end of column region for hit storage during the L1 latency (up to 6.4 μ s in this chip). Forty buffers are available for each column pair. This number could be increased to 64 if simulations suggest it is necessary for the B-layer. The coincidence with the L1 trigger is performed in these buffers. Hits from rejected crossings are immediately cleared.
- A readout sequencer stores information on up to 16 events pending readout. The only error condition is again EOC buffer overflow.

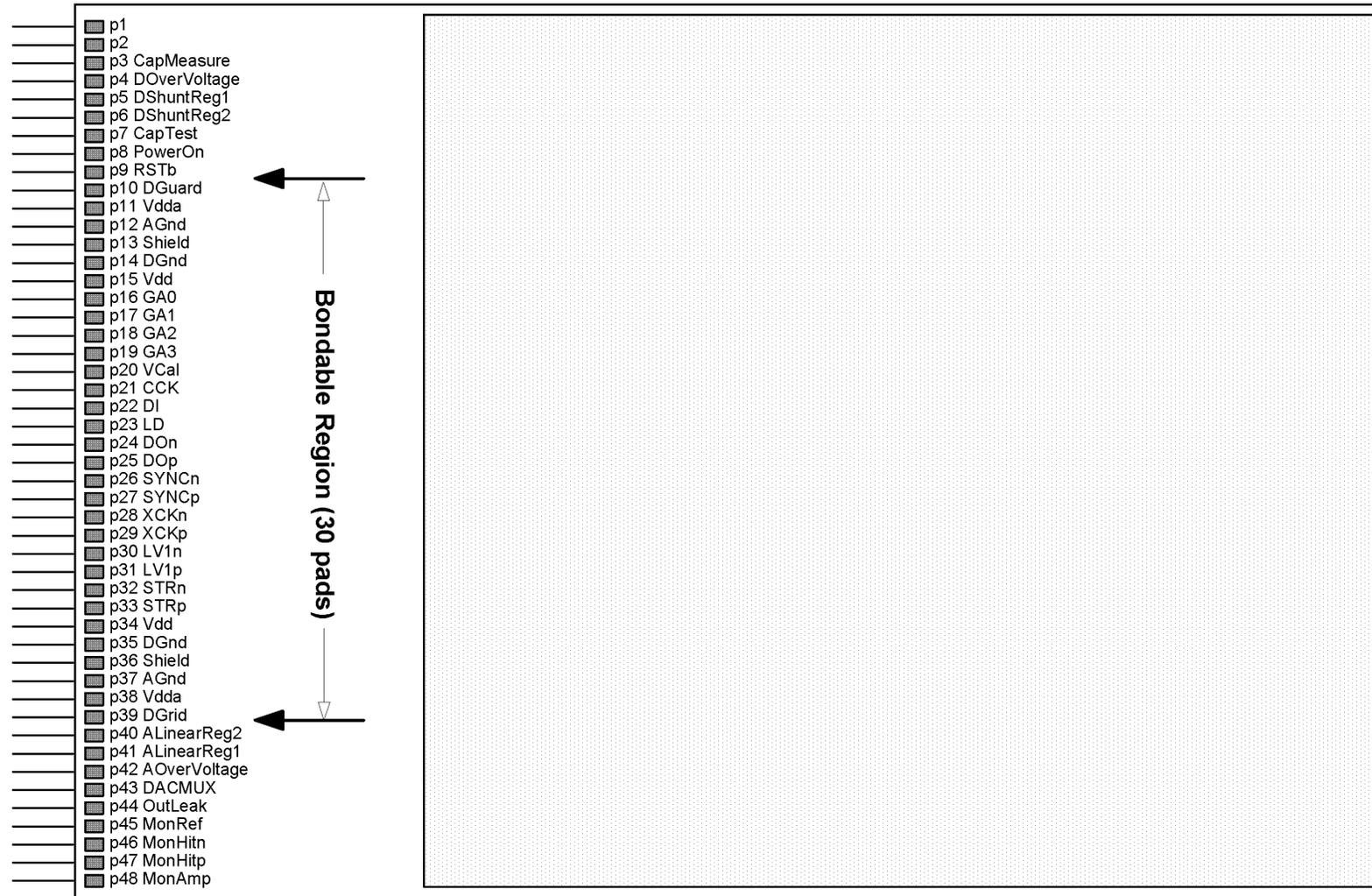
- There is now a TOT processor at the bottom of column. This processor converts the LE and TE information to binary, and subtracts to compute TOT. It offers the option of applying a digital threshold to the TOT, or of duplicating hits below another threshold (one hit is given timing LE, and one is given LE-1). Reading one crossing will then also transfer timewalk-corrected hits with low charge.
- A multiplexor at the bottom of column allows transferring either the LE, the TE, or the TOT data into the TOT data field of the EOC buffer. This allows simpler more complete testing of all storage bits in the pixels

Control Logic:

- There is a 20-bit Command Register. Individual bits in this register implement specific commands (e.g. ClockGlobal, WriteGlobal, ReadGlobal). The Command Register will use the same shift register and SEU-tolerant latch as the Global Register to make sure that no command bits can flip during operation.
- A Global Register, consisting of about 166 bits, controls Latency, DAC values, enabled columns, clock speeds, and many other parameters. This register is implemented as a shift register and shadow latch with readback capability. The shadow latch is SEU-tolerant since it contains critical configuration information.
- A Pixel Register which snakes through the active array provides access to the 14 control bits in the pixel (Select, Mask, HitBus, Kill, FDAC<0:4>, TDAC<0:4>). Readback capability is supported by transferring FF information back into the long shift register for readout. The 14 latches in each pixel are SEU-tolerant.

FE-I Pinout and Geometry

Sketch of pin assignments and overall geometry of die:



- Note new $100\mu \times 200\mu$ pad geometry to reduce effects of probing on bonding, and to allow multiple bonding attempts before pad damage becomes too severe.

Pins inside the bondable region:

- Pins in the bonding region are essentially the same as in earlier chips. We have replaced the second analog supply with Shield pins, which may be used for a second clean internal analog supply, or for a real shield plate over the digital section. This is still being discussed.

New features and pins outside the bonding region:

- CapMeasure pin is attached to new capacitor measurement circuitry, which uses a charge pump circuit to measure accurate values for the critical capacitors used in the front-end ($C(\text{feedback})$, $C(\text{inj-low})$, $C(\text{inj-high})$) by measuring a single DC current. This circuit has been used in the DMILL CapTest chip, and can provide accurate measurements of capacitor arrays at the fF level.
- Power Management features (overvoltage clamps and regulators) will be discussed in more detail by P. Fischer. The intention is to place them inside the die (we should have space), and connect them into the power net by stitch-bonding. There is little risk if the bonds are not connected, and the performance of modules may be compared with and without these circuits, without the need to design a second Flex which would need 16 small die sites to mount this circuitry.
- CapTest pin is to control new “smart” decoupling capacitors which we plan to use internally in the FE chip. This test pin would normally be pulsed in order to cause the capacitors to check for an internal-short condition. Shorted capacitors would be automatically disconnected from the power supply.

- PowerOn pin provides a power-on reset, which can be bonded across to the RSTb pin for testing. The Global Register, when reset, suppresses the basic clocks for the digital readout. The major power consumption in the digital logic is in the TSI distribution, CEU operation, and EOC buffer state machines. When the Global Register is reset, the digital part of the chip will operate in a low-power condition (less than 10% of nominal power), but all basic registers will still operate. The analog supply could be turned on, but since the DAC values would all be set to 0, the current consumption would also be very low. This low-power power-on state would permit simple continuity tests of the module (and the rest of the cable plant) with a power consumption so low that no cooling would be required.
- DACMUX provides multiplexed access to all of the internal DACs for characterization during testing.
- OutLeak provides access to a current summing tree (controlled in the same way as the HitBus) that allows a direct measurement of the preamp feedback current and the sensor leakage current: $I(\text{OutLeak}) = 3 \cdot I_f + I_{\text{Leak}}$. This has already proven very useful in chip characterization. A simple internal ADC may also be provided.
- MonAmp would be upgraded to allow us to see the preamp waveform, the two sides of the second amplifier, and the chopper input. There is also a 100Ω buffer amplifier, which could drive a daisy-chained bus of test amplifiers, provided only one was enabled at any time. This circuitry has proven vital in Analog Test chip.
- Pads include improved ESD clamping, with IBM transient clamp on power supplies, attempting to provide much more robust protection against supply spikes.

Reticle for FE-I Run

Similar to FE-D2 run, all designs should use same pads

- **Two FE-I chips:** the present plan is that these would be identical.
- **MCC-I chip:** this should be the complete new MCC with U-pinout to satisfy module constraints. For the purpose of making a reticle, it would be simpler to dice if the long dimension was no more than the width of an FE chip (7.2mm)...
- **DORIC-I and VDC-I chips:** they would be improved versions of the designs submitted in the Feb MPW run.
- **Analog Test Chip:** this should be very similar to the test chip just fabricated, but would contain the final design and layout of all analog blocks, and perhaps 64 channels instead of 20. We should attempt to keep a similar pinout.
- **LVDS Buffer Chip:** this is a convenient way to include the interface between a single chip and our test system into a rad-hard chip. Given the absence of commercial LVDS drivers operating at less than 3.3V, this is even more useful. It contains 4 LVDS->CMOS converters, 3 LVDS->LVDS converters (3.5mA outputs) and possibly a buffer for the MonAmp pin (depending on how this is handled in the FE-I chip).
- **PM bar:** may be useful for checking details of device characteristics, although the very good parameter stability seen so far suggests it may no longer be needed. It is more likely that we will just include the small bar designed by the CERN group, and used by them to track the parameter stability on all multi-project runs.

Common Engineering Run

Processing options defined:

- Five metal layers, with LM top metal (1.0μ , $30\text{m}\Omega/\text{sq}$) and TV passivation (1.0μ , oxide/nitride).
- No backside grinding, so wafers will be left at their native thickness of about 700μ .
- Additional masks for special features: OP Resistor (silicide block for poly resistors, ESD output drivers), MiM Capacitor (high value linear capacitor made with additional Q2 layer).
- Request 12 wafers (nominal maximum for an engineering run is 6) under informal agreement with IBM. This will provide us with enough wafers for multiple bumping vendors, MCC commercial IC tester screening, etc. Second set of six wafers would be delivered several weeks after the first.
- Possibility of “striping” is interesting. Vendor uses standard processing in central 80% of wafer, and does ± 1.5 and ± 3 sigma variations of a single parameter on the rest. This option needs further discussion to understand possibilities.
- Approximate total cost 190K\$. Purchase Order will be issued by CERN from their standard foundry account, and TID's will be used to collect money from specific institutional accounts in ATLAS pixels. This allows all preparation to proceed without signatures.

Present Status

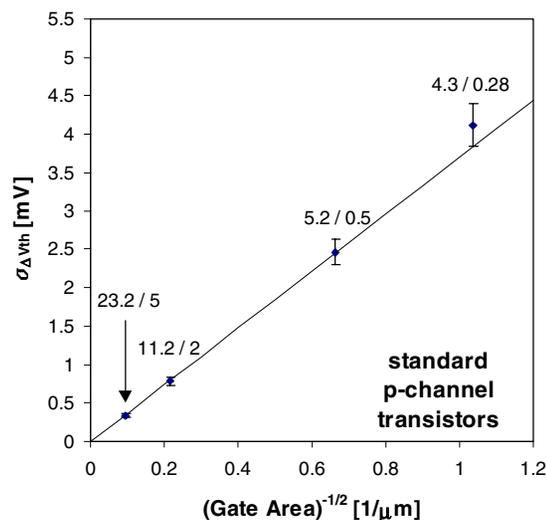
ATLAS Review of FE-I

- Review took place at CERN June 6-7. Reviewers were Anghinolfi, Campbell, and French (Campbell dropped out due to prior commitments).
- It is clear that this review, scheduled back in Feb/Mar, was too early for us. However, we decided to go ahead, and we will have a brief follow-up review prior to submission.
- Presented designs and all measurements to date, plus plan for finishing the chip. This was very useful, and pretty well filled the two days. We learned a number of things.
- We need very much to write a complete specification for the FE-I, against which its performance can be judged.
- Our major concern at the moment is to understand the very large threshold dispersion observed in the TSMC Analog Test Chip. We will receive the IBM version of the chip any day now, and plan to test it immediately (we brought our test system to CERN). We will irradiate the IBM chip on June 21 at LBL, and possibly carry out further irradiations in July at the PS.
- We should receive a written report from the reviewers shortly.

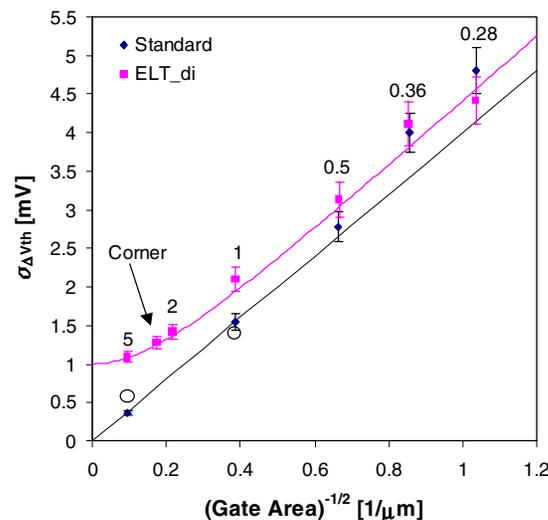
Threshold dispersion and matching:

- Have carried out first studies of impact of VT matching on present front-end, as a possible explanation of the large threshold dispersion.
- First simulations just used a voltage source to shift the VT of each critical transistor in the preamplifier and second stage by a known amount, and then scaled to the expected VT mis-match for that device. There are 10 sensitive FETs in the preamplifier and 4 in the second amplifier. This gave a crude estimate of 1500e threshold dispersion, by looking at DC baseline shifts at the discriminator input.
- A more sophisticated analysis has been done by Peter Denes by actually injecting charge and scanning to find the discriminator threshold for each simulation. This gives a set of curves which show similar features to those seen in the data.
- A more extended Monte Carlo run was then performed, where each device had its VT modified using a Gaussian with sigma taken from the thesis of G. Anelli:

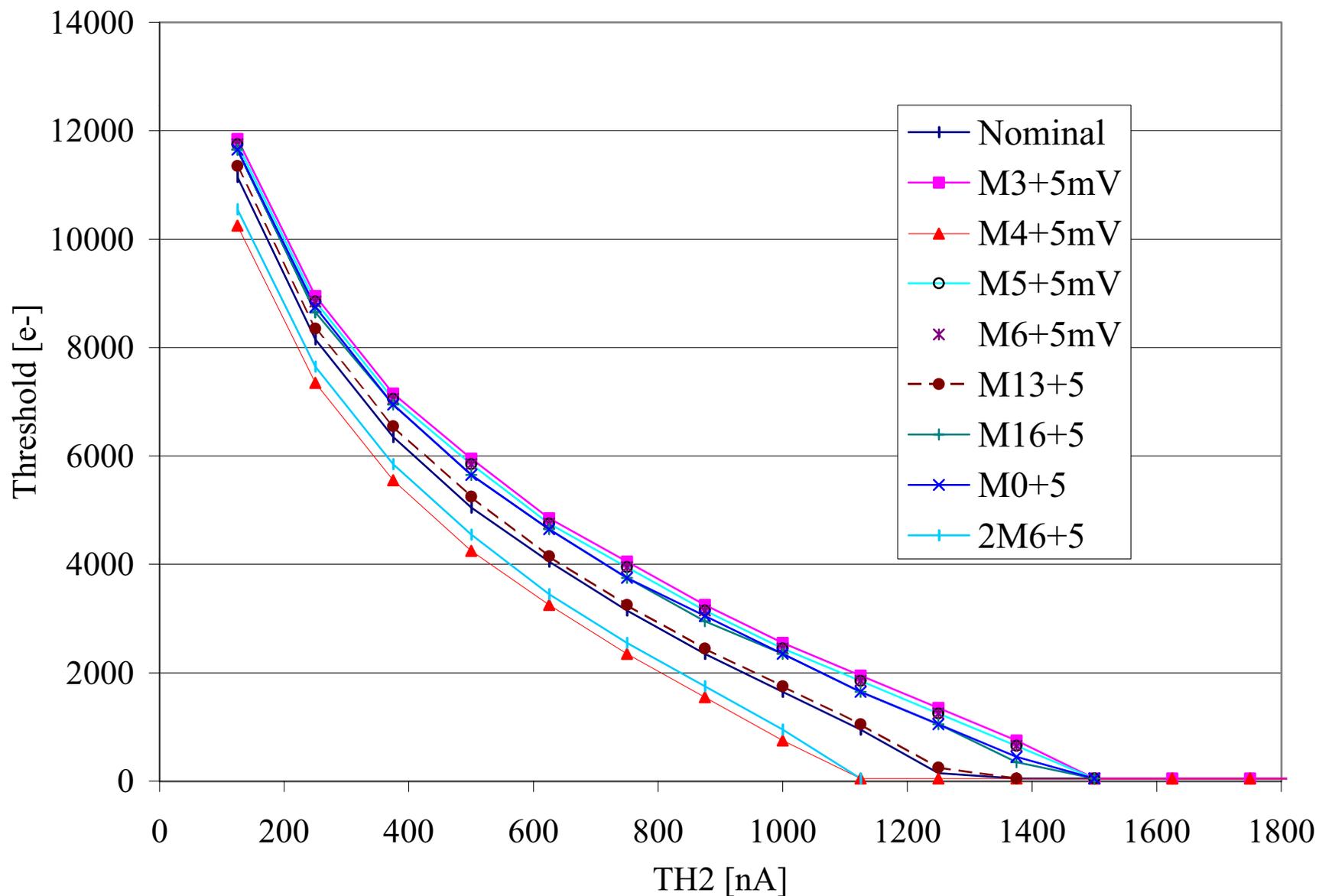
Standard PMOS VT matching versus device size



Enclosed NMOS VT matching versus device size

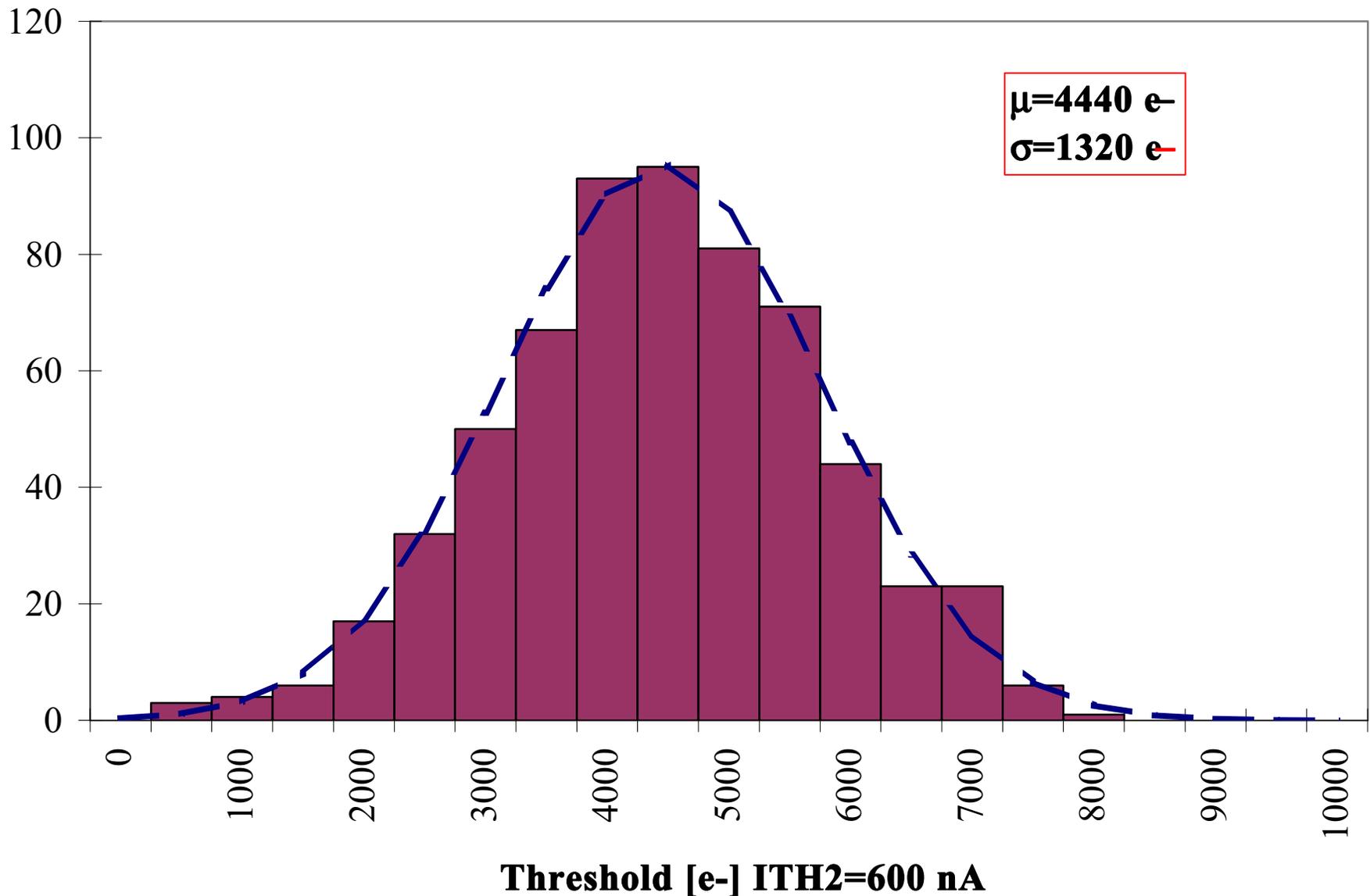


• Threshold simulation, moving each device by $\Delta VT = +5mV$:



• Need to combine contributions in quadrature, but behavior looks like measurement.

•Results of Monte Carlo simulation, sliced at one value of ITH2 (threshold):



•Have not included sources of chip-chip variations, but matching contributions can clearly explain a large fraction of the excessive threshold dispersion observed.

Status of FE-I Integration

- Layout/integration of front-end blocks and analog bottom-of-column almost complete. This includes 12 DACs, bias mirrors, and current reference. Integration of buffering and logic for the control section started but not yet complete. The test pixel support (MUX and buffer) not yet integrated, but blocks exist in the test chip.
- Now plan to also integrate significant decoupling (several pF per pixel on both analog and digital supplies) into each column pair, and will likely modify the present shielding scheme somewhat.
- Layout of digital readout is complete, including CEU, sense amplifiers, and TOT processor. Have performed TimeMill simulation of this circuitry for a complete column pair with full parasitic extraction, and the performance looks good.
- Layout of EOC buffers (presently 40 per column pair) and MUX sparse scan of column pairs is complete. Could add more buffers for a total of 64 if needed.
- Power budget for digital supply looks OK (10mA for column readout, 7mA for EOC buffers when idle). PowerMill being used to study dynamic consumption.
- Performing final updates on Verilog descriptions of blocks at the bottom of the chip (Readout Controller, Clock Generator, Command Decoder, Global Register, Grey Generator, Reset Generator, Output MUXes). These blocks will then be synthesized and placed and routed.
- Additional special blocks (smart decoupling, overvoltage protection, regulators, and capacitor measurement) are in progress at Bonn.

Estimated submission date:

Issues raised so far by the test chips:

- Large threshold dispersion observed. Calibration scale not yet definitive, but range of dispersion is sigma of 2500e. Studies suggest matching of small current mirrors is a major factor - there may be others. This needs to be reduced to about 1000e before submission (remember have 5-bit threshold trim DAC). This will require major re-layout of front-end to increase many device sizes by factor of 4...
- New chopper design shows offset when compared to external injection, and preamp pulse from test pixel shows undershoot. Better understanding needed.
- New LVDS driver shows poor waveform shape and transit time. This needs to be better understood, and improved.

Remaining tasks:

- Continue characterization of test chips to learn as much as possible about the present designs, including irradiations.
- Finish the overall layout by integrating all present blocks together. Estimate this will take about 4 more weeks. Additional work on front-end almost certainly needed.
- Top level simulations using Verilog for functional verification and TimeMill for timing verification have started, but estimate another 4-6 weeks of work here.
- Formal verification (LVS and DRC) will also take several weeks. Estimate that with significant effort, could submit roughly 2 months from today.