Pixel Electronics Status

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Status of FE-D submission

Status of Honeywell SOI

Status of DMILL MCC conversion

Status of Opto-electronics (DORIC+VDC)

Status of Power Supplies

L1 Latency Issue

Status of FE-D Submission

- We had a successful 2 day design meeting in Bonn last week, with all of the FE-D designers in the same place.
- The complete layout and corresponding simulations are advancing well. All major circuit blocks have been layed out. Verilog and SPICE simulations for these blocks are still in their early stages.
- The integration of the blocks into the overall floorplan is proceeding. The first stumbling block has been to fit all of the circuitry in the pixel within the 400μ allowed size. A first attempt last week gave a pixel pair dimension of 805μ. About 6-7μ has been found in the digital readout section, but modified layout is not yet available. Hence, we are reasonably confident that the present design will fit in 399μ. Note however that it has proven necessary to give up the bipolar front-end design to achieve this (it is more than 12μ larger in each pixel). Also a desired small increase in feedback capacitance will probably not be possible.
- We willl have our first ATLAS pixel electronics review on Tuesday, Feb 23. We believe we are in good technical shape for this review, although our documentation still leaves something to be desired.
- Our goal is still to submit these designs by about April 1-15. This submission would presently include a digital test chip, and a DMILL MCC prototype, as well as some kind of process monitor structure. We will probably try to rely on the re-submitted MAREBO to provide more detailed analog characterization.

- The submission date is getting close enough that we should begin preparing the procurement, etc. This will be a common procurement with a CERN PO.

Status of Honeywell SOI

- We are still waiting for the TAA (export control) agreements to be in place for Bonn, CPPM, and Genova. The most recent news from Gil suggests that they should be in place in 3-4 weeks.
- We expect the return of our test HSOI run (submitted in Nov. 98) at the end of March. Recall that this includes a transistor and capacitance test structure, an improved FE-B dual-threshold design in a test chip, and a second test chip with several variations on the improved FE-B design.
- Franz will spend two weeks in LBL in April to help test these chips, and we will also carry out irradiation tests. Note that this run was not the “enhanced” SOI process we plan to use (with improved oxide treatment to reduce V_T shifts), but the standard production SOI process.
- Minor improvements have been made in our Cadence technology files, and we are ready to work again on this process as soon as the FE-D chip is safely on its way to fabrication.
- As mentioned in a recent EMail from A. Seiden (UCSC), several US groups have received enough non-ATLAS funding to do a small (5 wafer) engineering run in Honeywell SOI this fiscal year (before 10/99). Although the timing is tight, we encourage creative thinking about how ATLAS might benefit from this run.

Status of DMILL MCC Conversion

- R. Beccherle spent three weeks at LBL in Jan. to lay out a DMILL version of the AMS FIFO used in the existing MCC chip. The new design is about 1.5 times larger than the design used in AMS.
- Roberto has also spent time working with the DMILL standard cell library. He finds that it is almost 100% larger than the equivalent AMS cells. Since much of the space in MCC is used for routing, which does not increase significantly in size between the two processes, one might expect that a DMILL MCC would be roughly 1.5 times larger than the existing die, for the same functionality.
- A test chip, pin-compatible with the existing MCC, but lacking any event building capability, is being prepared. It is expected to be submitted as part of the FE-D engineering run.
- If we really intend to build an MCC with DMILL, we will probably need to work more on the standard cell library layouts, and also reduce the FIFO size by reducing the word count. This might lead to an acceptable size MCC for the outer layers of ATLAS, but would probably fall short of the B-layer needs.
- It seems clear that we need to work on a standard cell library in Honeywell that would be suitable for logic synthesis. The denser layout rules, and possibility of third and fourth metal routing, could lead to an MCC die size which is 50% of the DMILL version for the same schematic.

Status of Opto-electronics

- We had a good meeting in Oxford in Nov. 98 to start off this work.
- The Siegen group has submitted a prototype chip to AMS including bi-phase decoding and a delay-locked loop in Dec 98.
- The OSU group has invested significant effort in converting the existing DORIC design to CMOS. Several minor problems have been found along the way, and a new improved design has emerged, which is more fully differential, has better common-mode rejection, and lower power consumption. Frequent meetings with RAL/Oxford have allowed both SCT and pixels to benefit from this effort.
- The next step is a further meeting in March, including SCT people, to examine the present two pixel designs in more detail. The intention would be after this to agree on a single common design, which would be prepared for submission to DMILL, including full SPICE simulations with process corner analysis. If FE-D is somewhat late, this could be on the same run, otherwise on the May MPW run.
- In the near future, the VCSEL driver chip (VDC) will also be converted to CMOS. This should be a fairly simple exercise.

- This would give the pixel community its own set of radiation hard opto-electronics chips which would be much better matched to our module needs. Further study of the difficulty of integrating these “analog” circuits onto the digital MCC is needed. Feedback from module design studies is needed to assess how important this goal of a combined MCC+opto-electronics really is.

Status of Power Supplies

- We need to acquire prototype power supplies soon in order to evaluate them for use with our modules and a realistic cable system.
- We have seen detailed presentations from CAEN and Wiener. A third company, Bastian has also expressed interest in our multi-channel modules.
- Two options have emerged. The first one includes the 5 LV channels (AVcc, AVdd, DVdd, VPIN, VVCSEL), and the HV channel (VDet) in a single module. The second involves a 5-channel multi-channel LV supply, and a separate HV supply. It would be preferable if these separate supplies would operate in a common crate with common control protocols.
- We need to finalize our power supply specifications, and write them up in a decent document. This includes clear specifications of voltages/currents, isolation, interlock capabilities, sense capabilities, etc. We need to clarify for ourselves the necessity of full multi-channel supplies.
- One reasonable proposal for these prototypes is to wait until we ask for production quantities to do the official market survey and tender. We would then request one LV/HV combined multi-channel module vendor (e.g. CAEN) and one separated LV/HV vendor (e.g. Wiener LV plus ? HV) to provide prototypes this year for evaluation.

L1 Latency Issue

- Present best estimates of the L1 latency needed for the pixel system, including the contingency of 20 crossings presently held by the trigger group, give an estimate of 131 crossings.
- Since the maximum latency supported by the new FE-D chip is 128 (although this can be stretched by several crossings using a wrap-around latency scheme, this is quite ugly), we are very close to being in big trouble.
- Much of the surprise in this estimate comes from the cable lengths in the problem. It seems clear that alternate routing patterns for the fiber optics for the pixel sub-system should be investigated. The worst case route from the detector to USA15 is now taken as 115m. Simultaneously, it is clear that rack assignments and cable routing in USA15 need to be firmed up soon to avoid continuing uncertainty in this area. We need a real local contact for this !
- Some modest improvements in delay might be achievable in the off-detector electronics through careful attention to clock distribution (using multi-phase 40 MHz clocks). This leads to a less robust system, but may be necessary to provide some modest contingency...
- This subject should be watched carefully by us !