Recent FE-B Module Experience at LBL and UOK

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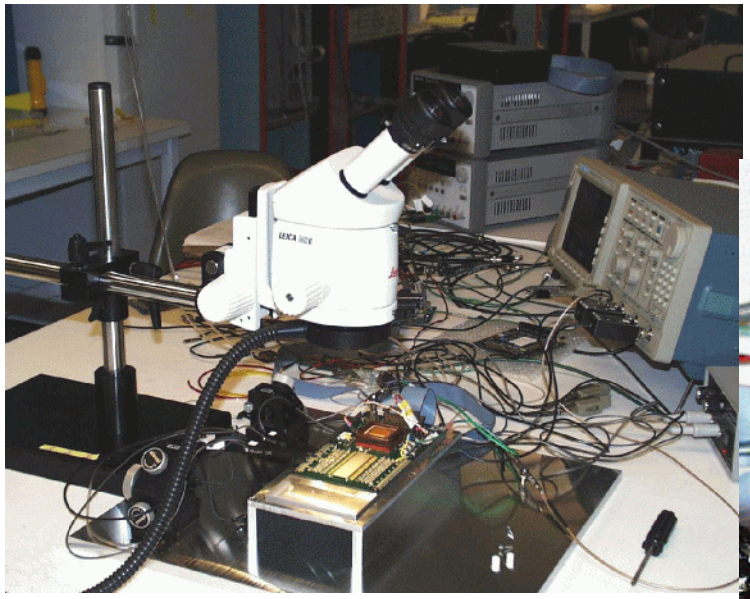
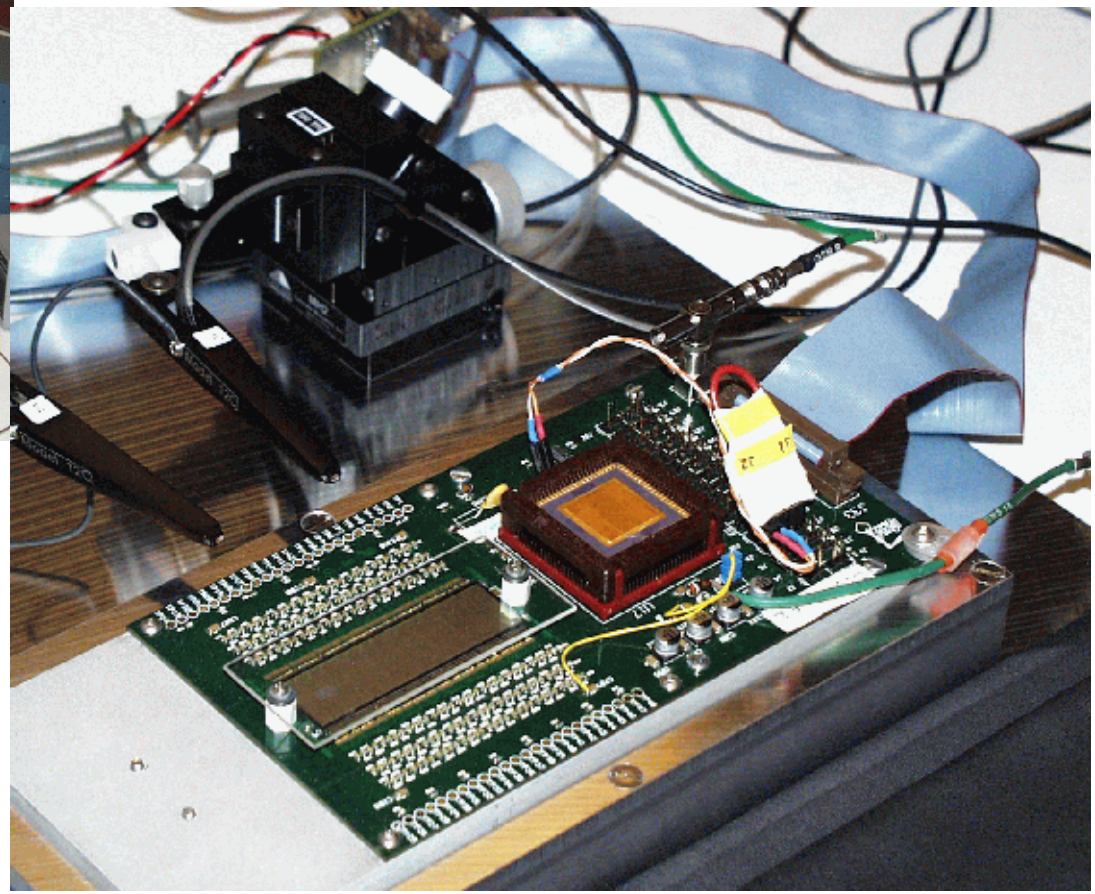
Status and results from first two FE-B "bare" modules

Status and results from first FE-B Flex module

Status of FE-B "bare" modules

- Two modules were flipped by Boeing in June, and assembled using the Genova Module Support Card (12 layer PC card which makes all of the necessary interconnections between 16 FE chips and MCC).





Some features of the first generation Module Support Card:

- Decoupling using 0.01 μF is present for all 9 bias points (8 DACs and MON_REF) on each FE chip.
- Decoupling using 0.01 μF is present for each of the 3 LV supplies on each FE chip.
- Hitbus from each chip is brought to a patch point for jumper-selection of this signal to PLL for self-triggered readout, but it is not buffered to transmit off of the board
- Only internal charge injection is supported (static VCal plus strobe). Modifications needed for external injection (external chopping of VCal).
- Three planes exist in the board: DGnd, AGnd, and AVdd. AVcc and DVdd are distributed by U-shaped bus.
- Detector connections (DGUARD and DGRID) are AC coupled to AGnd. A jumper-selected DC connection is needed. A 1 nF disk capacitor is used for decoupling.

An improved card is in fabrication:

- Three larger decoupling caps exist for each FE chip (allows use of 0.1 μF), other decoupling dropped. Five power planes provide all critical voltages.
- Global HitBus OR for complete module created using external logic.
- All other minor problems fixed (except for possible improvements in bias connect)

Summary of the two “bare” FE-B modules:

- After some wire-bonding problems were fixed, both modules work perfectly from the digital point of view: all 16 chips have every channel working when using digital hit injection.
- When the detector is biased, and the FE-B DACs are set to standard conditions, the power consumption is very stable and reproducible (for 16 FE-B plus MCC):

  DVdd uses 400-450 mA at 3.5V (about 20 mA per FE-B plus 80 mA for MCC) = 1.4W

  AVdd uses 700-750 mA at 3.5V (about 25 mA per FE-B in front-end, rest in Hitbus buffers) = 2.3W

  AVcc uses 250 mA at 1.75V = 0.4W

  A total of about 4.6W maximum, with standard biassing of 40µW/pixel in analog FE
- One module uses a CIS Tile2 detector, and the other is a Seiko Tile1 detector. Both are 1M. The detector currents are quite high at -150V. The Tile1 uses about 45µA and the Tile2 about 200µA.
- The Tile1 module has only a few dead channels, with the exception of one chip (Chip 14) which has about 140 dead channels, mainly in the first two columns. Here, dead means that when doing a threshold scan, these channels produce essentially no hits. X-ray scans indicate these are due to regions with merged bumps.
- The Tile2 module has many dead channels, mainly in the chips on one side (a total of about 800 bad channels are found, most of them in Chips 0 and 4).

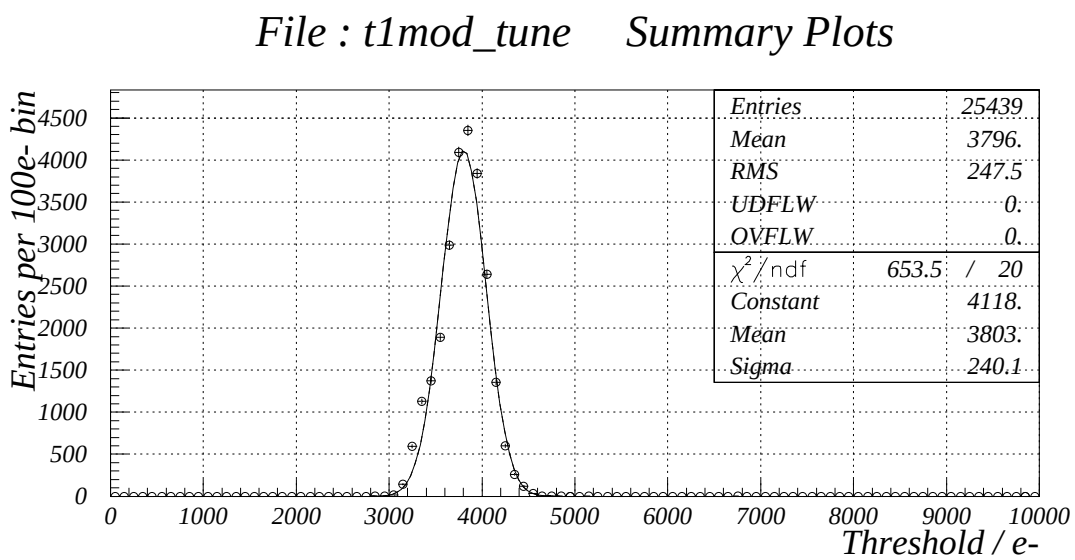
- Initially, behavior was quite poor when all chips were enabled and set to nominal thresholds. Very high noise was observed, with module sometimes entering a high current state in which all channels appeared to be oscillating. This behavior was considerably improved by adding more local LV decoupling (0.1 µF). This state has not been observed since on either module.
- Large number of dead channels was traced to poor bump-bonding (see talk of Gil). These bad channels have a significant influence on the performance of the chips that they occur on.
- These modules were constructed using thermal grease (Dow340) between the FE chips and the Aluminum support plate, with UV-cure epoxy applied to the four corners to hold the module in place. This is different from the single-chip assemblies, for which a silver-loaded epoxy was always used for attachment to a conductive AGnd plate on the PC card.

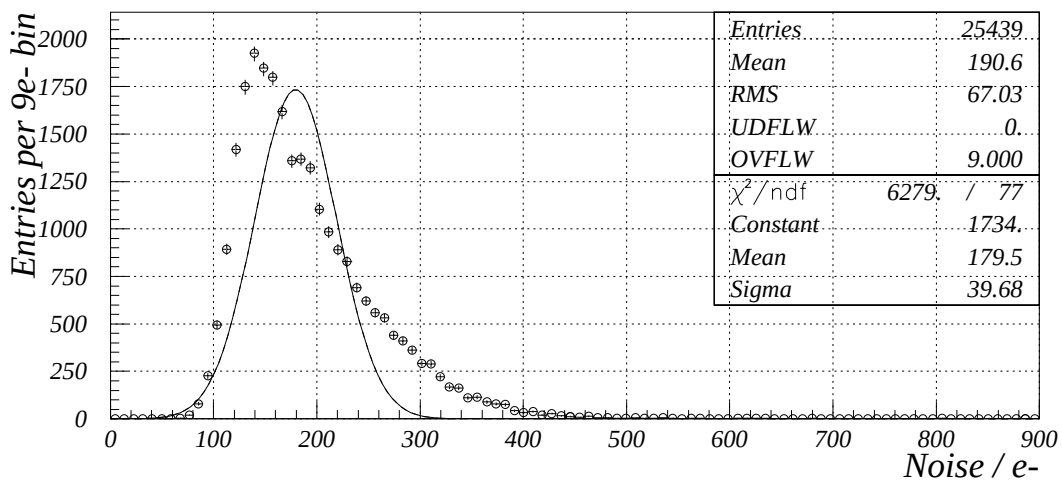
Modifications made to the Tile1 and Tile 2 module cards:

- Added piggy-back 0.1 µF capacitors by each chip in parallel with existing 0.01 µF capacitors.
- Removed wire-bonds from 9 bias nodes on each chip (8 current DACs plus MON_REF).
- Improved AGnd to DGnd connection near chips by soldering a wire across the ground side of the LV decoupling capacitors.
- Improved HV decoupling by using 47 nF surface mount capacitor.
- This essentially eliminated the instability problem. It was possible to operate the modules consistently with all chips tuned (TDACs set for minimal dispersion) and a threshold of about 3.5Ke. This was previously impossible.

Tile1 Module Results:

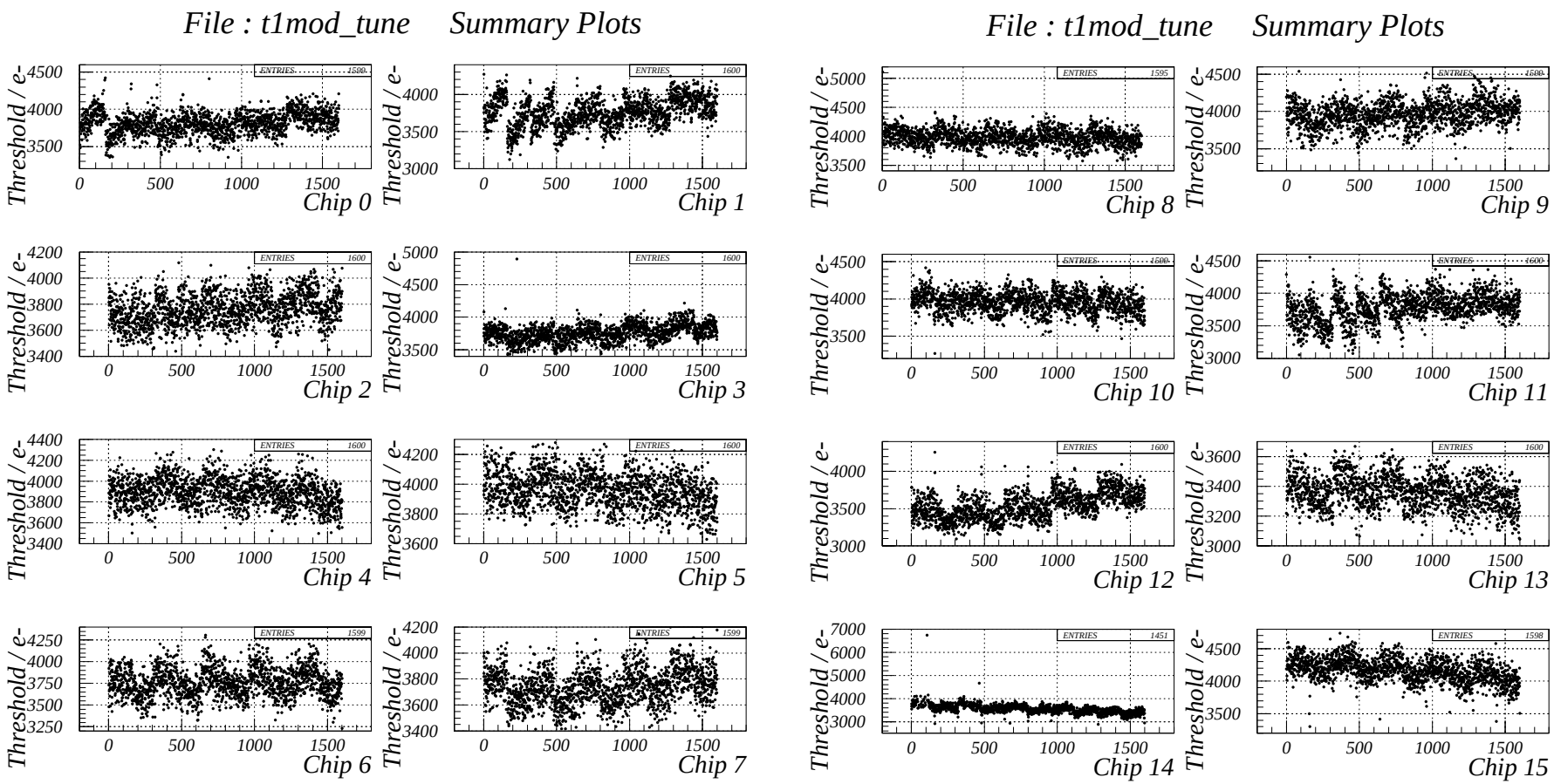
- Show summary of performance with all chips tuned, but only a single chip injected at a given time:





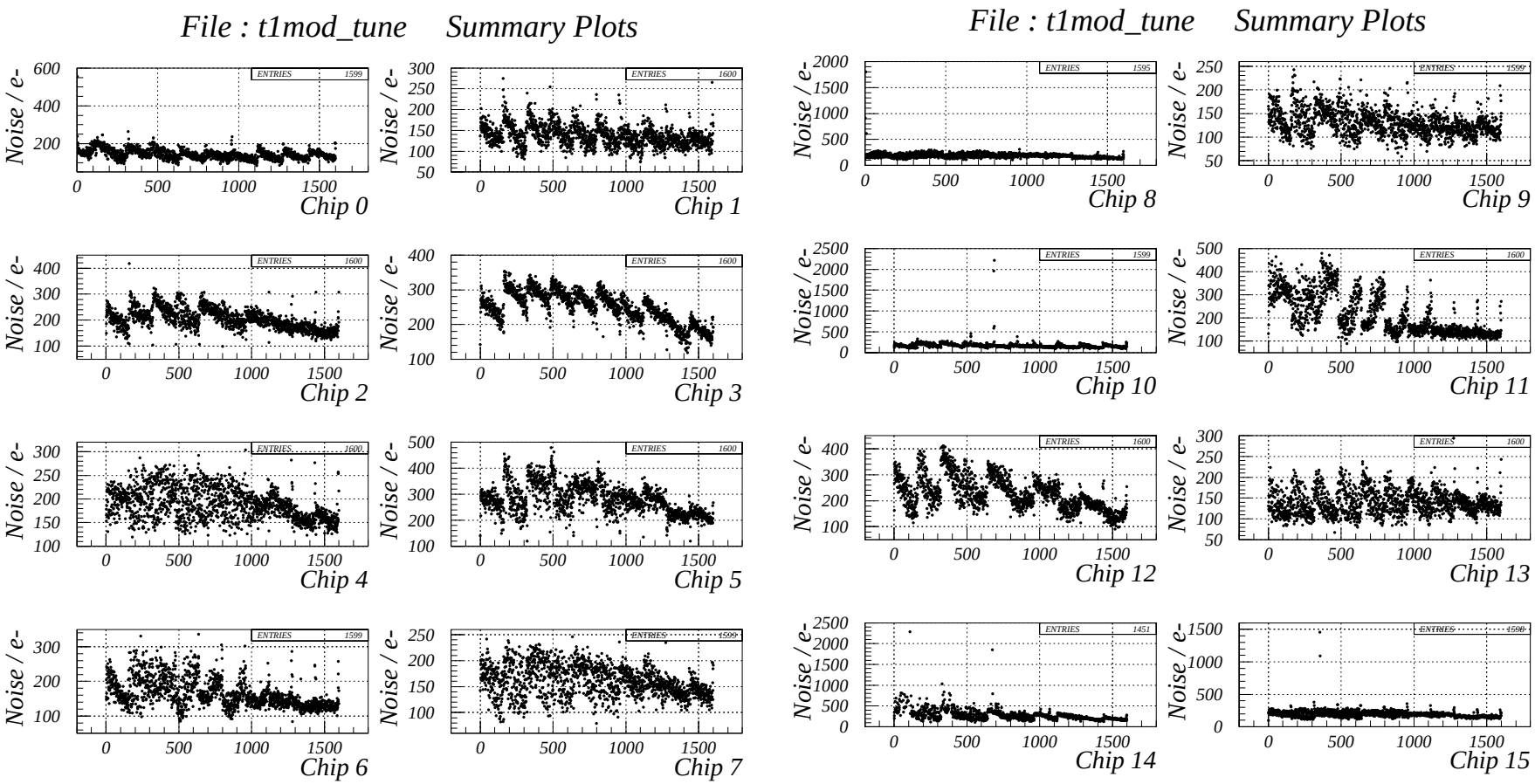
- Overall threshold dispersion, without tuning mean threshold of 16 FE chips, is 240e.
- Mean noise is about 200e, but some chips have noise extending up to about 400e.
- There are 25439 channels in this plot of the 25600 channels that should work in an FE-B module.

Behavior of threshold for the individual chips:



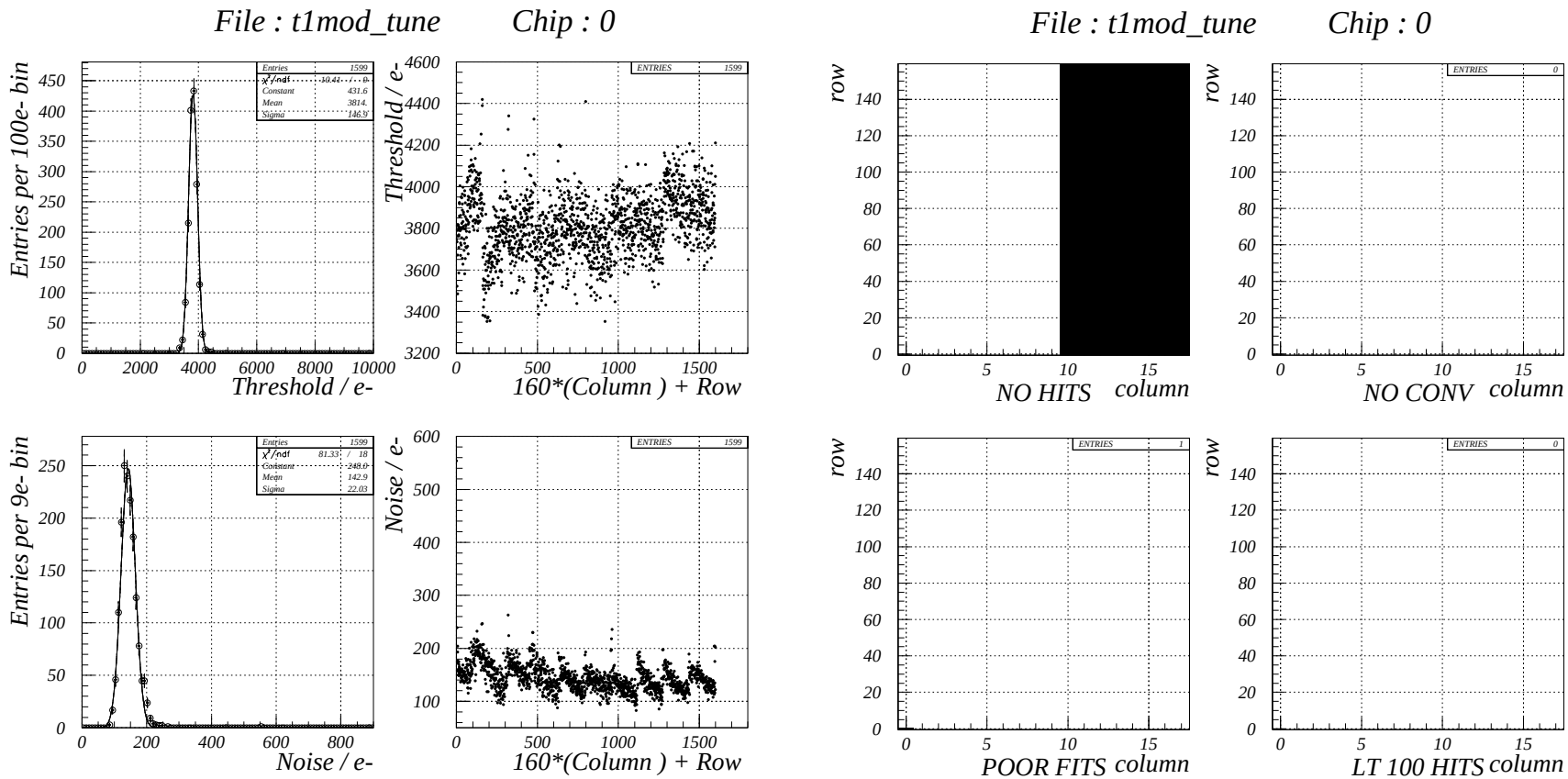
See that some of the chips do not show nice “tuned single chip” behavior, but rather show large systematic variations which increase the dispersion somewhat.

Behavior of noise for the individual chips:



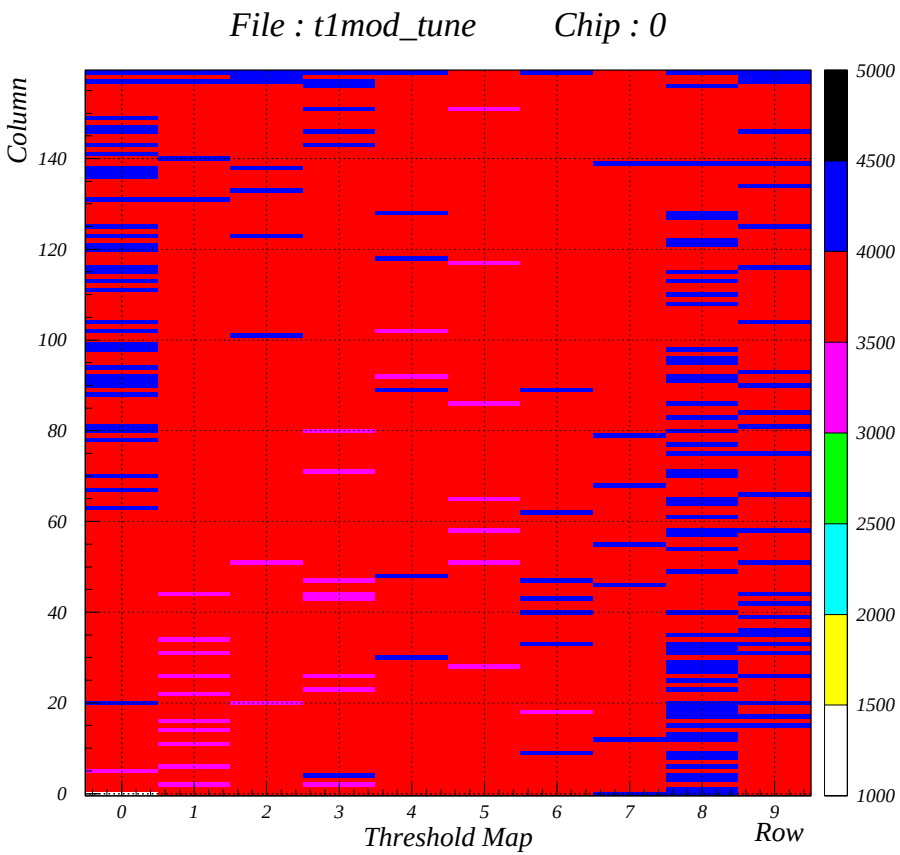
- Some of the chips have non-uniform noise behavior different than expected from single-chip behavior.

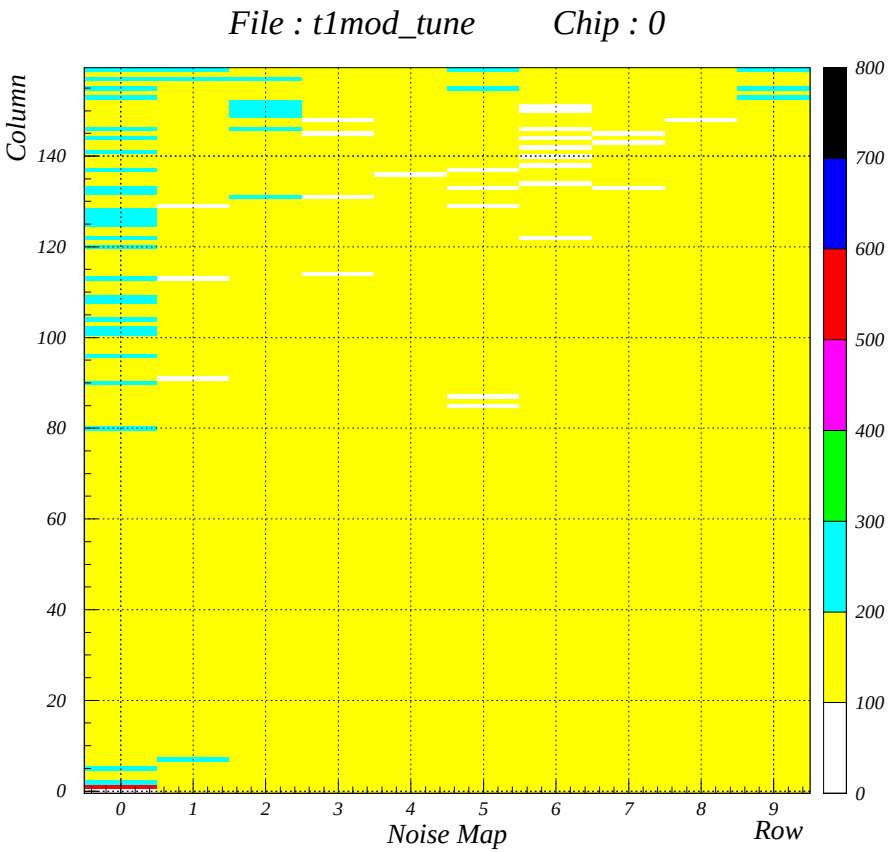
Threshold scan result for a typical good chip (Chip 0):



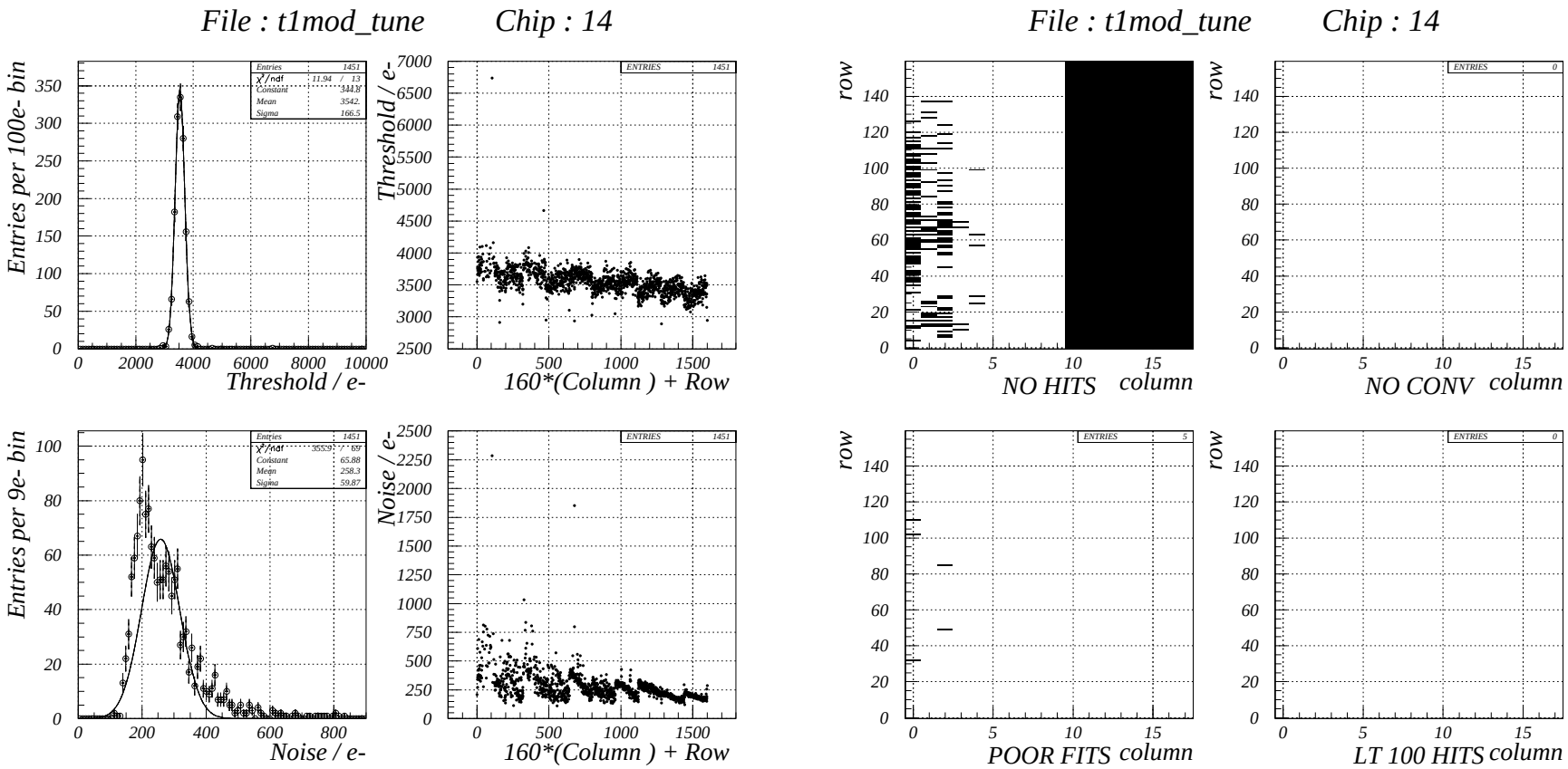
- Noise is worse than isolated single chip, but still acceptable. Threshold dispersion is good. Uniformity is not as good as for single chip assemblies.

- Threshold and noise map:

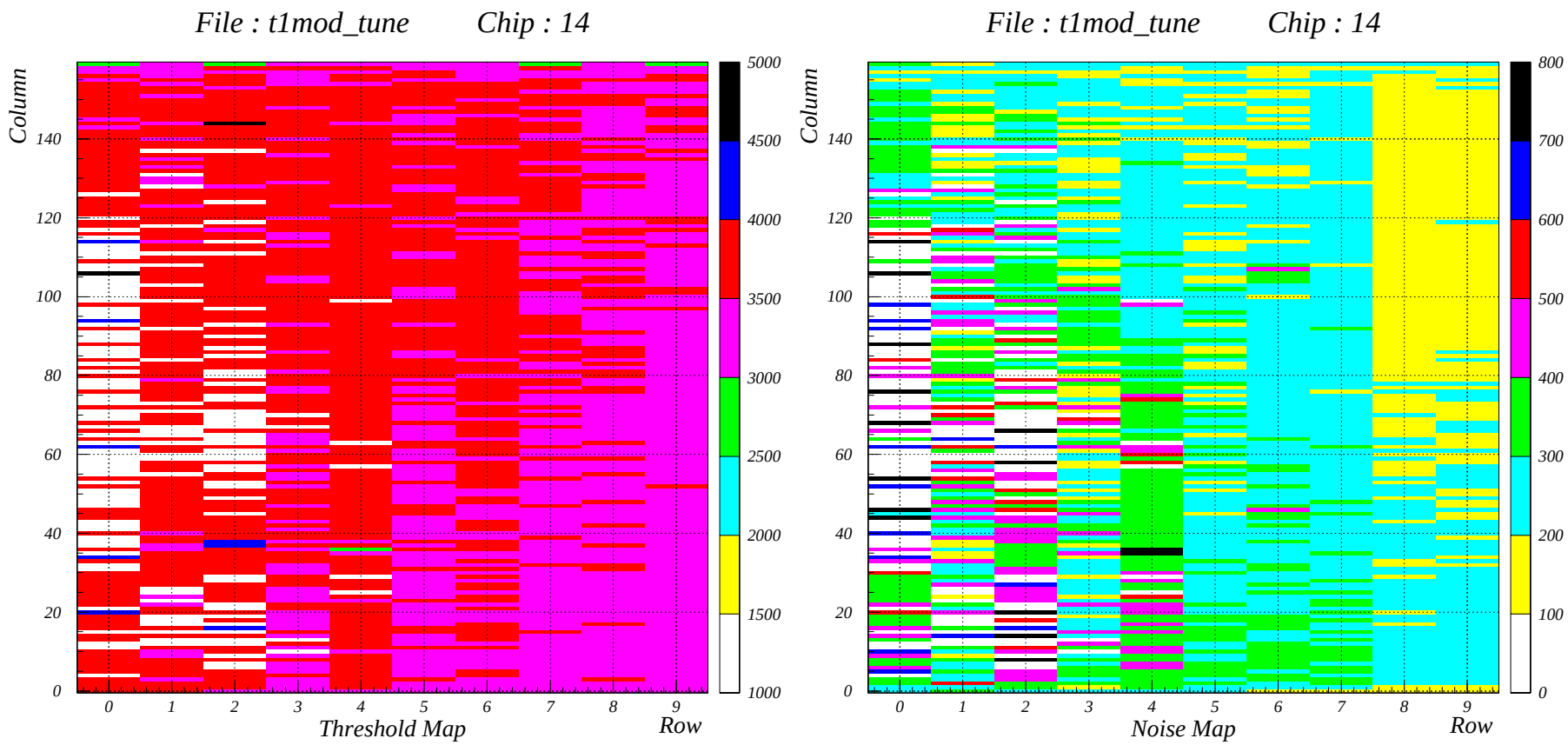




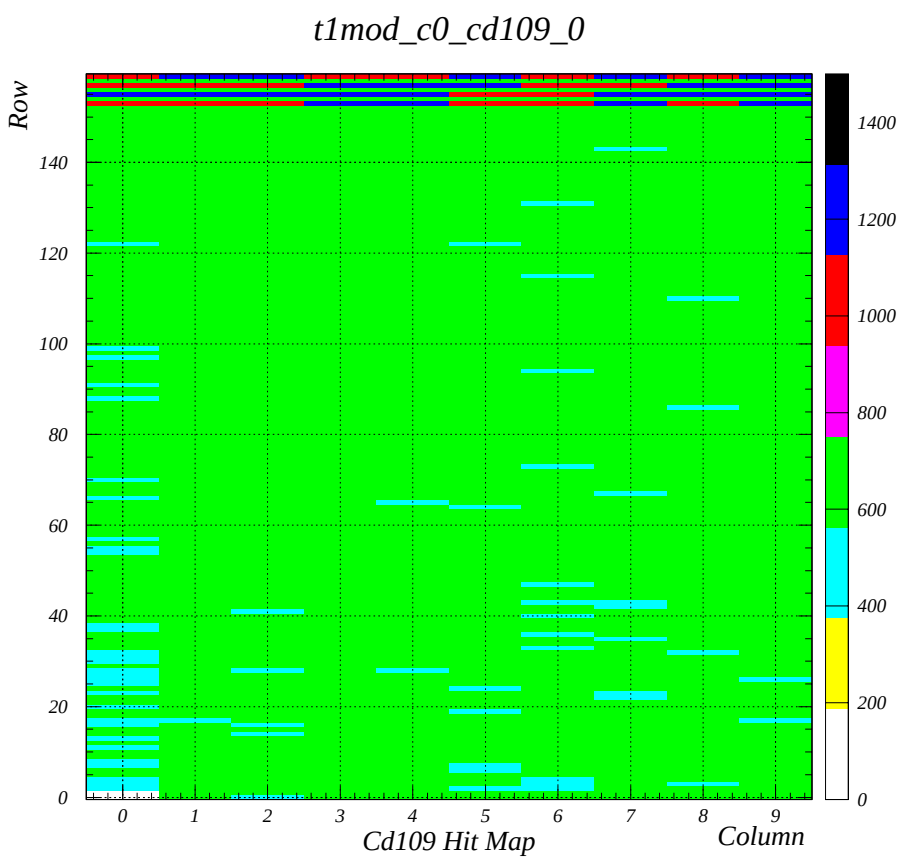
- Chip 14 is the only one with a significant number of dead channels:

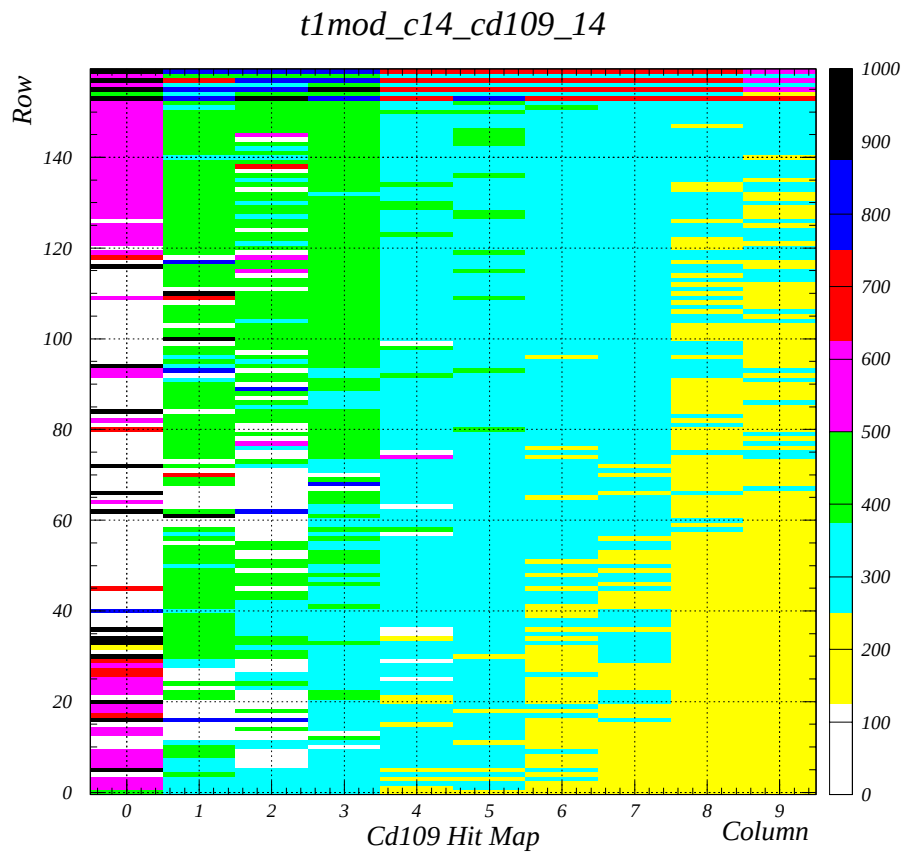


- Behavior near the dead channel region is quite poor:



- Source runs with Cd109 source have been made after tuning:



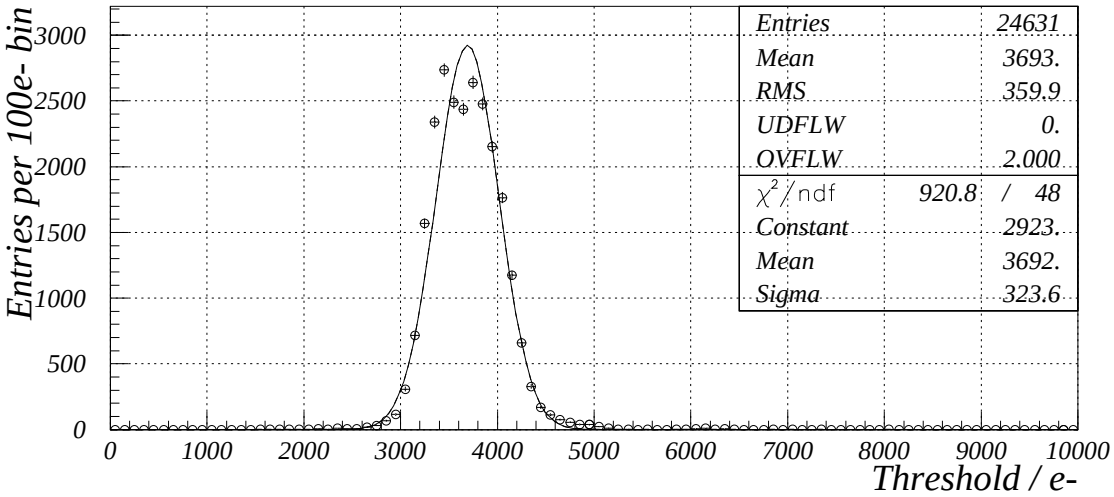


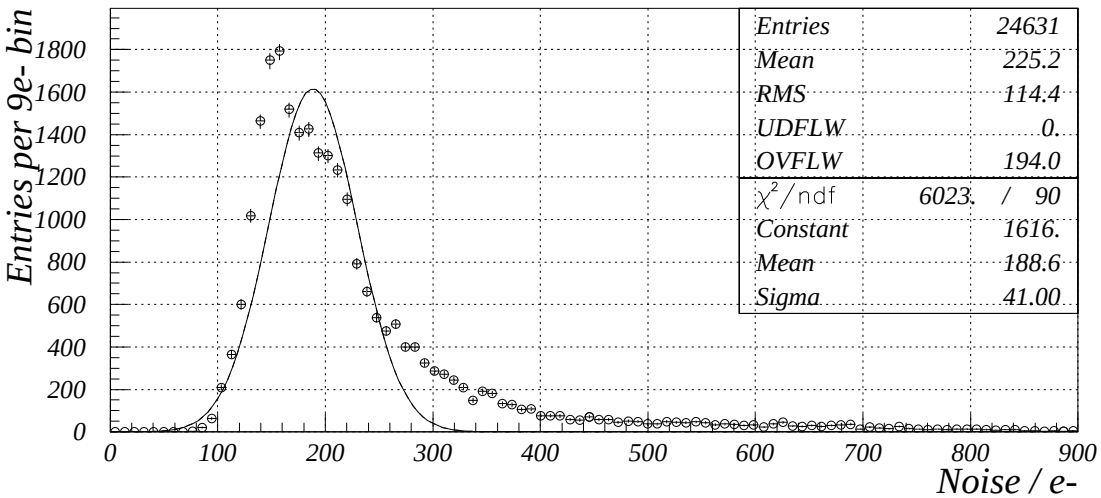
- Note Chip 0 and 8 in Tile have Column 0 400μ long, all others have 600μ.
- This module shows problems with “readout all” mode at nominal thresholds due to some instability (?). It is almost impossible to enable the entire chip. Instead source scans are made of parts of each chip and added to make full image.

Tile 2 module results:

Summary of performance with all chips tuned:

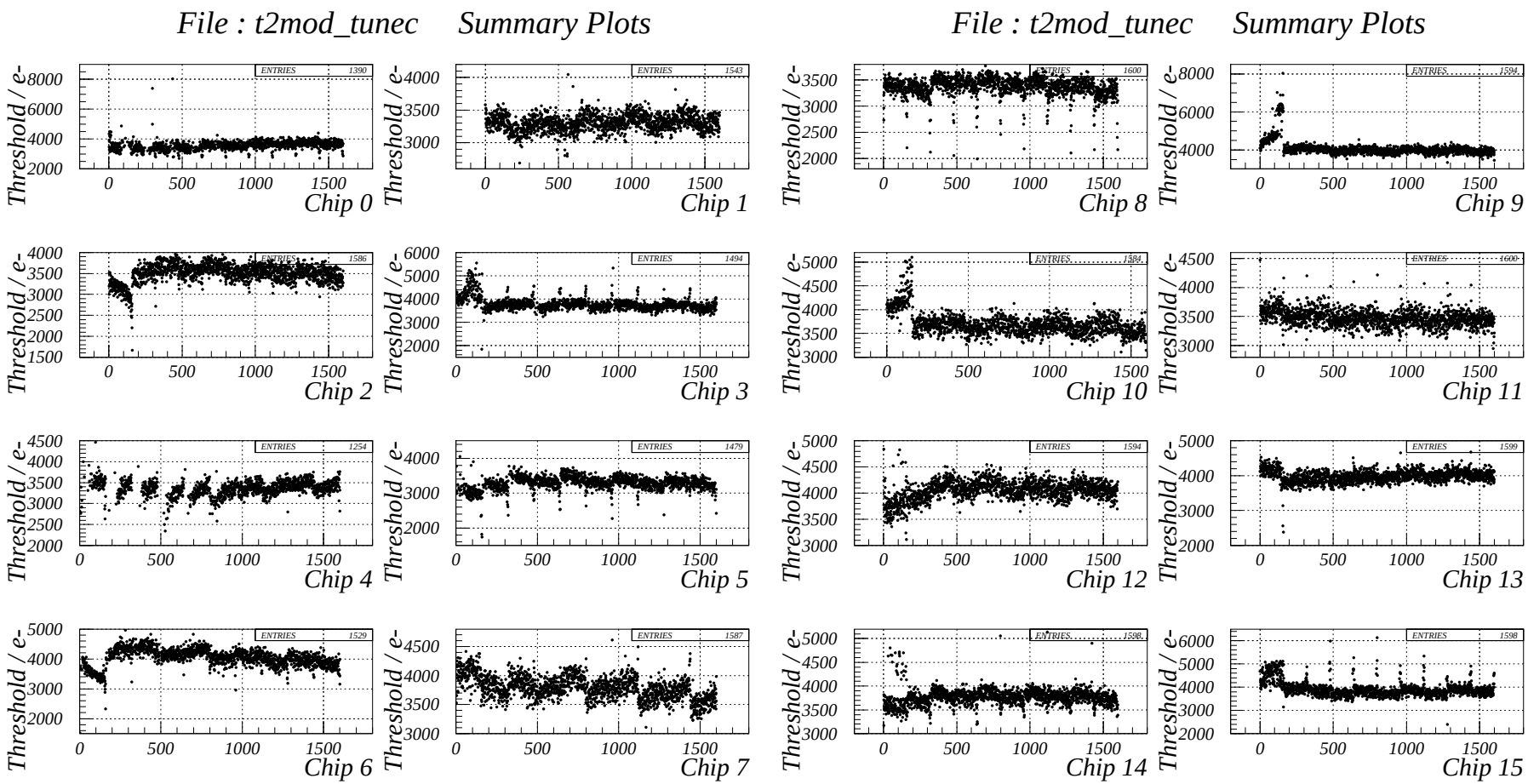
File : t2mod_tunec Summary Plots





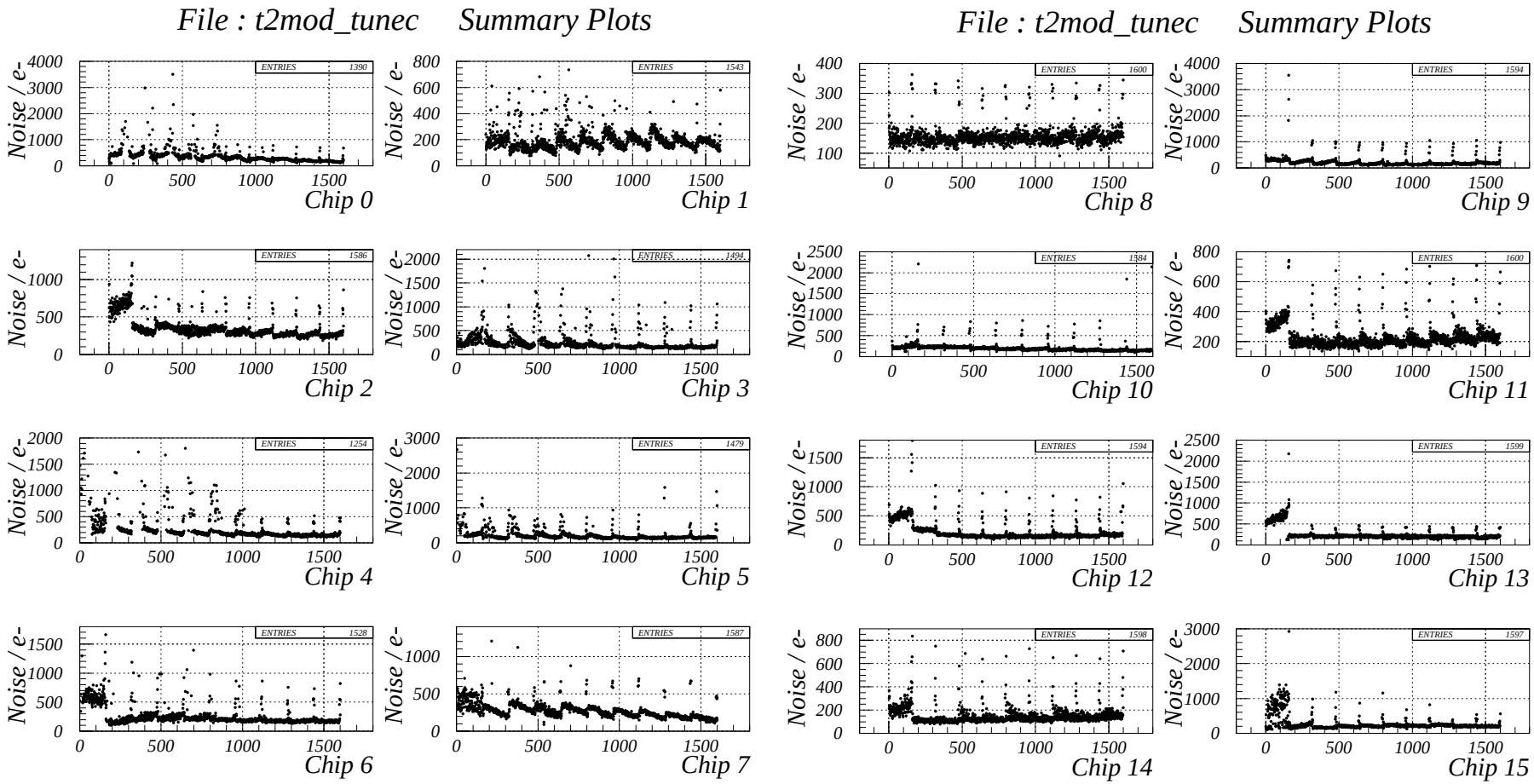
- Threshold dispersion is 320e, with no tuning of individual chip averages.
- Average noise is about 220e, with a tail going out to beyond 500e.
- Most of the tail in the noise distribution is for Column 0 channels, which are much noisier than expected in the Tile2 module (this feature is not present in the Tile1 module).

Behavior of thresholds for individual chips:



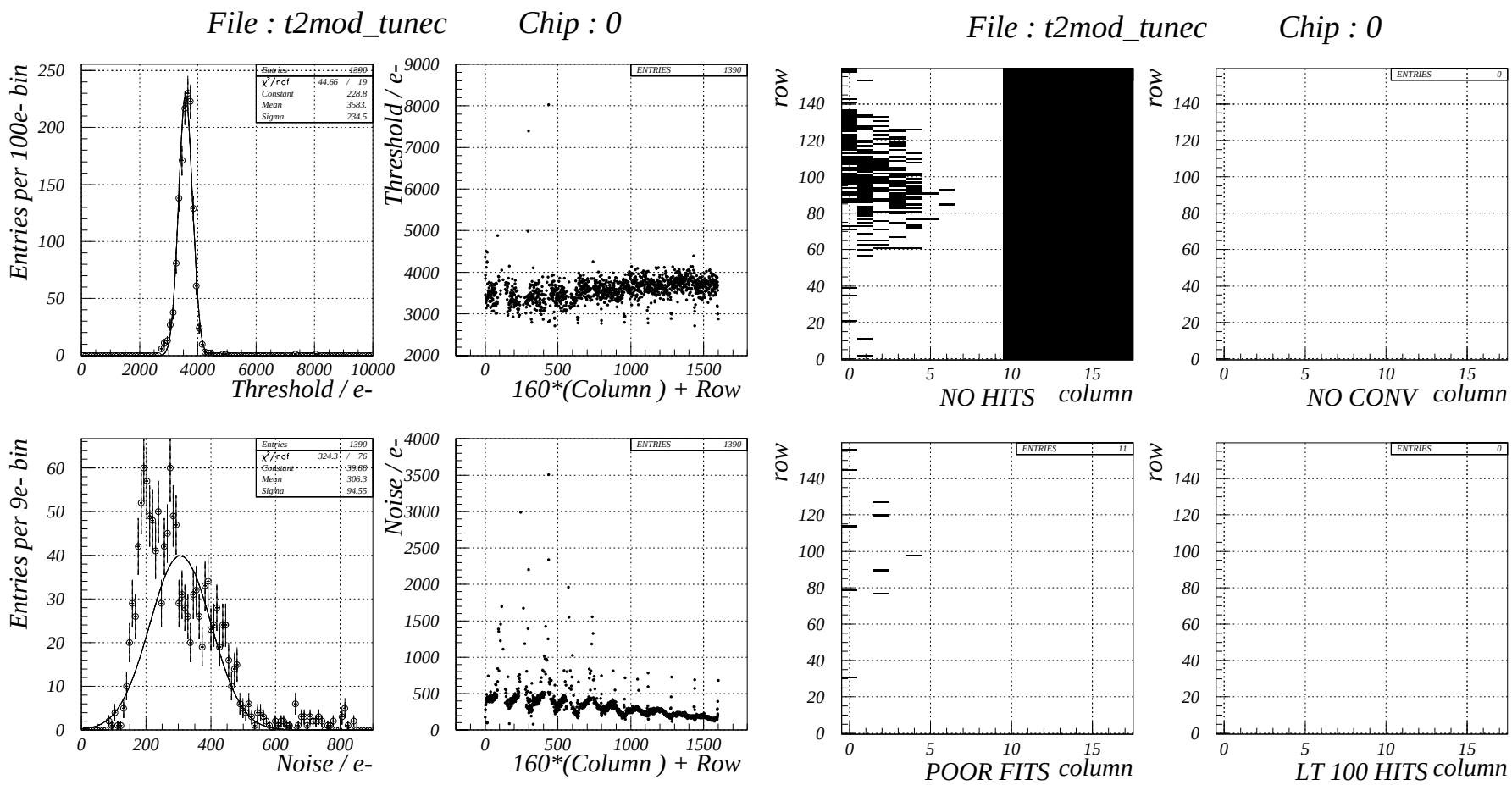
- Note poor behavior of column 0 in many of the chips.

Behavior of noise for individual chips:

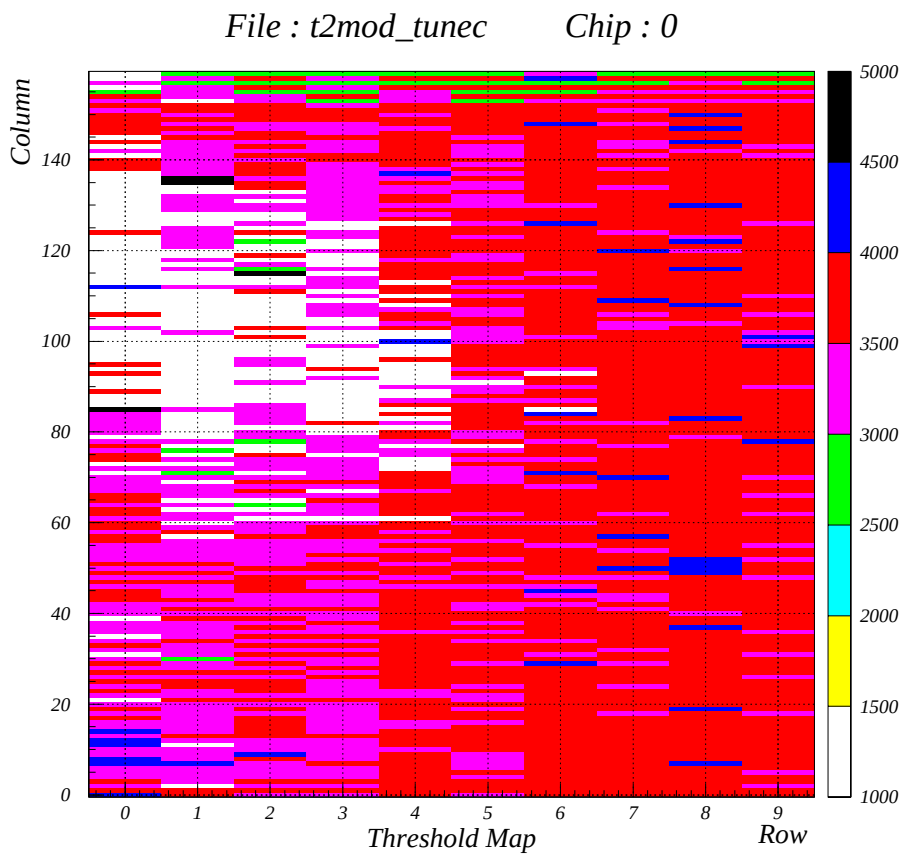


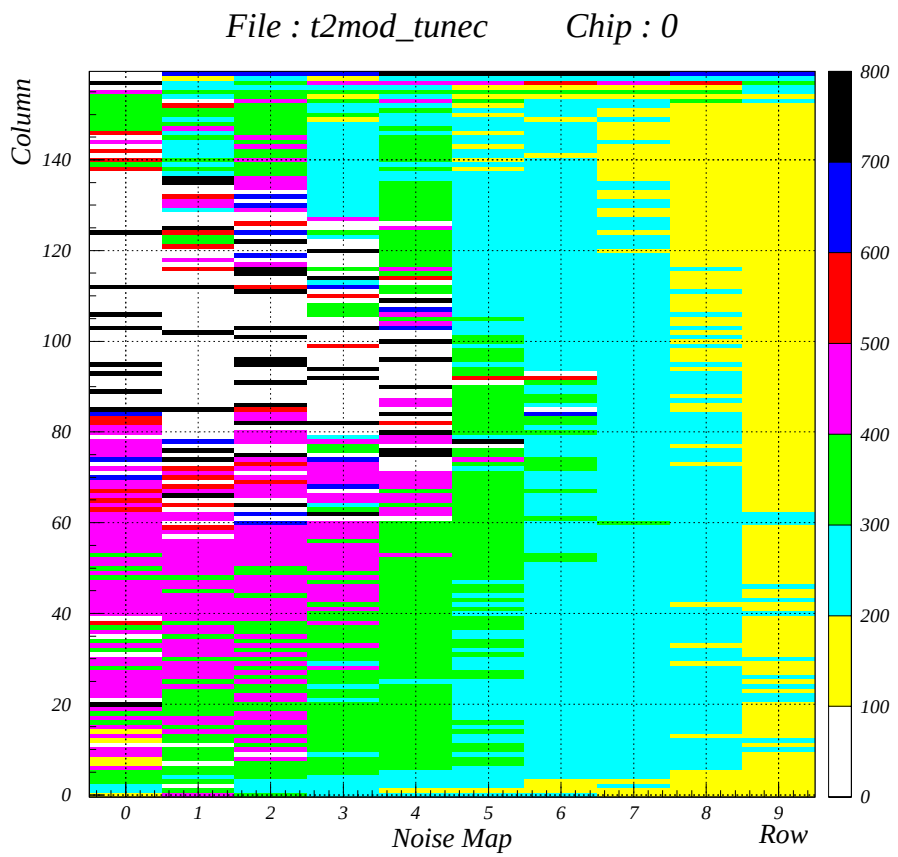
- Note unusually high noise in column 0 and in the ganged regions of the chips.

Example of chip 0, a chip with many merged bumps, tested with charge injection:



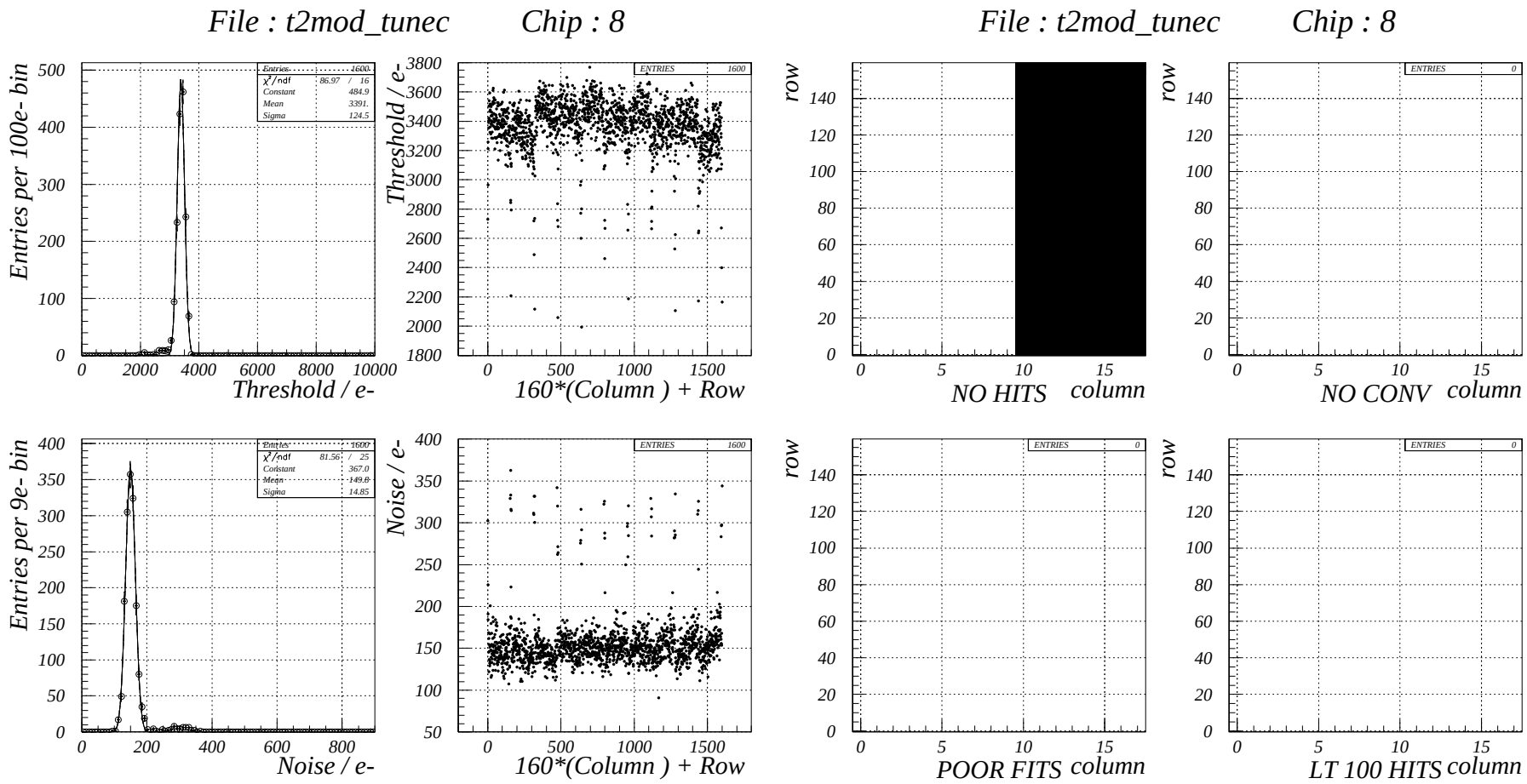
- Two dimensional map of threshold and noise behavior:





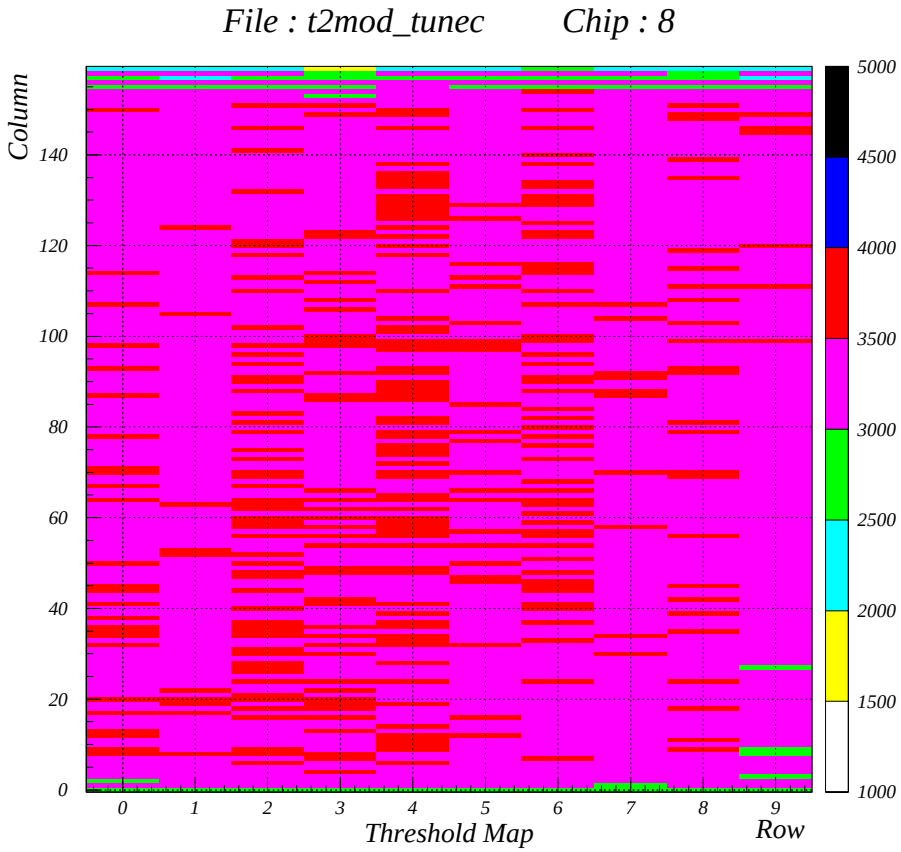
- Region near merged bumps has very poor behavior.
- It is difficult to operate this region in a “readout all” mode, as required for source tests and real operation in experiment.

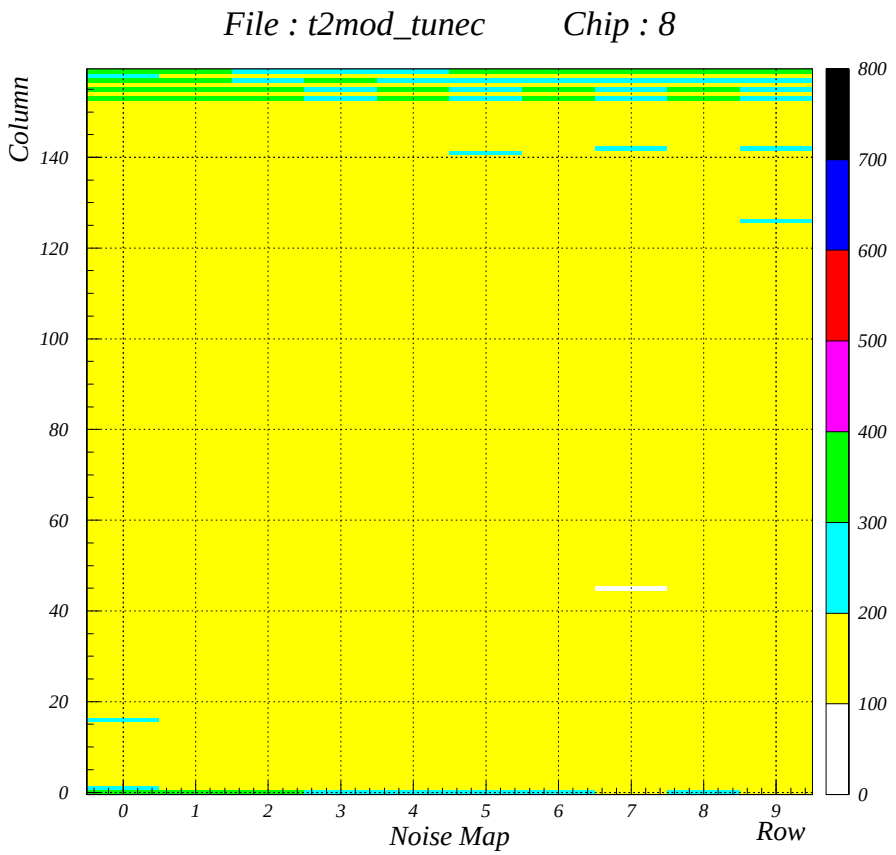
- Example of chip 8, an almost perfect chip:



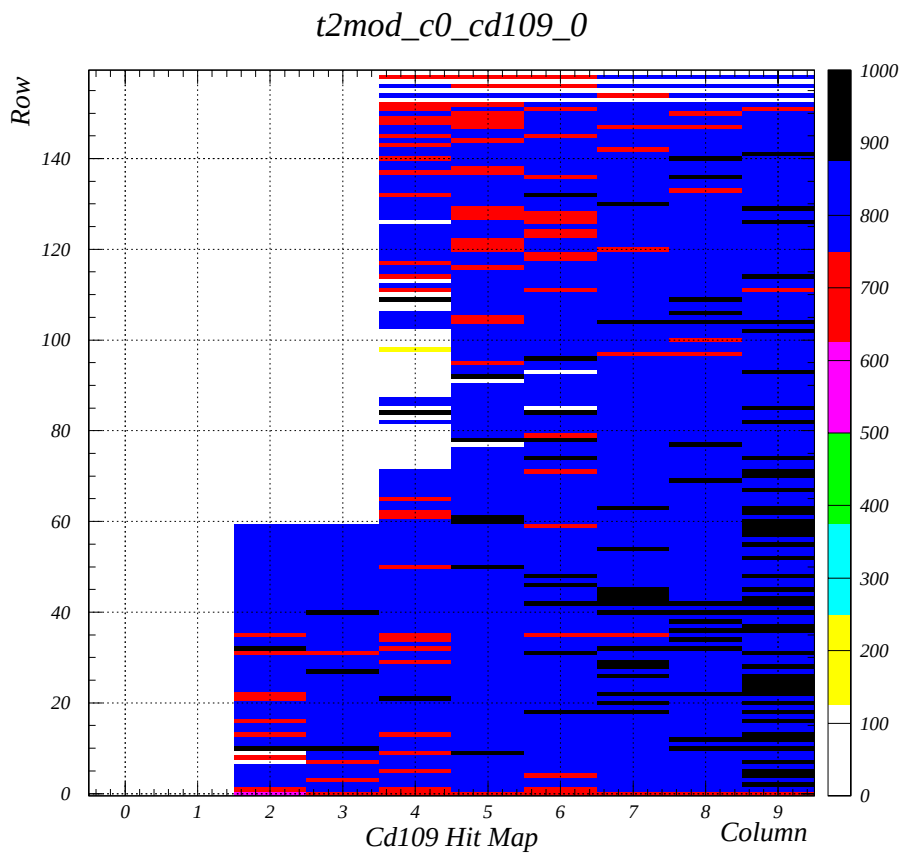
- This indicates that there is no intrinsic problem in the modules which prevents any chip from having good performance. Instead, it seems that for some collection of reasons, most chips do not achieve this expected level of performance.

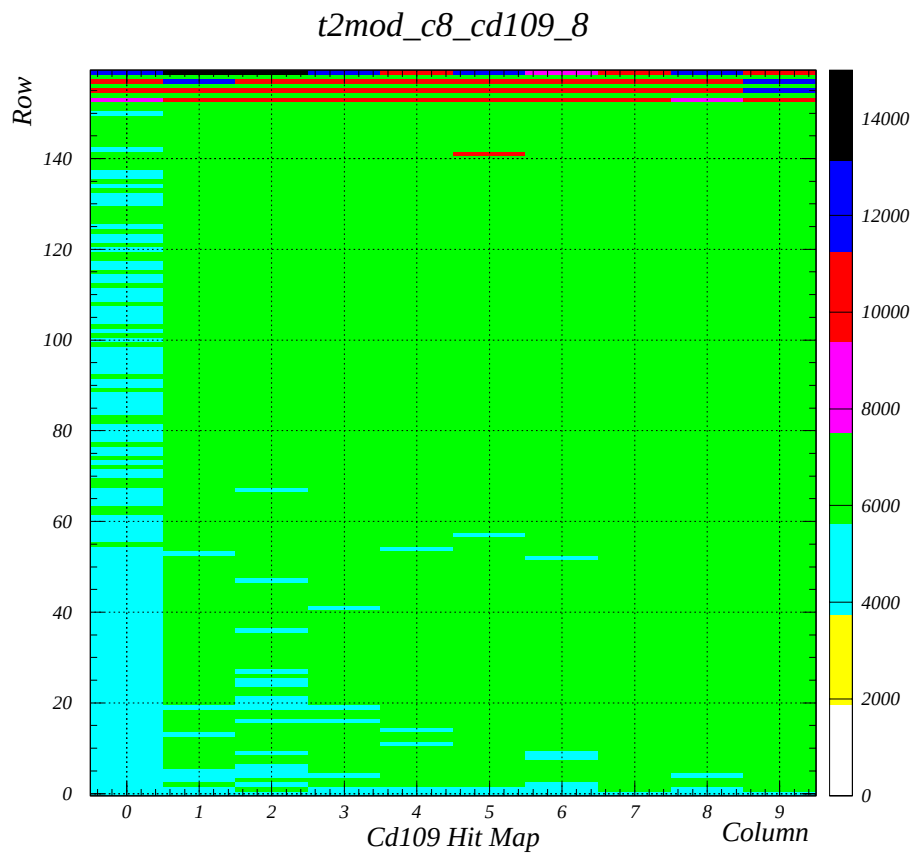
- Two dimensional map of threshold and noise behavior:





- Behavior with Cd109 source:





- This module shows no problem with operating in “readout all” mode, except on chips with large numbers of merged bumps, where it is necessary to enable only channels which have reasonable noise behavior.

General Observations on Modules

Two major differences relative to single chip operation:

- Significant noise increase for comparable operating point
- Instability of operation observed

Instability:

- For basic module support card, fully bonded, find that module can enter a “high current” state in which I(AVdd) increases from about 650 mA to about 900 mA.
- This seems to correspond to most or all channels in the full module “oscillating”. This is easily seen on the Hitbus, or when doing a threshold scan and finding many hits below threshold.
- After adding additional decoupling capacitors, this state has never been seen again. At low thresholds, when trying to run in “readout all” mode for a source scan, similar behavior can be observed at the single chip level. In this case, perhaps 50% of the chip can be enabled for readout, but not all of it. When operating in this reduced readout mode, no hot or noisy pixels are observed, so the problem would seem to be related to a coherent “digital crosstalk” effect. However, looking at the LV power lines or the test pixel preamp output and doing an FFT analysis shows no sign of large peaks at the column readout frequency (5-10 MHz), as would be expected for digital crosstalk.

High Noise:

- For most studies, the preamplifier feedback current (FPDAC or DAC1 in FE-B) was set to 5, corresponding to about 1.5 µs return to baseline for 20Ke charge. At this operating point, we typically observe about 110e of noise on both ST1 and ST2 detectors (single chip devices on the single chip support card).
- For the modules, minimum noise values in the range of 150-200e are observed. However, noise levels of up to even 400e or 500e have been observed. For some chips, these measured noise values change significantly from one threshold scan to the next in an apparently random way. Sometimes, there is even a corresponding “column-dependent” threshold shift observed.

Module Concerns

Many sources of “coherent” effects that do not show up in single chip assemblies:

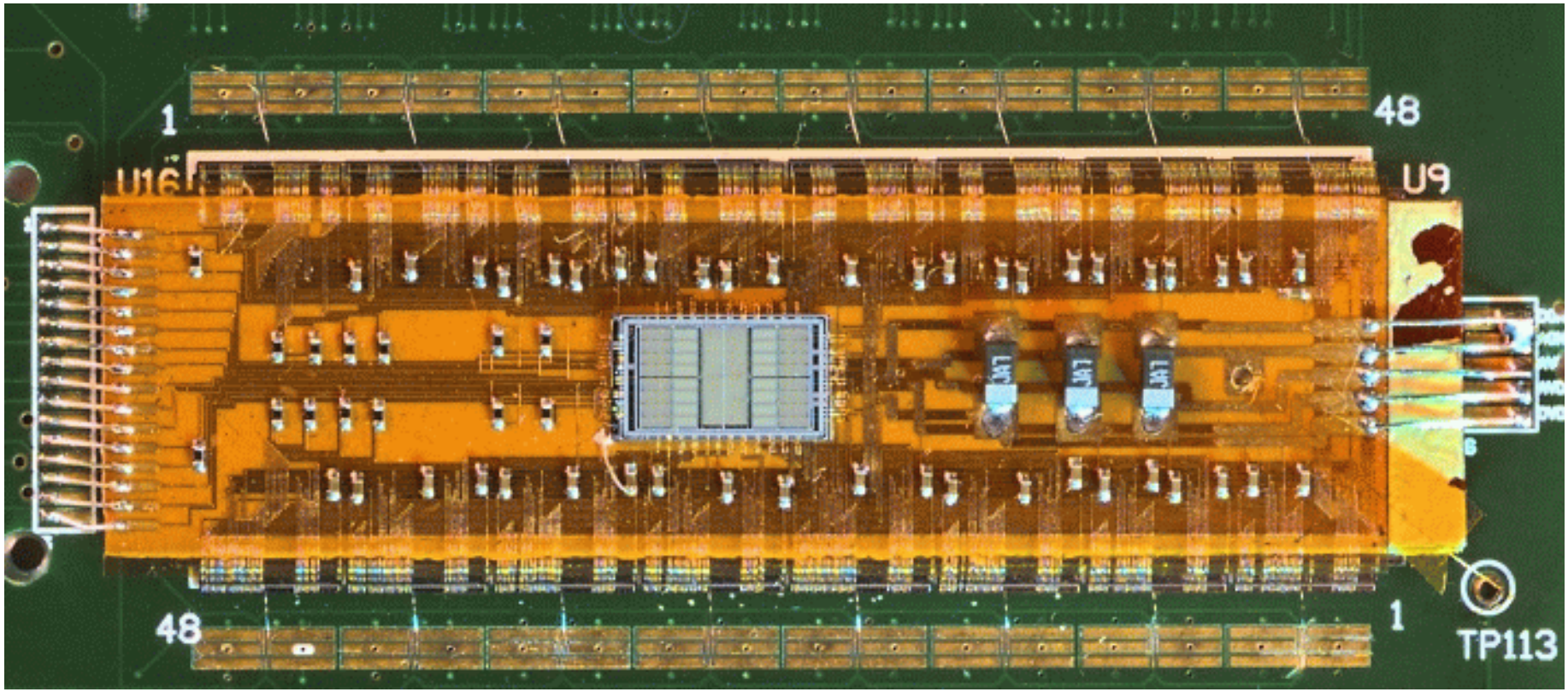
- FE chips can communicate via power supply lines if the decoupling is not adequate.
- FE chips can communicate via large sensor substrate, especially through shared structures (p-stops, guard rings, etc).
- Noise levels on the LV or HV supplies can be larger due to PC board layout, etc.
- There can be more analog-digital cross-talk within the chips because of poor substrate contacts.
- There can be greater coherent digital activity (all 16 chips have a clock with the same phase) induced on the shield in FE-B which could couple into the detector or into AGnd.

Two tests to occur soon (should have results by end Feb):

- All modules so far made using Indium bumps. There are many “merged bumps” observed, and some evidence that the noise is high in part due to residual oxide layers causing high series resistance. Very eager for solder-bumped modules !
- Wafers prepared with gold backside plating to check importance of high quality backside contact in module construction. They are now being bumped by IZM.

Results on first LBL Flex module:

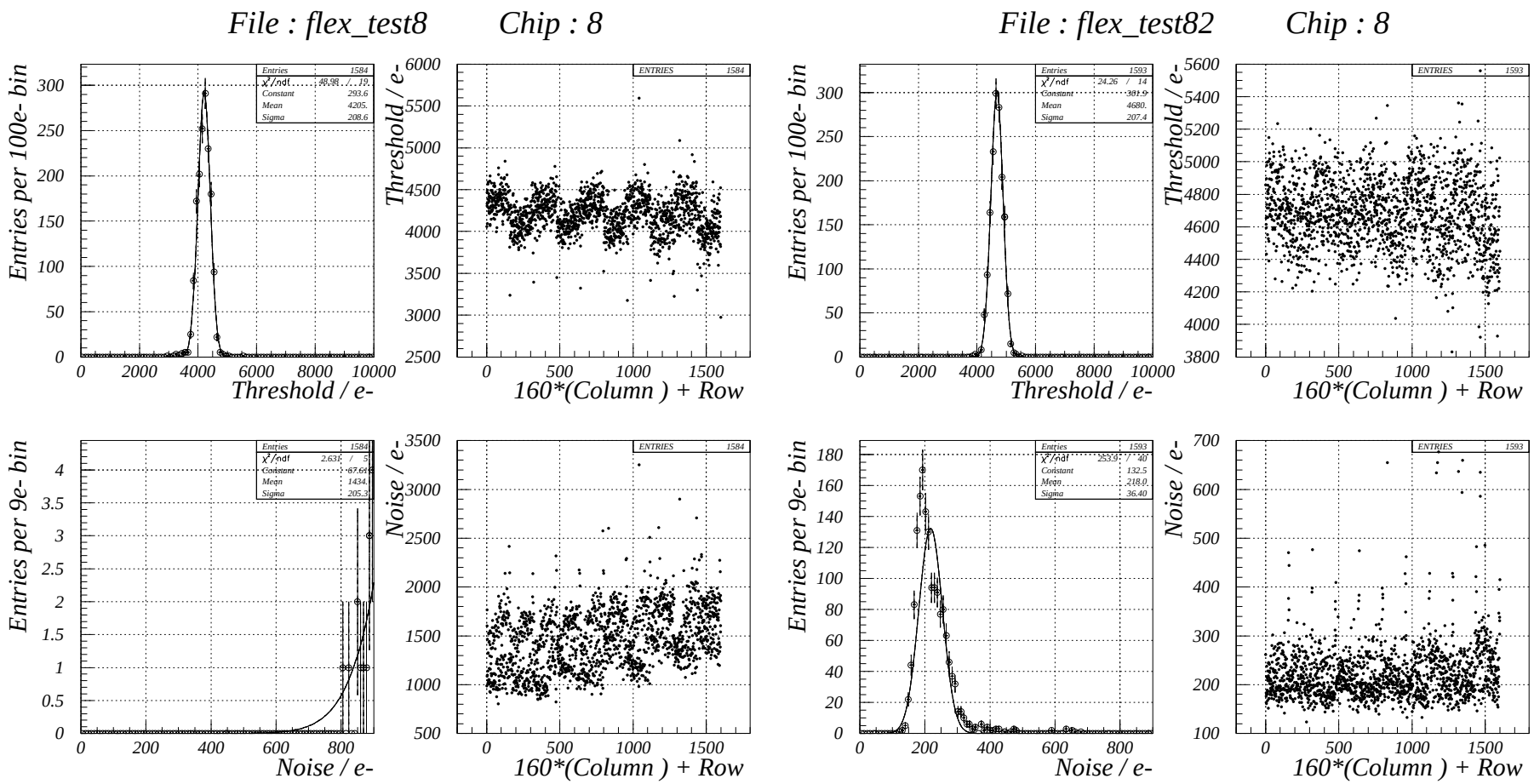
- Module was the last Boeing module, which was built using a CIS Tile1 detector and chips from a wafer that had been thinned to 150µ by GDSI. The thinning was done by cutting the wafer in half after bumping, protecting the bumps, and back-grinding. The dicing was done by GDSI. We had fun pulling the die off the dicing tape (tweezers don't work on such thin die...) The flip-chipping was done without any problems by Boeing.



Summary of Flex module behavior:

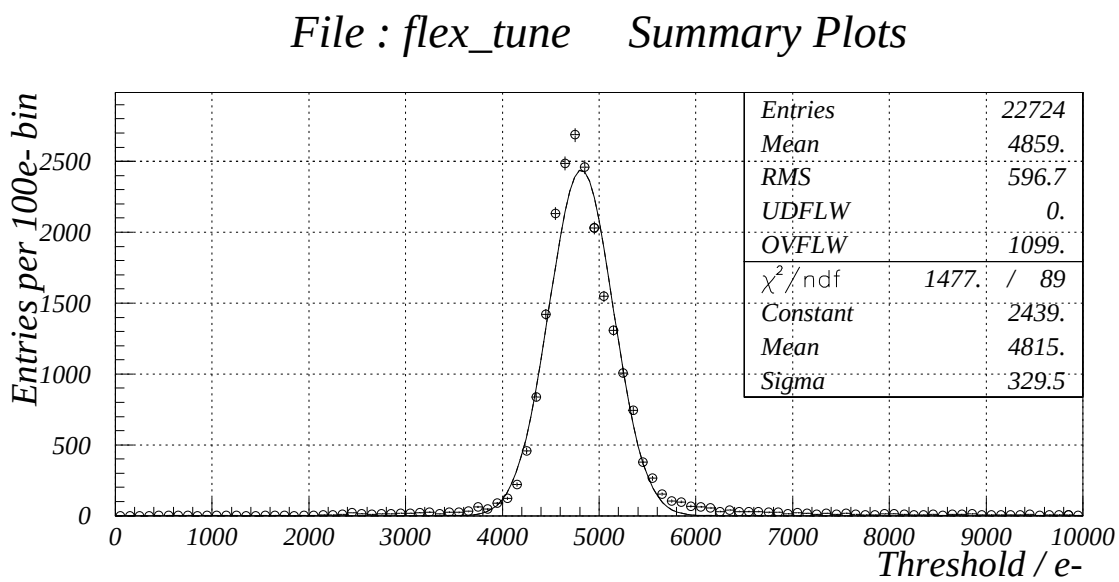
- All 16 FE chips plus the MCC work perfectly from the digital point of view
- Chip 15 does not respond to analog charge injection, although all analog nodes have correct signals and voltages when probed with picoprobe, and it operates correctly with a source in Hitbus mode.
- There are many bump-bonding problems, including several chips with regions of merged bumps. There are several very noisy chips that upset the operation of the entire module.
- No sign of high current state observed, in spite of the minimal decoupling (0.01 μF 0402 capacitors roughly for each chip), suggesting that better backside grounding is a contributing factor to this problem. However, if the module is operated with all chips operational (FE biasses correct), then it is very noisy.
- Noise levels are reasonable on some chips which have no serious bump-bonding problems, once the CINDAC (input transistor bias) is turned off on the noisy chips. Noise levels are very high on many other chips. Overall, this performance seems poorer than for “bare” modules, perhaps due to more limited decoupling, or perhaps due to problems from very thin chips. All results from this module are measured with CINDAC=1 on all chips except the one under study.
- Module was modified to add Hitbus source test capability (left off of the first generation Flex Support Card), and source characterizations were performed.

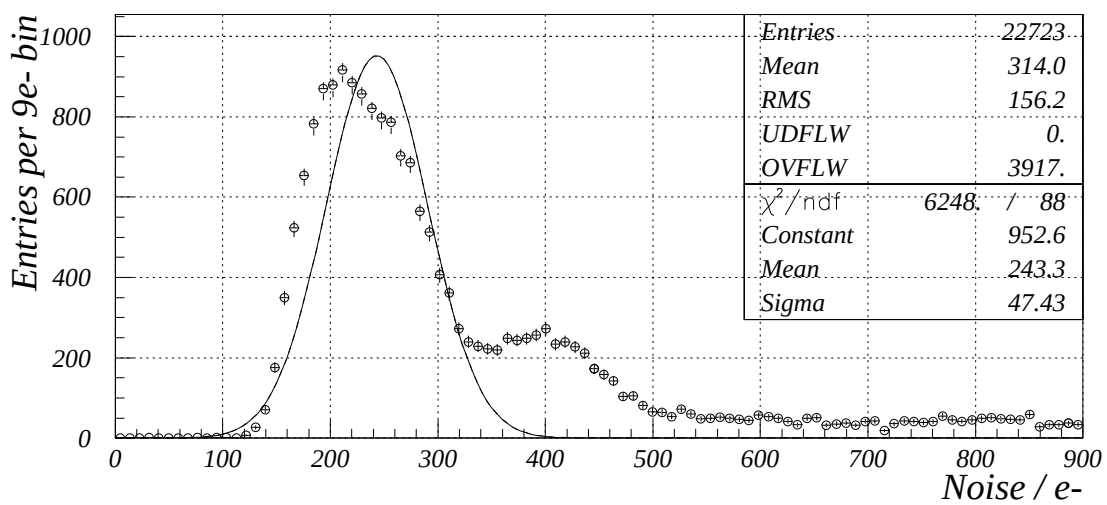
Comparison of behavior with all FE chips on, and all off except chip under test:



- Noise decreases dramatically from above 1000e to about 200e.
- The same improvement is obtained if the 3 worst chips on module are turned off

Summary of behavior of 15 characterizable chips:



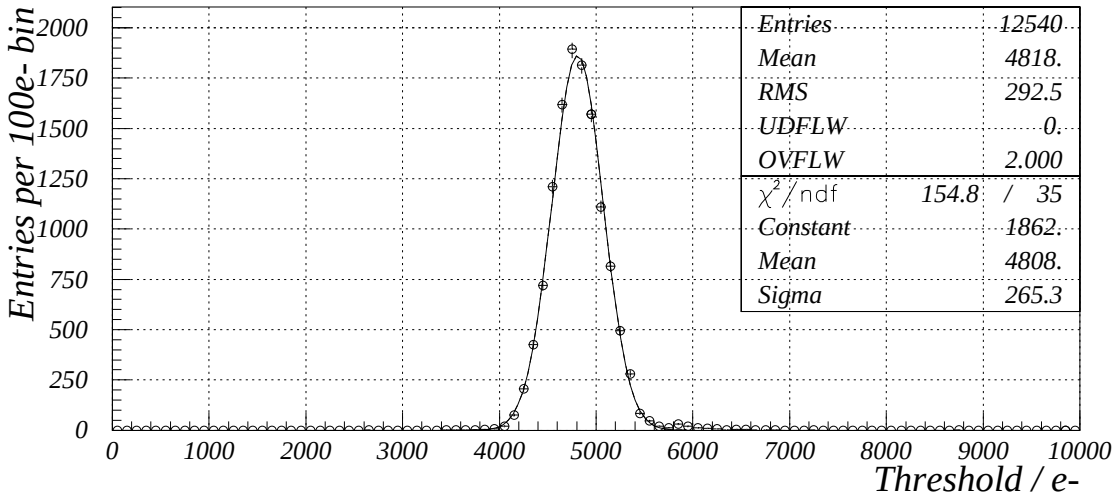


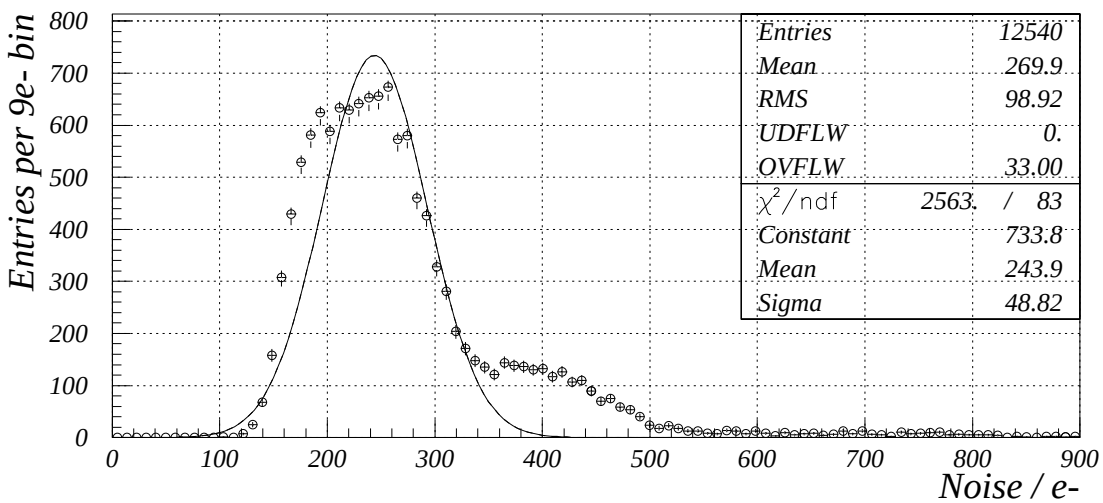
- Overall threshold dispersion is about 330e.
- Average noise is moderate for those channels in the plot, but there is a long tail, and there are several thousand off-scale entries.

- Note: all measurements made with CINDAC=1 on 15 of 16 chips

Summary of eight "good" chips (0,1,3,6,7,8,12,14):

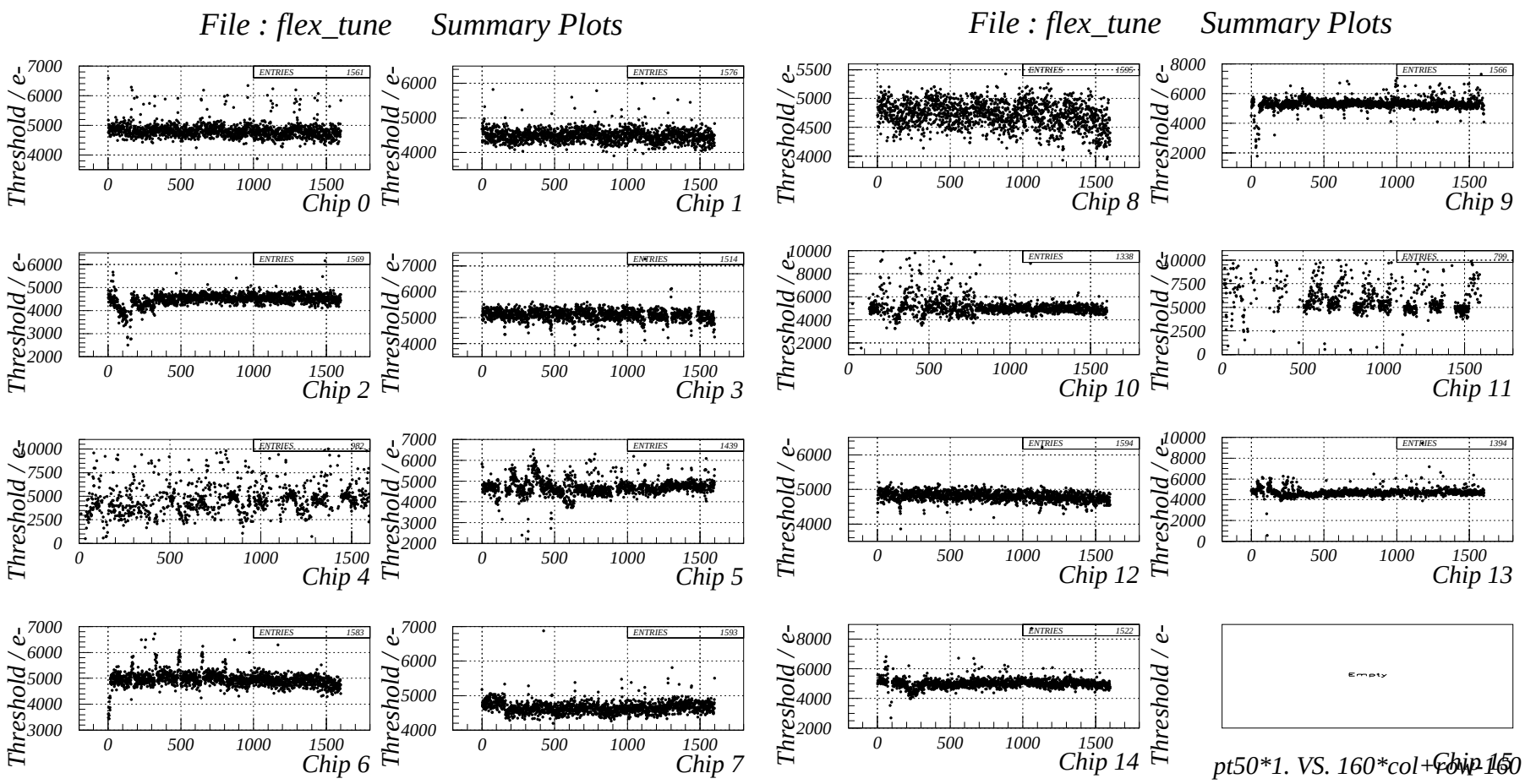
File : flex_tune_good Summary Plots



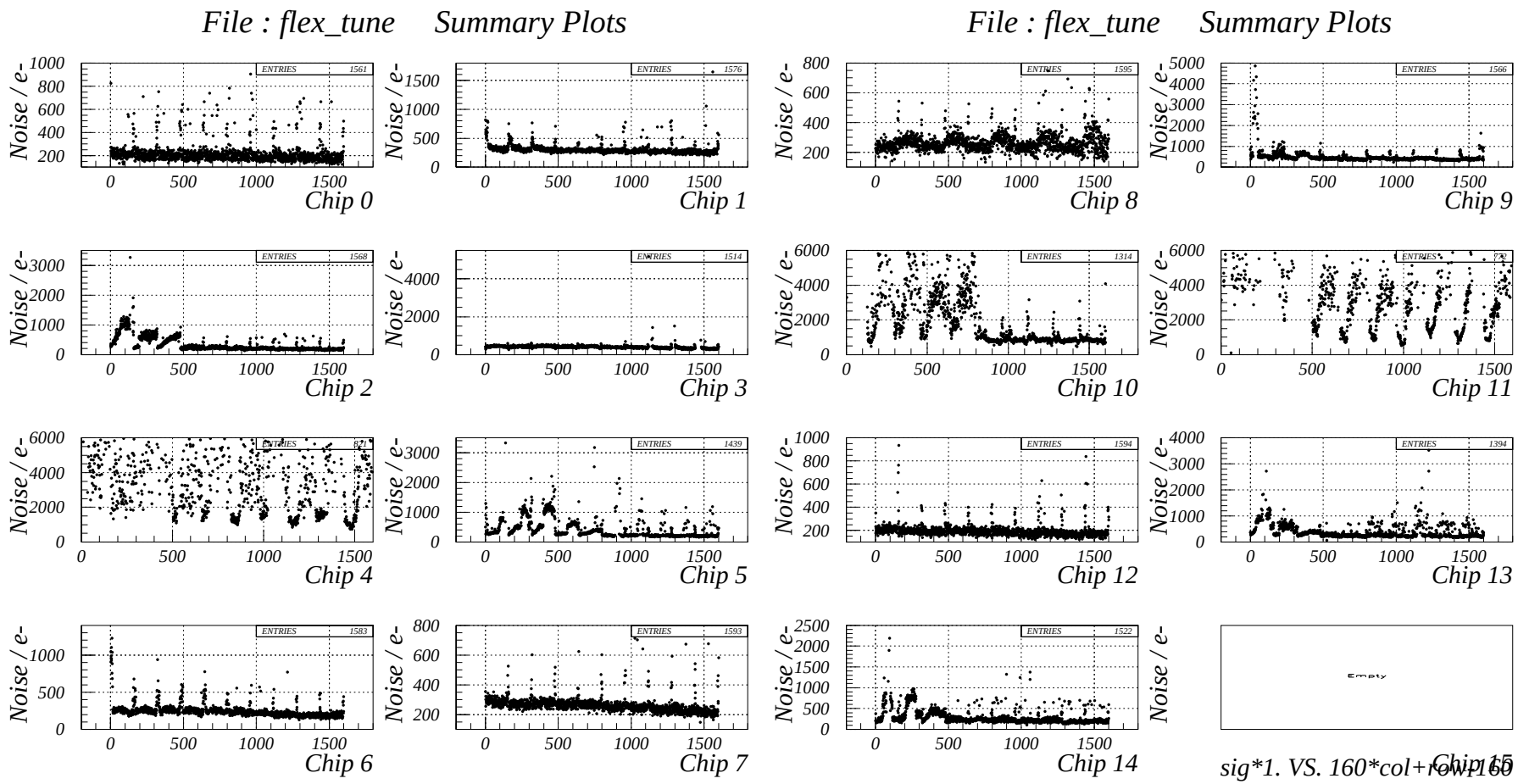


- Dispersion is reduced to 265e
- Very high noise tail has disappeared, with mean noise now 270e, and essentially no overflows.
- One of the good chips is right under the MCC (chip 12), so there is no indication that the presence of this bare die on top of the sensor causes any problems.
- Other good chips are at both ends of the Flex, so there is no indication of systematic problems due to power or signal bussing

Threshold behavior for individual chips:

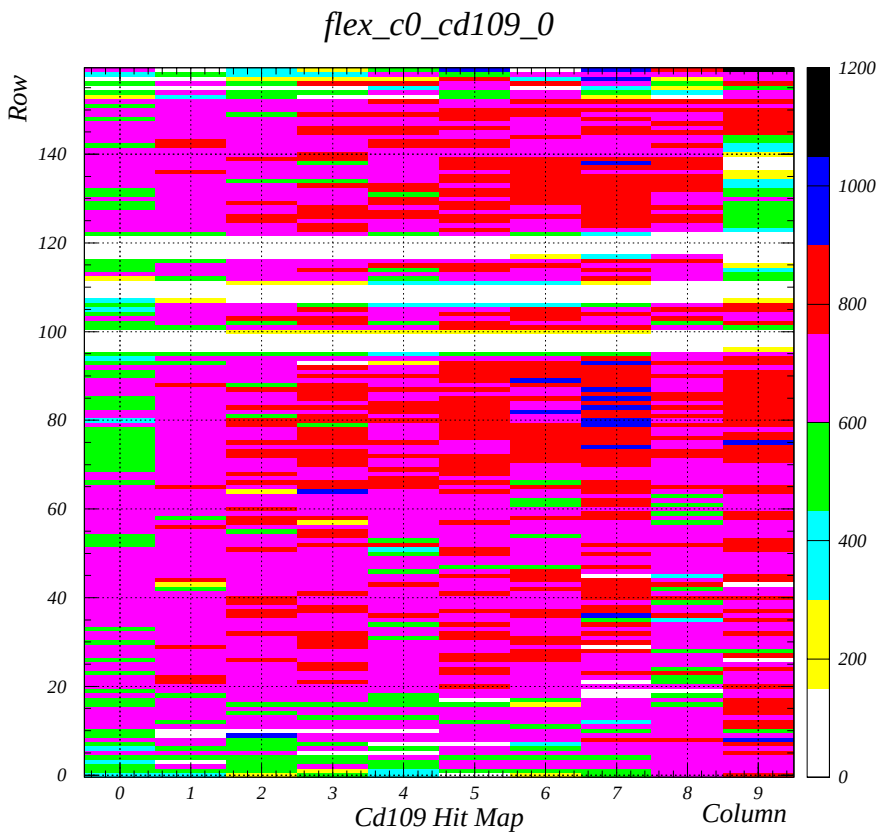


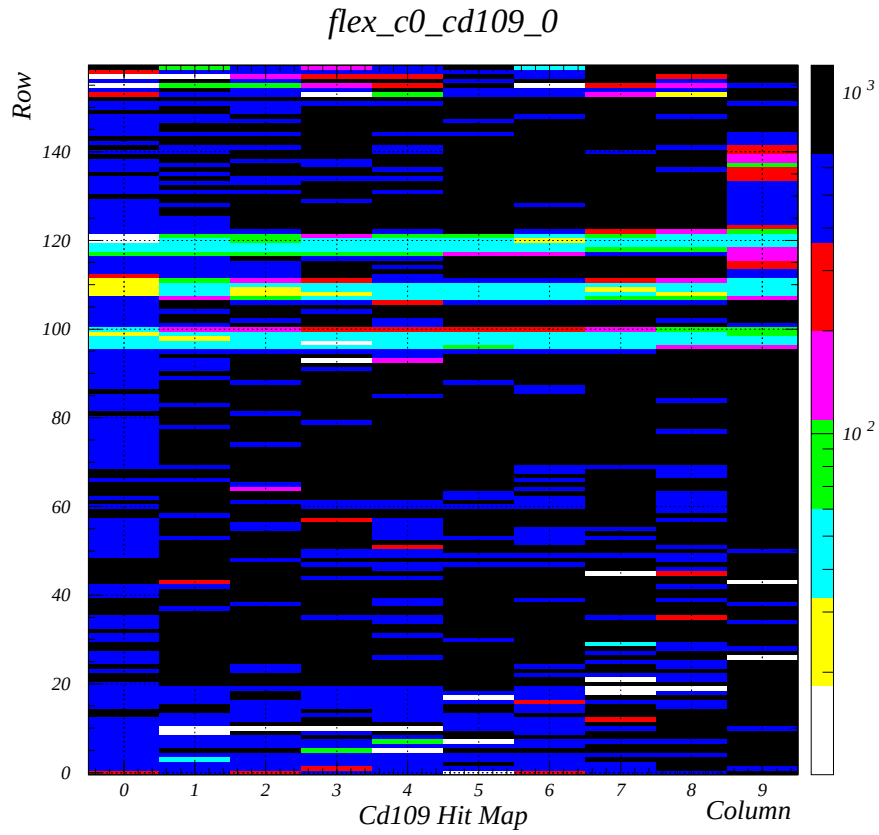
Noise behavior for individual chips:



- Chips 4,10,11 have extremely poor noise behavior, worse than anything seen before. Perhaps this is a problem with the thinned die.
- The good chips have noise behavior which is as good as that in “bare” modules.

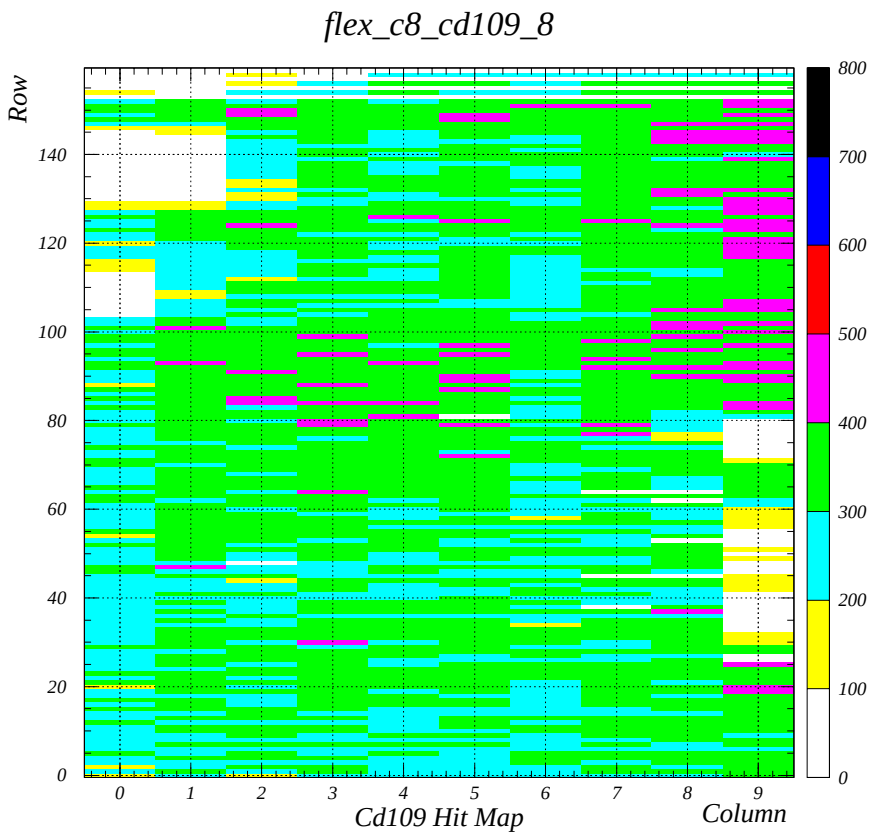
Source characterizations with Cd109 source:

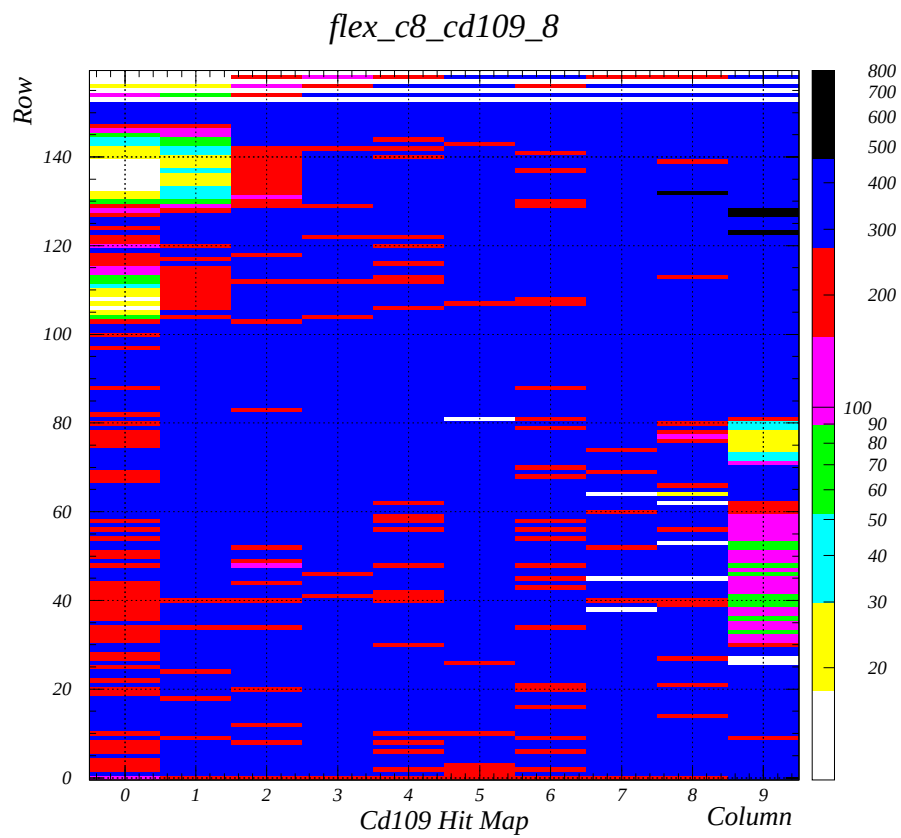




- The source is strongly attenuated in the material on top of the Flex. The three parallel lines are the leads of a Pt100. A termination resistor is visible in Column 9.

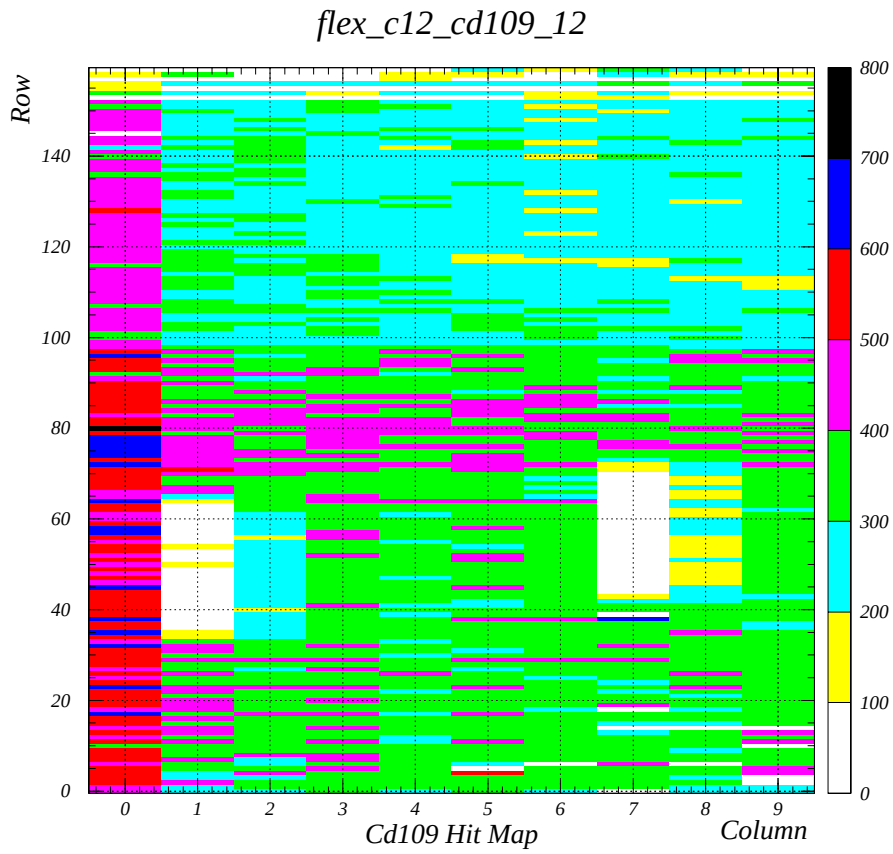
- Source map of Chip 8:

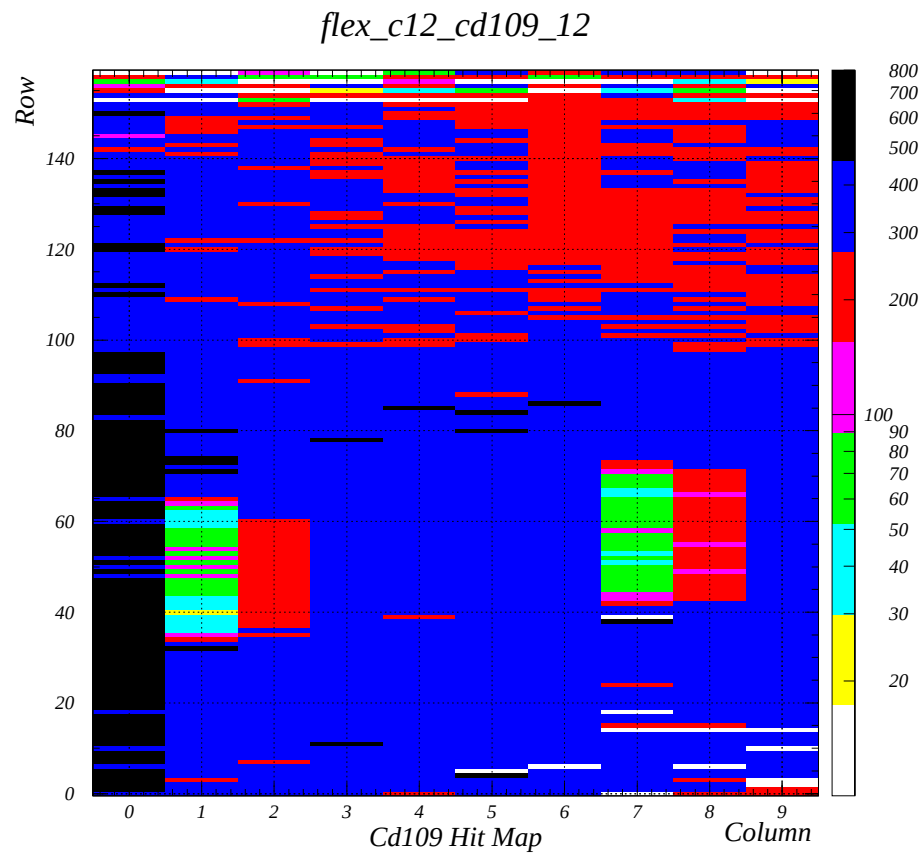




- Holes in upper left are due to wires bringing power into Flex, plus two decoupling capacitors are visible in Column 9.
- Due to these effects, a low enery photon source is no longer useful for checking uniformity of response of a module. A higher energy source (such as a β source) is needed.

- Source map of chip 12:



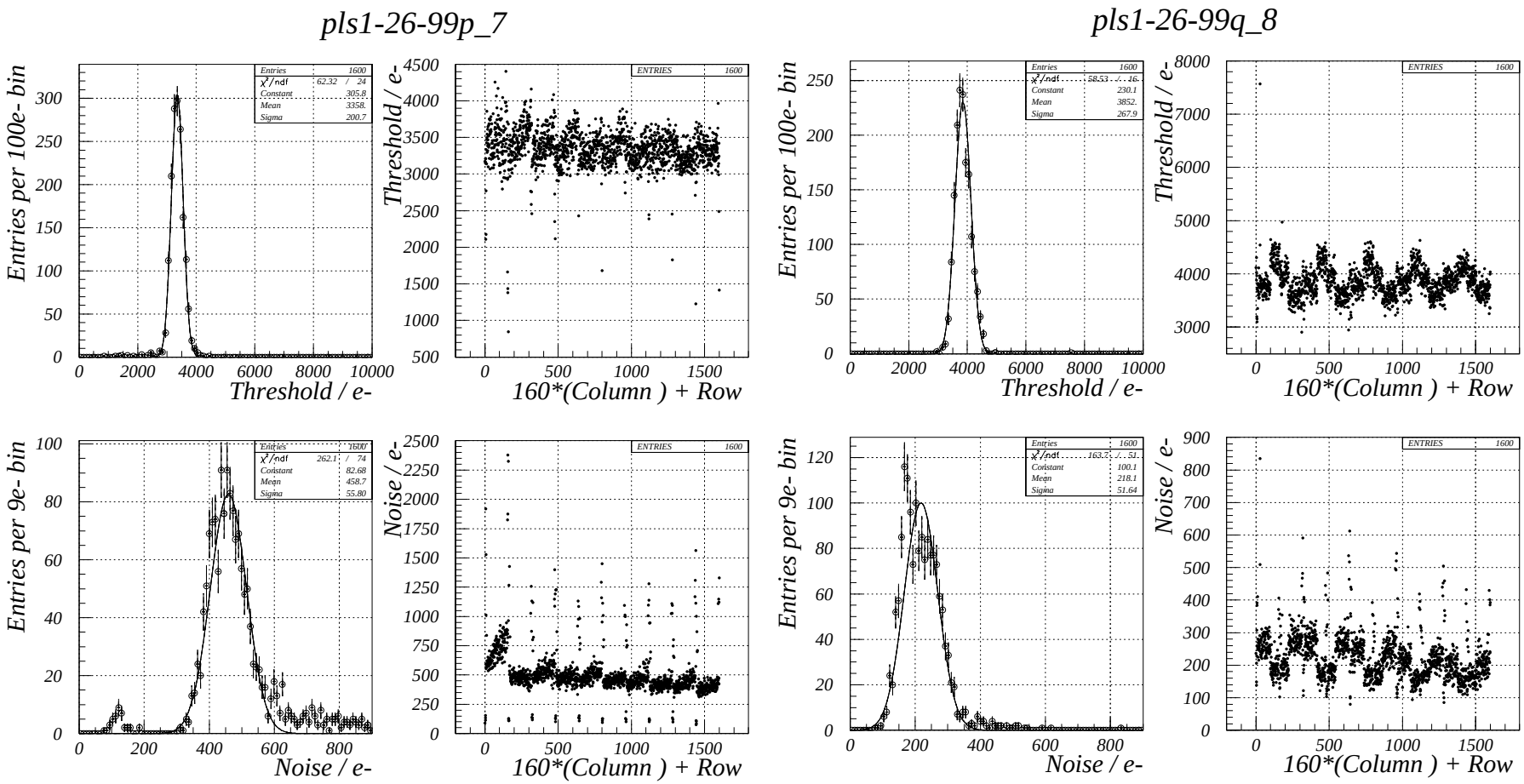


- See the shadow of the MCC in the upper half of the chip, as well as two decoupling capacitors.

Results from first UOK Flex Module

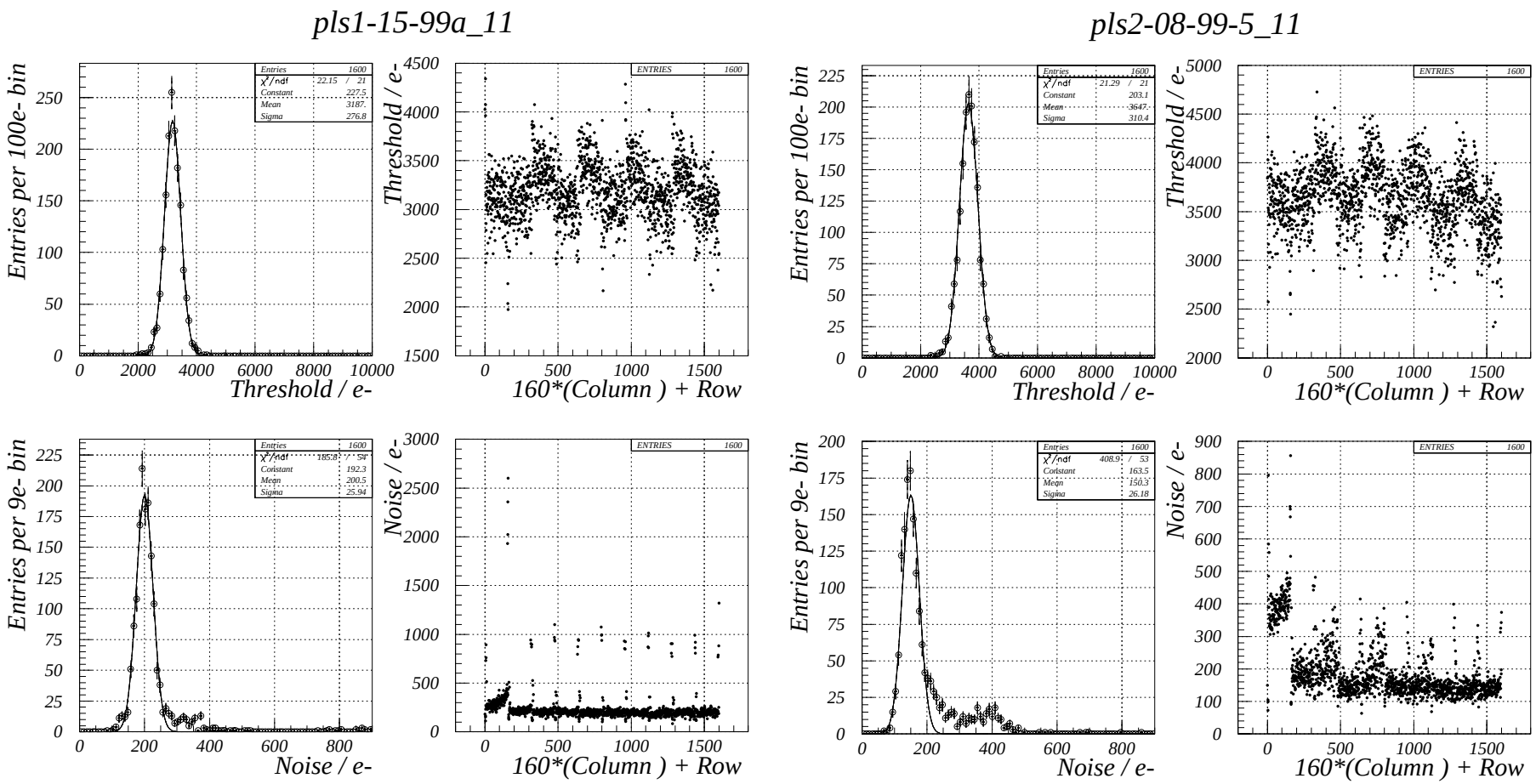
- Module was a 2M Tile 1 module bumped at Boeing. All assembly with Flex and Flex Support was done at UOK. The backside of the chips is electrically isolated from the Aluminum support plate by Kapton tape.
- Twelve chips work reasonably well, other chips have problems of varying severity.
- Small glitch in initial turn-on meant that module might have suffered a high temperature cycle of about 30 minutes, which could possibily explain relatively large number of chips which have problems.
- In this module, high current state observed when all chips operated at 4K threshold at the same time, and addition of 0.1μF instead of standard 0.01μF on LV supplies did not help this problem. This is different than the three LBL modules.
- All studies shown here were carried out by operating only one chip at a time (CINDAC set to 0 for others).

Threshold scans of two chips on the module:



- Some chips show relatively high noise always (500e), others show intermittent behavior of 200e or 500e).

Threshold scan of another chip twice:

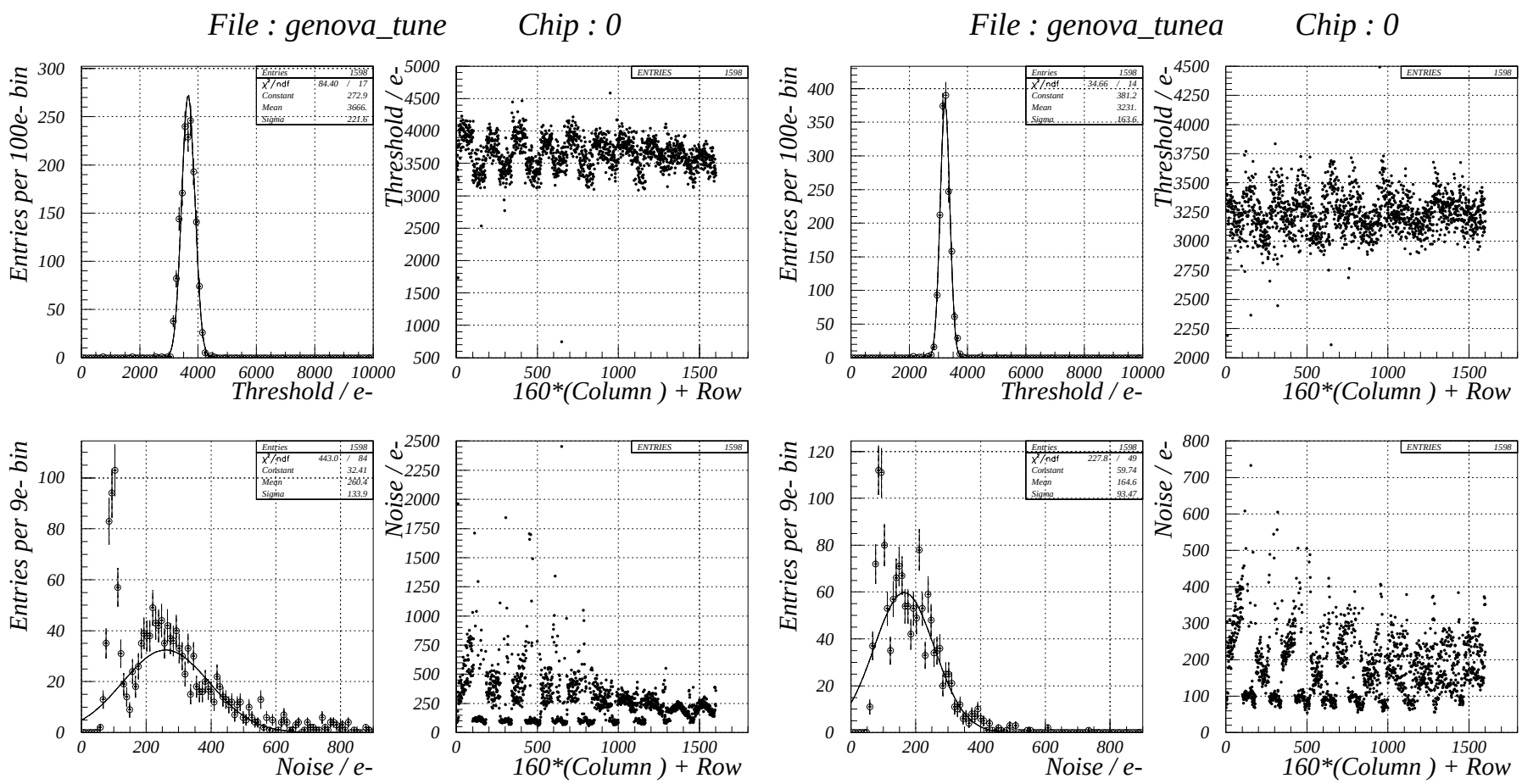


- Many scans of this chip always gave a noise of about 200e.
- Note the anomalous Column 0 noise behavior (expect less than 50% increase for 600μ pixel relative to 400μ pixel).

Single chip studies with different bump-bonding vendors

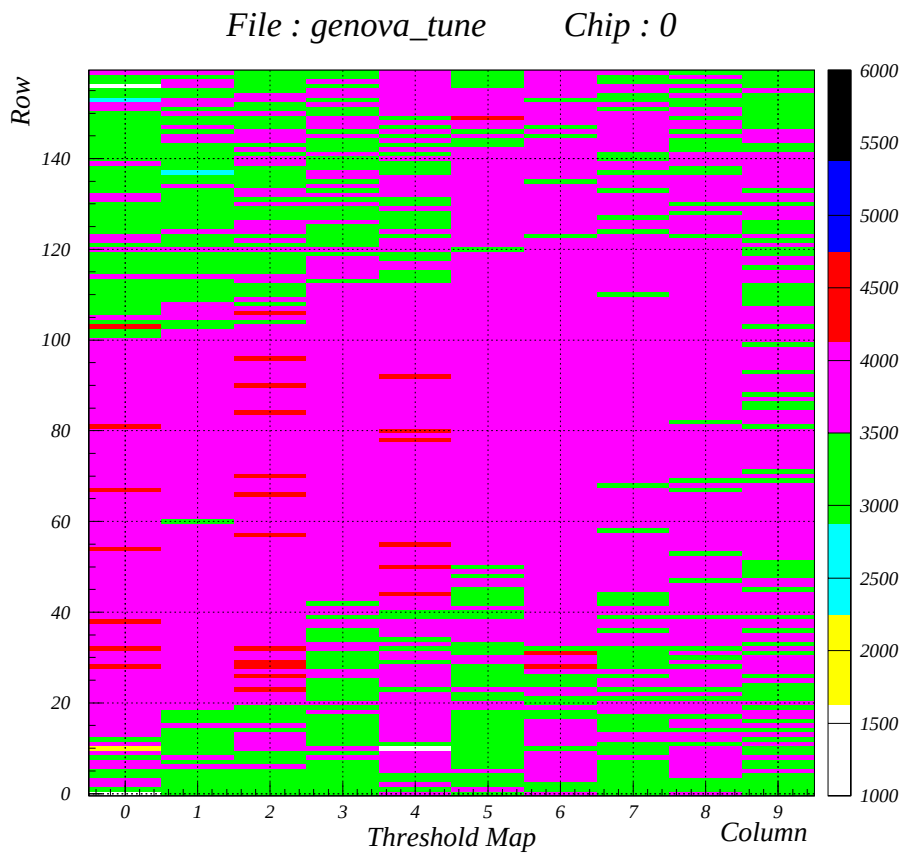
- Genova has sent us one of their Alenia bumped assemblies to study in more detail, to see if we could figure out why the noise performance was so poor. This particular assembly had several problems, including AVCC current of 5 times the nominal value (never seen before), and many unconnected bumps.
- In the Genova assembly, we observe very significant after-pulsing (digital crosstalk) effects whenever more than one pixel is being injected. However, scans in which a single pixel is injected in the chip give very similar noise behavior, which suggests that the excess noise is not related to the after-pulsing. The after-pulsing behavior might be expected given the very short Alenia bumps which will place the electronics die and the sensor very close together (roughly, Alenia is 5μ, Boeing is 10μ, and IZM is 15μ).
- Have compared two identical detectors, one with IZM solder bumps and the other with Boeing Indium bumps. The performance of the Indium bumped assembly was significantly worse, and shows clear evidence of resistive behavior.
- Sorting through our data on structures bumped by these two vendors, it is apparent that all of our good quality assemblies used solder bumps. In particular, there was a group of assemblies which we received in August, three identical ST1, and three identical ST2. All of the six assmblies had identical, and excellent, performance. The Boeing detectors typically show large noise and lack of threshold stability, neither of which are seen in IZM assemblies.

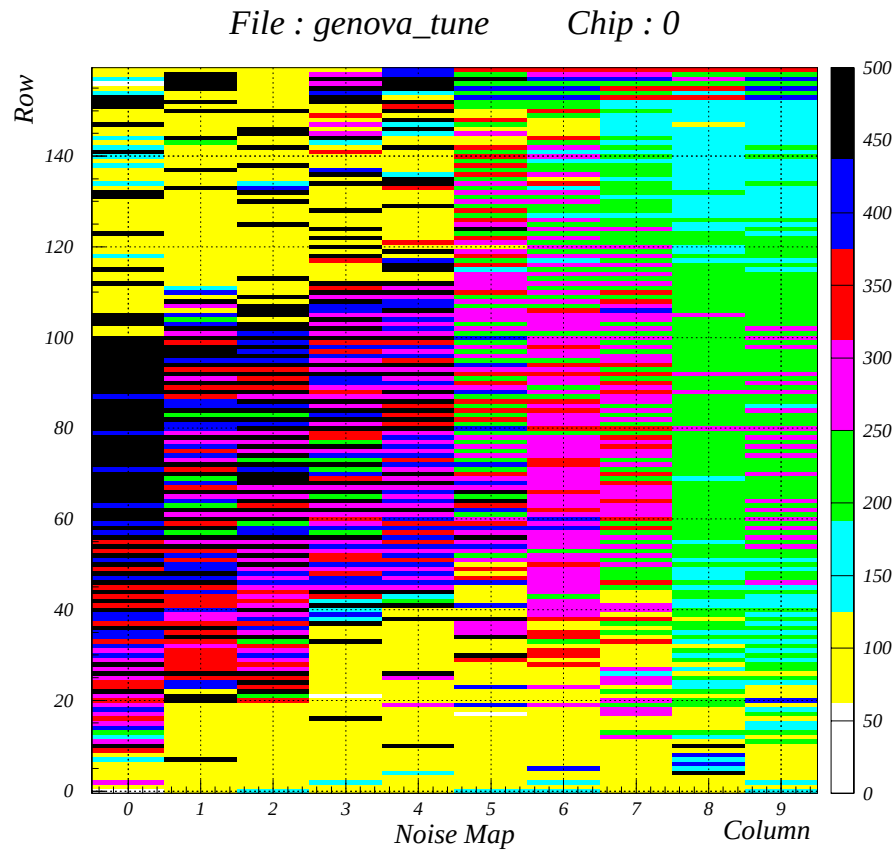
Genova single chip assembly (ST1):



- Do two threshold scans close in time. Observe many unconnected pixels, and behavior of threshold and noise which is not very reproducible from one scan to another. Connected pixels have noise of 200-400e, with best noise seen far away from unconnected pixels.

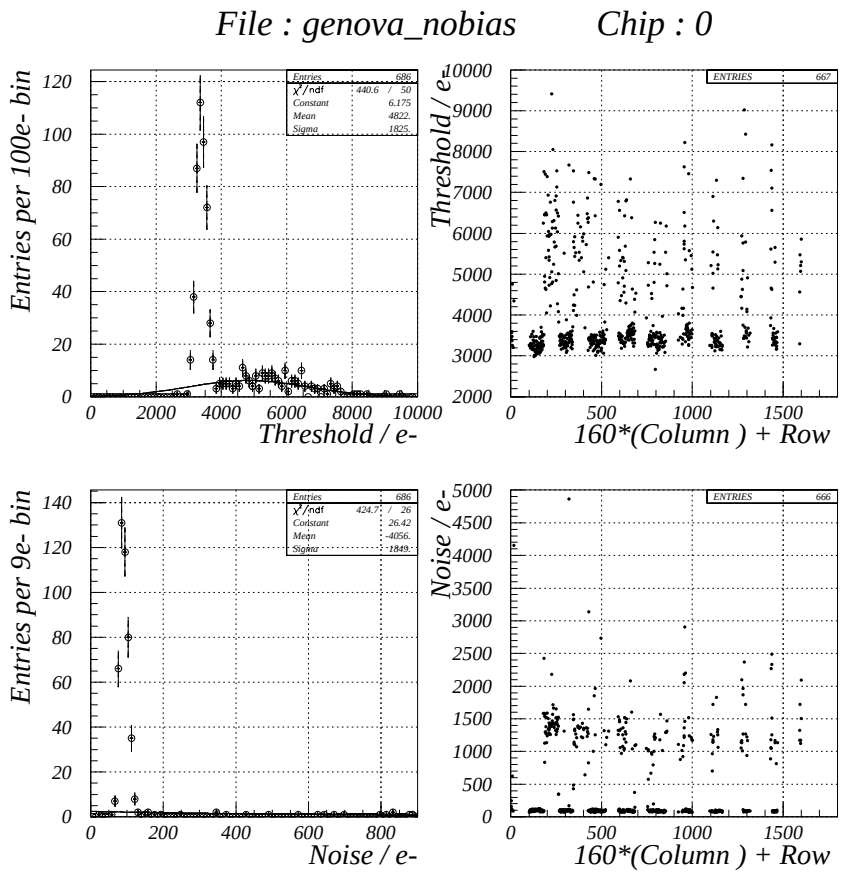
- Pattern of threshold and noise indicates the large regions of unconnected pixels:

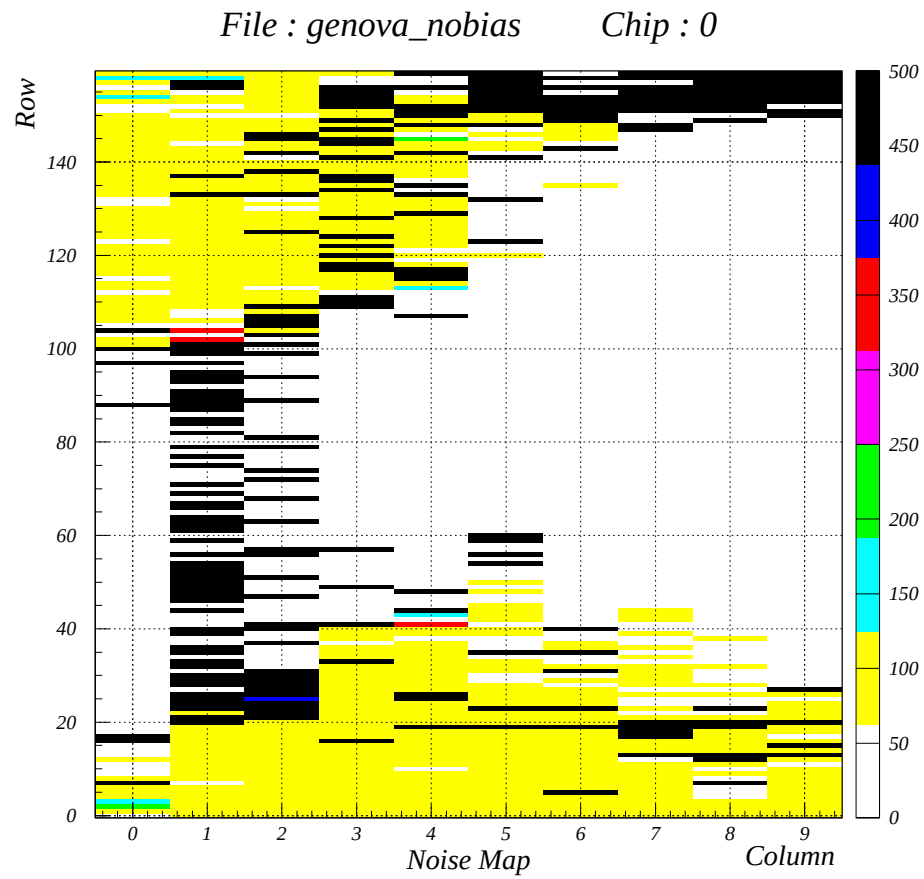




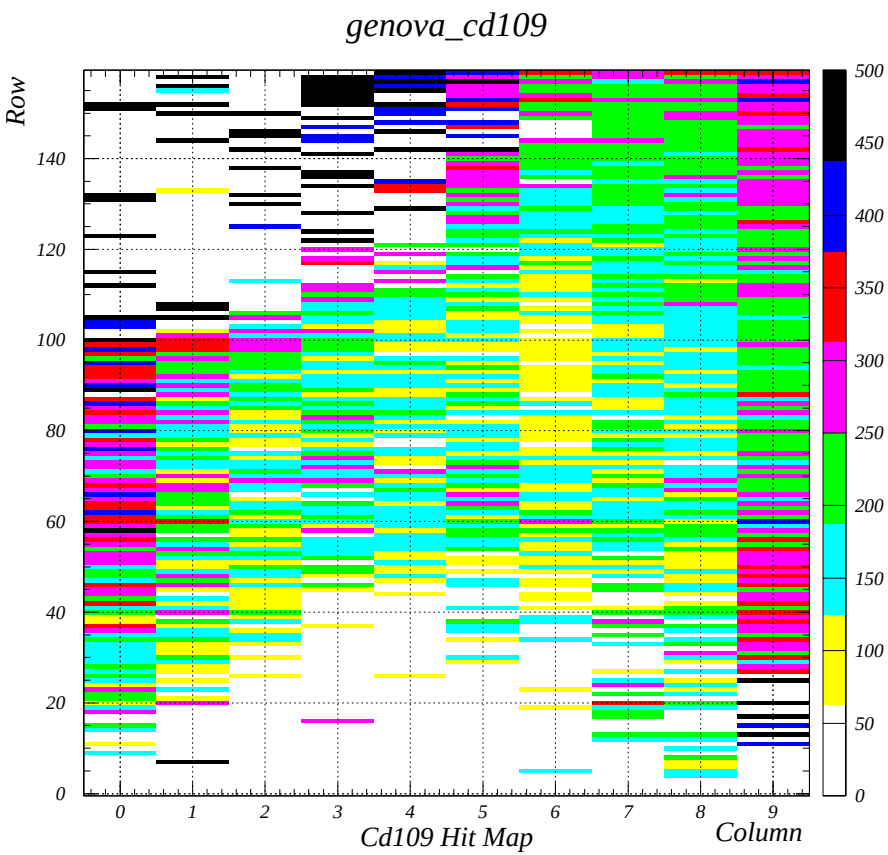
- For a ST1 detector, this will cause lack of depletion near the unconnected pixels, which may lead to large capacitive loads on pixels near this bad region.
- Noise performance in corner of chip (column 8 and 9) is not that much worse than expected (expect about 120e for nice ST1 detector). Unconnected pixels have noise of 80-90e, somewhat more than bare die which have 60-70e.

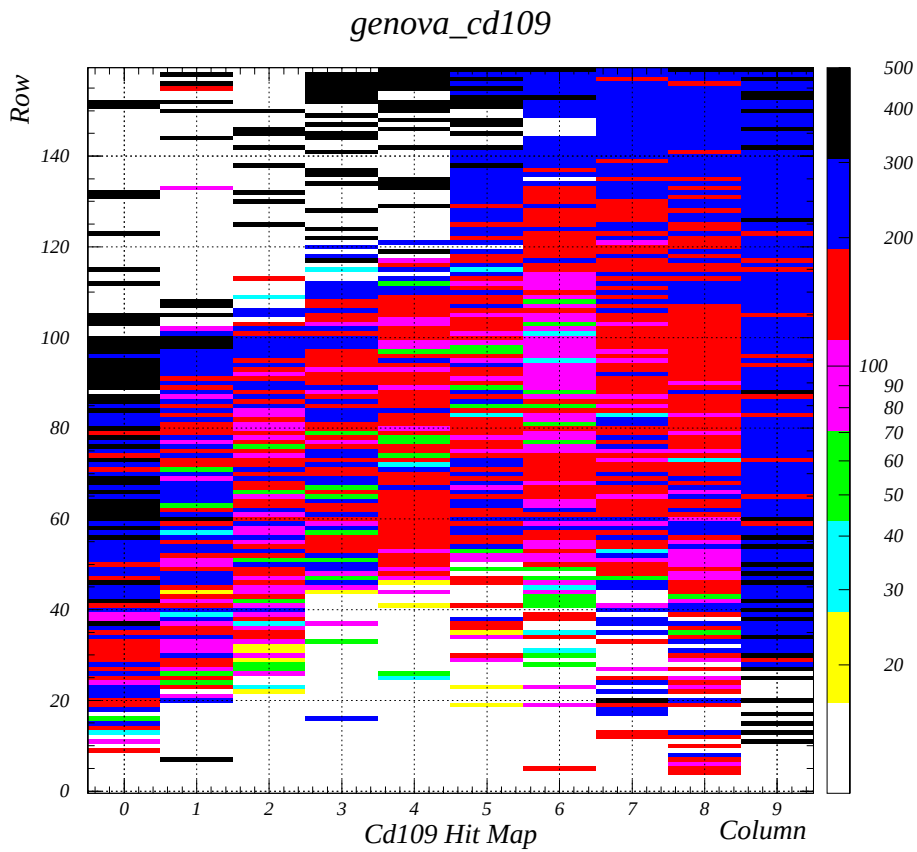
- Threshold scan performed with no HV bias confirms that pixels are really not connected to the detector:





- Source scan shows similar behavior:

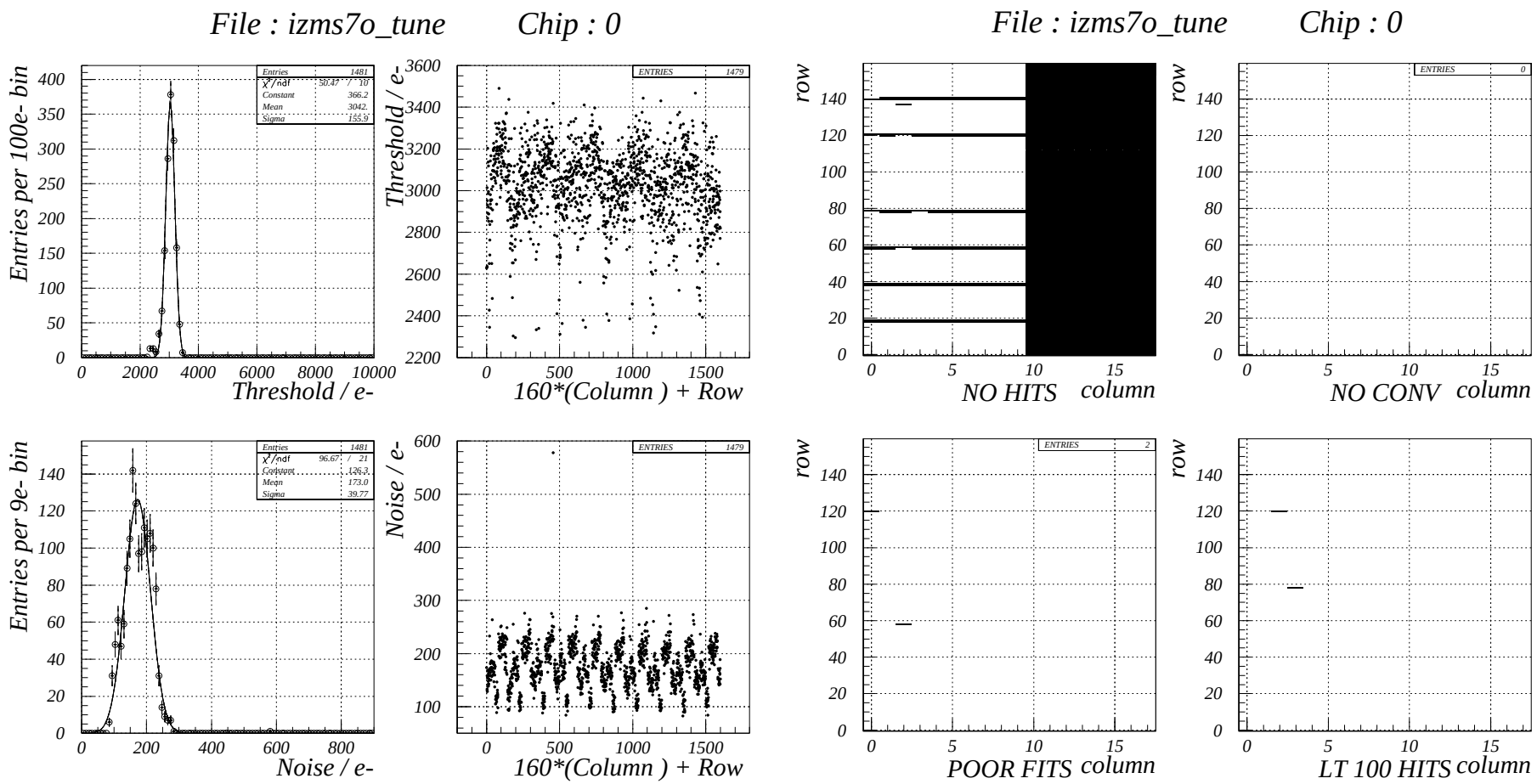




- To summarize: we have no understanding of the anomalous noise behavior observed. Measurements in Genova indicate that bump resistance should not be an issue for Alenia assemblies. However, this device was not typical, and so it is hard to generalize from measuring it. Genova claims that several other assemblies have similar behavior.

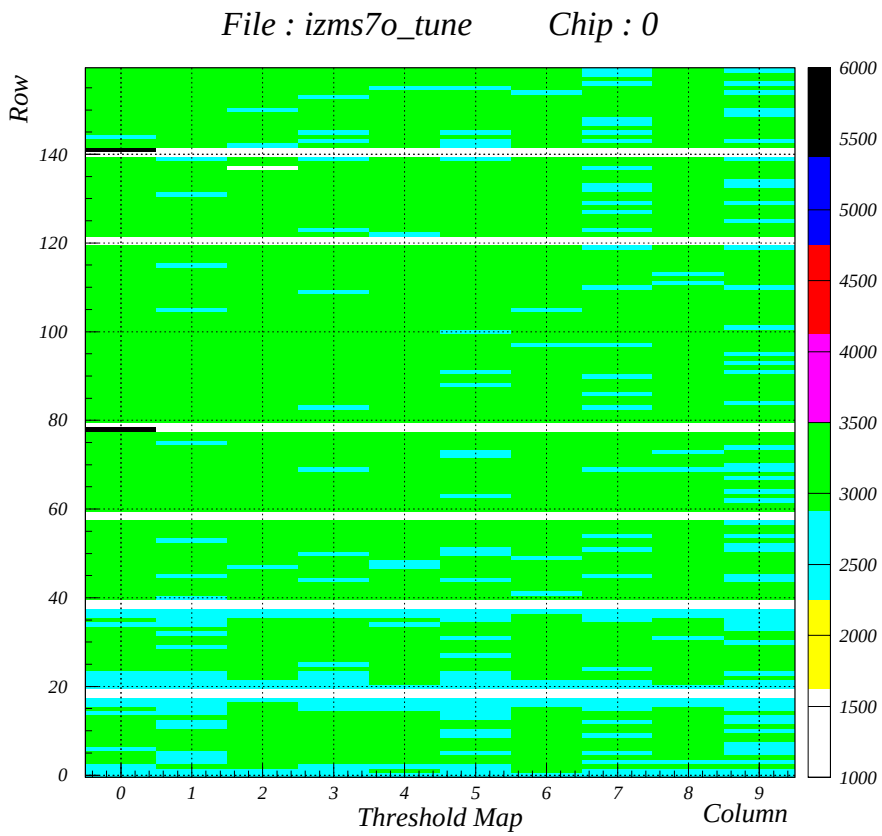
Measurement of IZM and Boeing S7O assemblies:

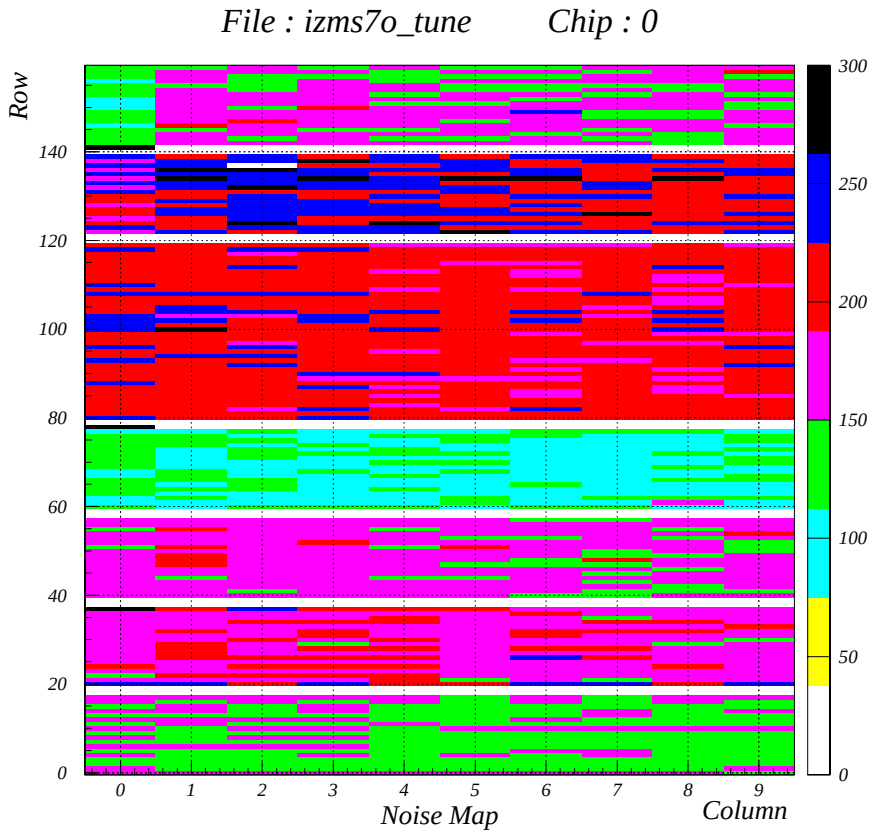
- IZM assembly has good performance, and was tested in H8 in August:



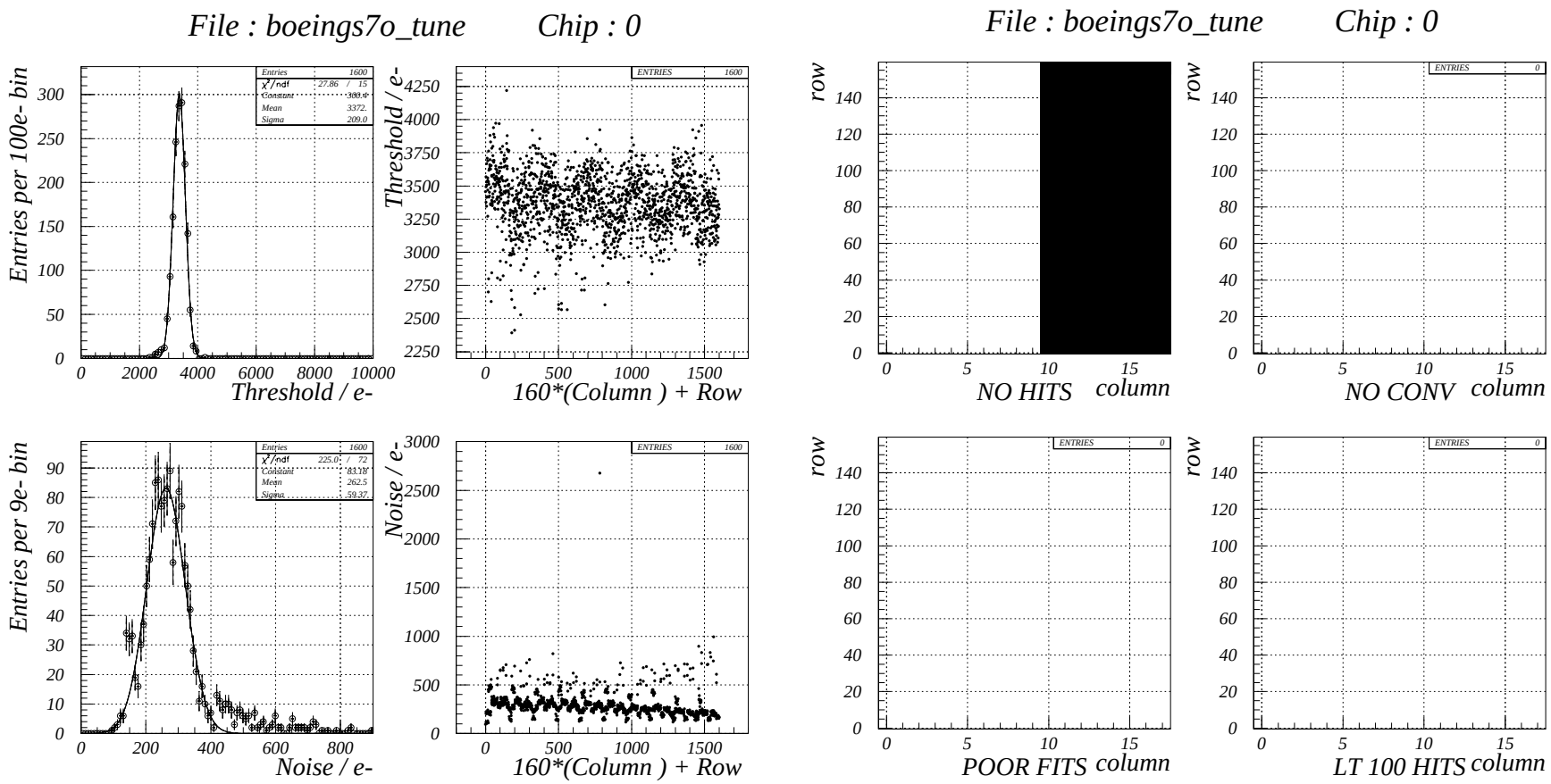
- Regions between each of the seven zones look dead, since those channels are all connected to a common metal guard ring.

- Threshold and noise maps look uniform within each zone, and behavior in the different zones matches that seen in complete single chips (at least for SSG and ST2):



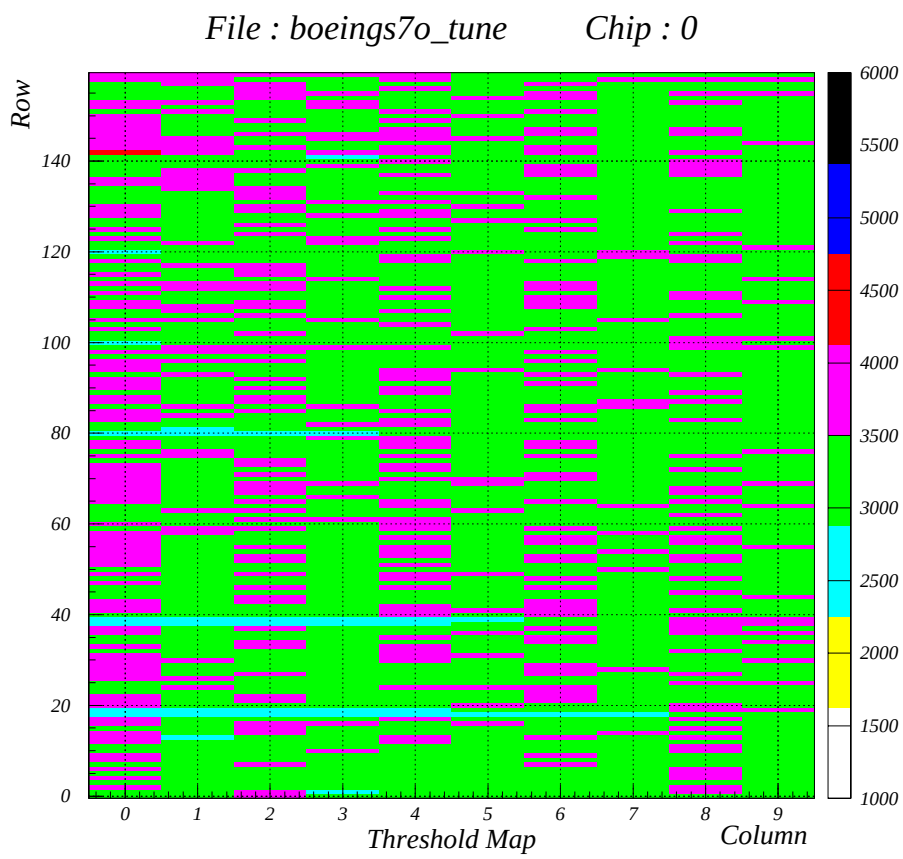


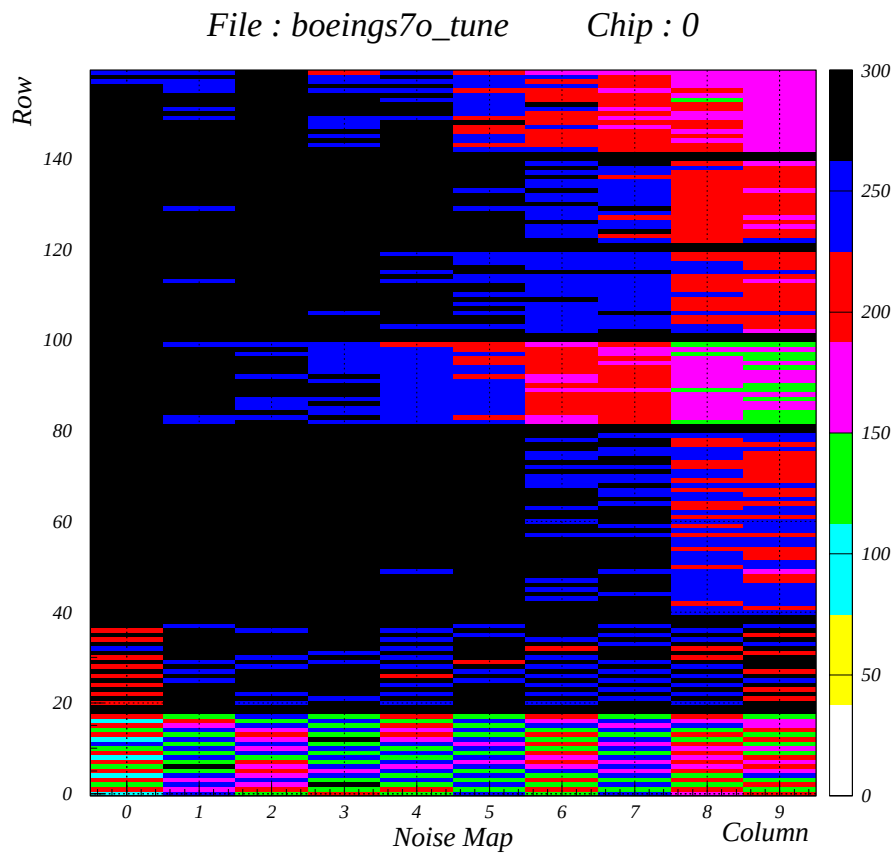
- For Boeing assembly:



- Noise is higher than for IZM assembly
- The regions between zones are not dead, but are only noisier than adjacent channels connected to the detector. For different channels which are connected together to work, the resistance must be large (more than 10 KOhm ?)

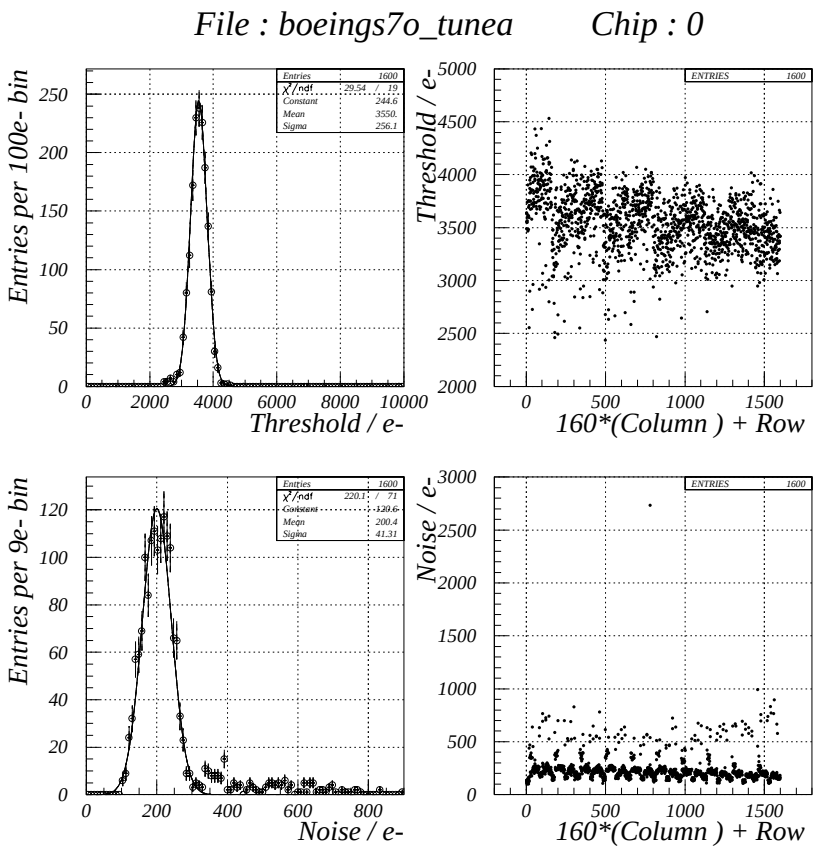
- Threshold and noise maps:

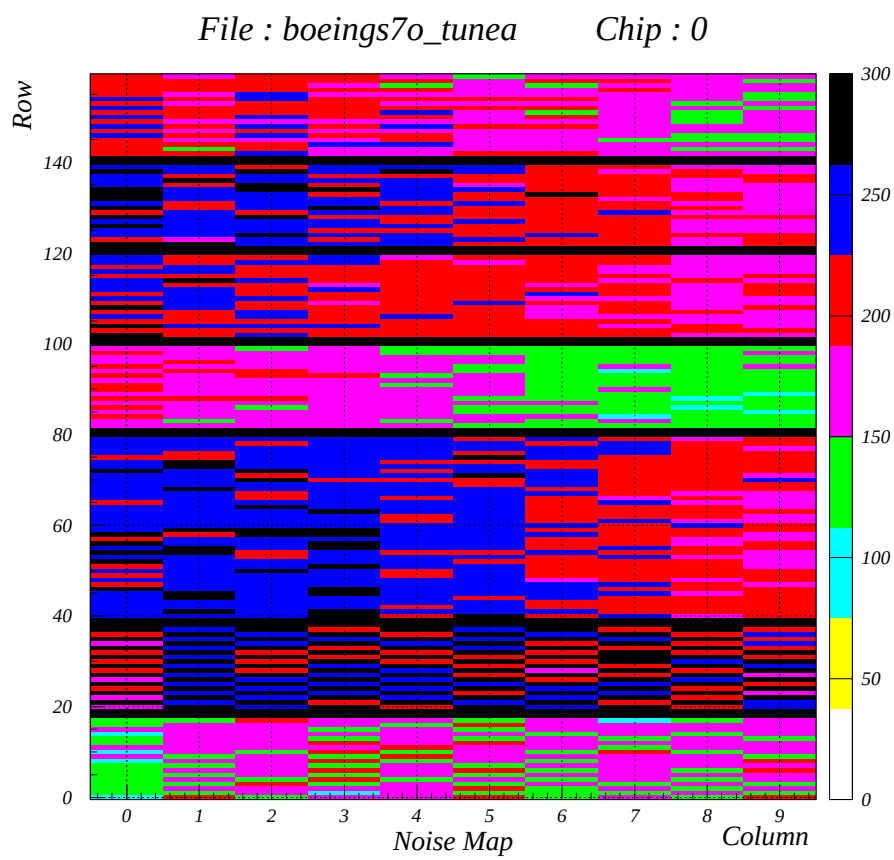




- See significant increase in noise, and it is now not uniform within a given zone of the detector.

- Perform additional threshold scans:





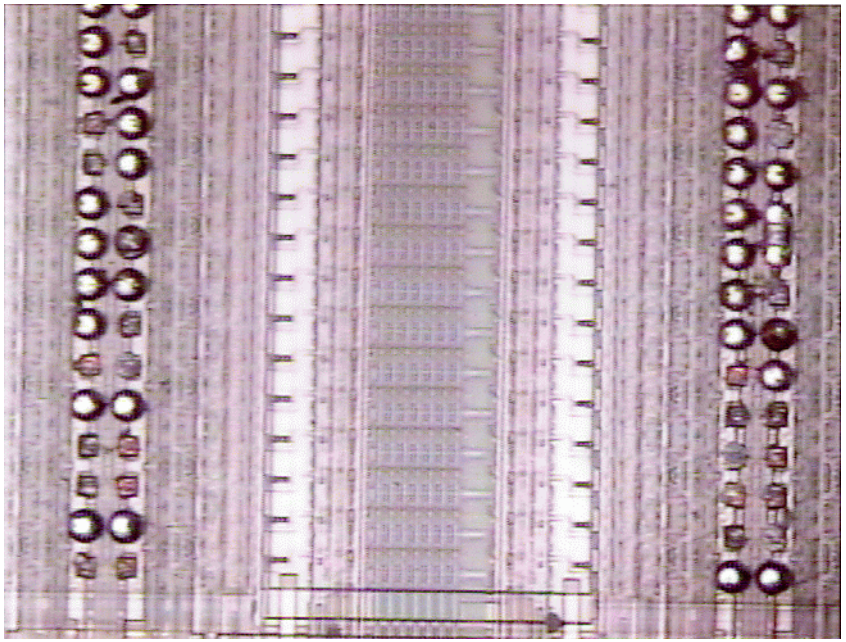
- In this particular scan, the noise is lower and more uniform. Several subsequent scans look more like the first scan (high level of non-uniform noise).

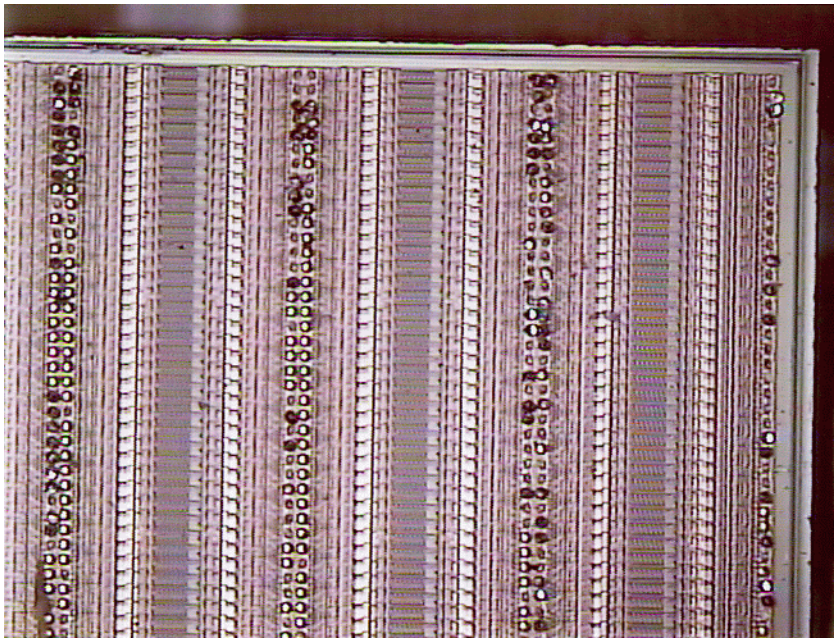
Next steps

- First solder bumped module (Tile1) now being assembled on one of the new “bare” module support cards. This should allow testing of module in “readout all” mode where all channels are active at the same time. This will require further modifications to PixelDAQ to support storage of data from multiple chips at the same time.
- A second solder-bumped module (Tile2) was broken in transit:

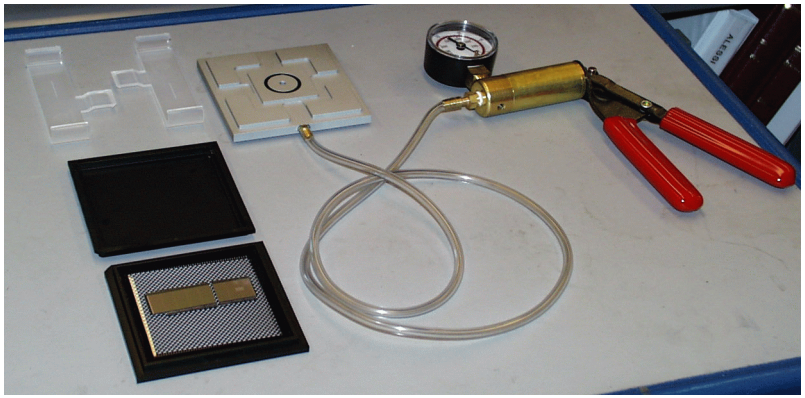
- Clips keeping box closed were broken, and one chip was knocked off the module!

- Looking at solder bumps on chip which fell off indicates bumping looked OK:





- Recommend that we ALWAYS use GelPaks for transporting modules:



- Fail-safe technology requires vacuum to release.
- Standard 4” packs are a good match to our module size.

- Now exists one MCM-D module that seems to work very well. We would like a chance to test this in Berkeley once Peter Gerlach is ready to loan it out for a few weeks.
- Awaiting single chips and modules build with back-side plated FE-B wafers (both Alenia and IZM have such a wafer) to see if making a good quality substrate contact can improve the noise behavior of the modules
- Also waiting to get assemblies using new Prototype 1.5 sensors. We should try very hard to have a reasonable selection of such assemblies (single chips, and possibly also modules) tested and ready for the May H8 testbeam.
- At least some of the modules above, operated in full MCC mode, should be studied in the May H8 run. We will soon begin working on the necessary DAQ upgrades for this. The Tile1 “bare” module has problems operating in “readout all” mode, and so is not useful. The Tile2 “bare” module has many bumping problems, but might be suitable for testing on one side. The Flex module also has trouble operating with all of the chips simultaneously biassed. Hopefully, next few modules made will have better performance...