LVL1 Latency for Pixel Electronics

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Summarize the present state of knowledge

LVL1 Latency from Trigger Group

- L1 Trigger Group has a clear definition of their contributions to the latency, but one has to read between the lines somewhat to see how to apply this for the Inner Detector systems since they do not use the standard TTC system...
- Basic L1 contribution is defined as time from collision in center of detector until time that L1A appears at the output of the TTCrx chip in the subsystem clock distribution system.
- This is 100 crossings, including 20 crossings of contingency, for the standard TTC system. This assumes that the standard TTC system is used, in which a short direct path is used to go from the CTP/TTC in USA15 to the sub-system TTCrx which is assumed to be located in the cavern (80m), and from which trigger signals are assumed to be re-distributed by optical fanout to local on-detector electronics.
- This calculation is modified for the pixel system by assuming only 40m of fiber from CTP to TTCrx (since the TTCrx is in USA15 instead of in the cavern). The speed of the fiber has been measured to be 5ns/m, so this gives 92 crossings.

TTC Distribution within Pixel System

- Many of these numbers are based on estimates from present prototypes. As such they are fairly realistic, albeit perhaps not very optimal.
- Once the L1A gets to the ROD crate, it enters a TIM (Trigger Interface Module), and is then distributed on the ROD crate backplane to the RODs. This is estimated to require 2-3 crossings.
- The ROD must then receive the L1A, encode it as a 3-bit serial message, and send it out through the BOC (back of crate card) which contains the opto-interfaces. This is estimated to require 5-6 crossings, including the 3 crossings for the message (this is the time until the end of the last bit in the message is sent from the BOC).
- The L1A must then be encoded by the BPM (bi-phase mark) chip on the BOC, sent down the fiber link to the detector, and decoded on the DORIC chip. These two chips are presently claimed to require 5 crossings to do this job, 4 for BPM and 1 for DORIC.
- The L1A message must then propagate through the MCC. This is estimated to take 2 crossings from the end of the last bit received.

- Finally, the L1A must be sent to the FE chips, and must generate the internal trigger coincidence. This is estimated to take 1 crossing. The propagation delay through the front-ends (preamp plus discriminator) has been ignored here, and could give up to -1 crossing of latency.
- The pixel system TTC distribution itemized here gives a total delay of 16 crossings. Areas where improvement might be possible include optimized distribution of timing from TIM to ROD, and improved handling of encoding in the BPM. This could save perhaps as much as 5 crossings, but would require substantial design work.

Fiber run to detector

- The additional fiber run from the ROD crates in USA15 to the detector is estimated to require 115m worst case. The worst case routing from the detector is for cables which exit in the horizontal plane away from USA15, route down around the outside of the muon system, and up into the center of USA15. This gives 23 crossings, but is clearly a very poor routing path for time-critical signals.

Total L1 latency

- The total of these delays gives an estimated latency of 131 crossings, including the trigger group contingency of 20 crossings.

Contingencies

Trigger

- The Trigger group contingency of 500ns includes possibilities that the time to get signals from the muon and calorimeter trigger subsystems could increase, the fiber routing assumed may not be realized in the final installation, and the trigger algorithms and electronics may not achieve the processing times estimated. They insist that they want to retain all of this latency to insure that the experiment will work.

Fiber run in USA15 (CTP->ROD):

- There is the 40m cable route from the CTP/TTC to the Pixel sub-system TTCrx, and then to the ROD crates themselves. This exact value will depend on our location in USA15. The trigger sub-system occupies the front rows of racks on both floors of USA15, but cannot yet specify the location of the CTP. There are no other official assignments of racks within USA15, and so at this time, we cannot assume a shorter fiber run than this. However, it is likely that this distance will shrink by 10-20m

Fiber run from USA15 to PPB1 (ROD-> detector):

- There is the 115m cable route from the ROD crates to the detector. This assumes that there is no special routing of the fiber bundles, and the worst case routing goes away from USA15 out to the muon radius, and then back again. Many options exist for improving this, including routing around the detector at smaller radius, and possibly even routing all fibers around between the ID and the LAr cryostat. These routes could save 20m-30m, but would route the fibers separately from the LV supply cables and the cooling piping, which is constrained by shear volume to be distributed equally around the detector in phi. Further investigations are proceeding.
- Note that given the optimal location of the trigger racks in USA15, we pay twice in routing: once to go away from the trigger racks to our ROD crates, and once to go back to the detector again. In addition, we pay for not routing our timing cables on the shortest possible path from the detector.

Pixel TTC distribution:

- In the pixel electronics contributions to the latency, no contingency was assumed, although it could be argued that one can improve on some of the present values by more careful design. This is potentially risky, because these values could get worse also.

Summary:

- I would argue that the only pixel contingency in the above calculations is in the run from the ROD crates to the detector, where we could perhaps save up to 40m (8 crossings) by routing our cables in a more optimal manner, with some increase in service installation difficulties.
- In order to gain further contingency, and minimize the final latency, it is important that the TIM+ROD delay be minimized, and that the BPM/DORIC delay be minimized. Close engineering attention in these areas is still needed.
- It is very important to begin the layout of USA15, and work to optimize the fiber routing paths from the ID to USA15.
- I would argue strongly against modifying the FE chips to operate at latencies in excess of 128 crossings (the next step is 256 with the present chips). This would require increasing many internal data paths from 7-bit to 8-bit, and would make fitting into a 400μ pixel in DMILL very difficult. In addition, it is in our interests to minimize the electronics occupancy which is related directly to the L1 latency.
- Note that it is possible to operate the present FE chips at slightly above 128 crossings latency by using the fact that there is a minimum time to get data from pixels and into the EOC. Hence, we could probably set a very short latency (3 crossings) and let the 7-bit counters wrap around with no loss in efficiency.