

Services Issues for Next Prototypes

K. Einsweiler, LBNL

Proposal for FE-I Pinout:

- Update list of pins, and tentative proposal for pin assignments needed to begin Flex3 layout.

Proposal for Flex3 Schematic:

- What changes are needed from Flex2 schematic ?

Proposal for updated list of service connections to Flex:

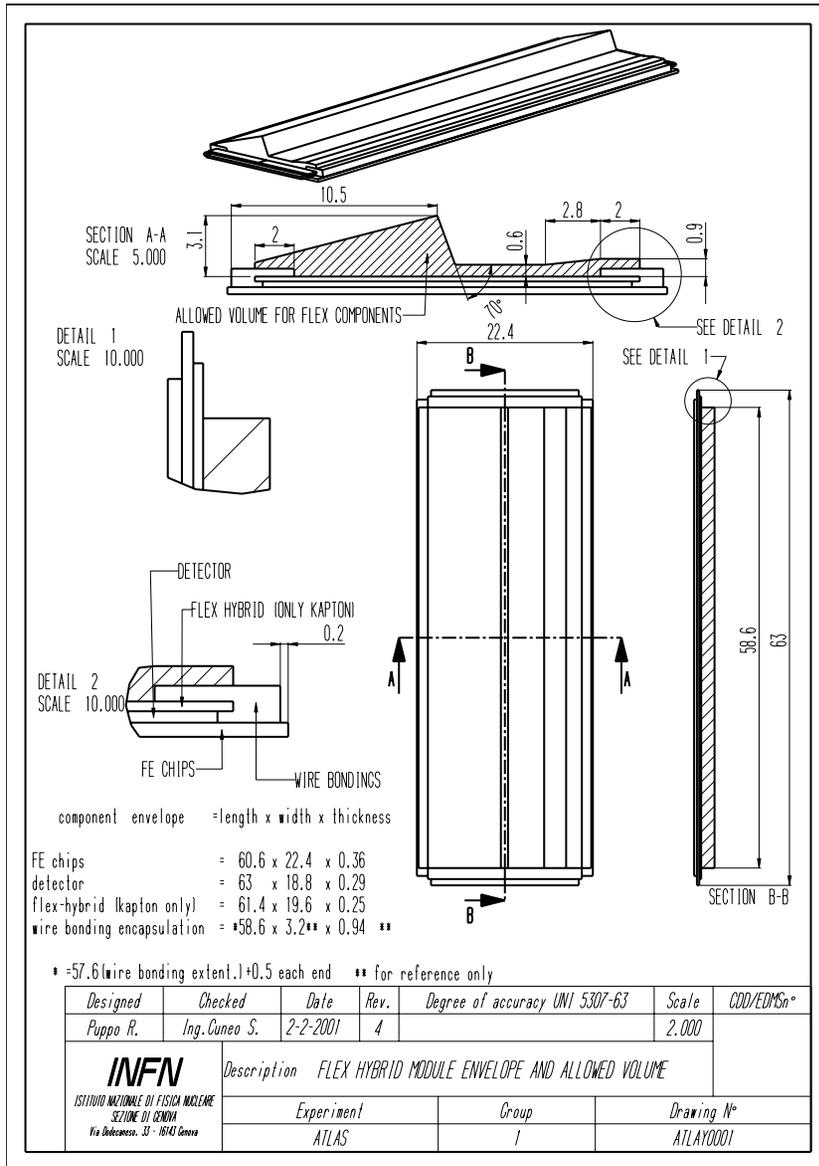
- New list of connections, including propagation of sensing capability down to Flex3 connection.

Proposal for modifying Type 1 cable plant for new connections:

- Present layout makes it difficult to add connectivity for sensing. Propose alternative handling of HV lines to resolve this.

Overview of Module Envelope Constraints

Summarize constraints on module envelope:



Constraints on FE die size:

- Present prototypes use:
7.2x(8.0+2.8)mm design size
with 0.1mm dicing zone all around:
7.4x11.0mm as-cut die size.
- Production size agreed to be same:
Provides total chip envelope in z of
 $8 \times 7.4 + 7 \times 0.2 = 60.6\text{mm}$

Constraints on FE bonding region:

- End chips have a constraint on the region which may be wire-bonded, in order to provide good Z overlap. Bonds must fit in central 57.6mm of module, meaning central 4.4mm out of the 7.4mm as-cut die width.
- If we retain the present 150μ bond-pad spacing, that corresponds to 30 bonding pads (4.35mm + pad size).

Proposed Final FE Chip Pinout (30 bonded pads):

- Total of 10 power pins, positioned at 1/4 and 3/4 points in die (mirrored) :
 - p11, p38 VDDA
 - p12, p37 AGnd
 - p13, p36 Shield
 - p14, p35 DGnd
 - p15, p34 DVdd
- Total of 1 analog pin (intended largely for lab calibration at this time):
 - p20 VCal
- Total of 9 Command and Address pins (GA closer to DGnd):
 - p16 - p19 GA0 - GA3
 - p21 CCK
 - p22 DI
 - p23 LD
 - p32, p33 STRn, STRp
- Total of 6 control pins (all LVDS pins are grouped together):
 - p26, p27 SYNCn, SYNCp
 - p28, p29 XCKn, XCKp
 - p30, p31 LV1n, LV1p
- Total of 2 output pins (now located in chip center for easier Flex routing)
 - p24, p25 DOn, DOp
- Total of 2 detector pins:
 - p10 DGuard
 - p39 DGrid

To reach this, have removed 18 pads from present pinout:

- RSTb, and Analog pins (I1-I8, and VCCD/VTH)
- All monitoring pins (MonHit, MonSel, MonRef, MonAmp)
- Propose to retain most on the die, in locations compatible with present floorplans:
- Total of 1 control pin:

p40 RSTb

- Total of 11 current monitor pins (may not all be used):

p1 I1

p2 I2

p3 I3

p4 I4

p5 I5

p6 I6

p7 I7

p8 I8

p9 I9

p41 I10

p42 I11

- Total of 6 special monitoring pins:

p43, p44 MonHitn, MonHitp

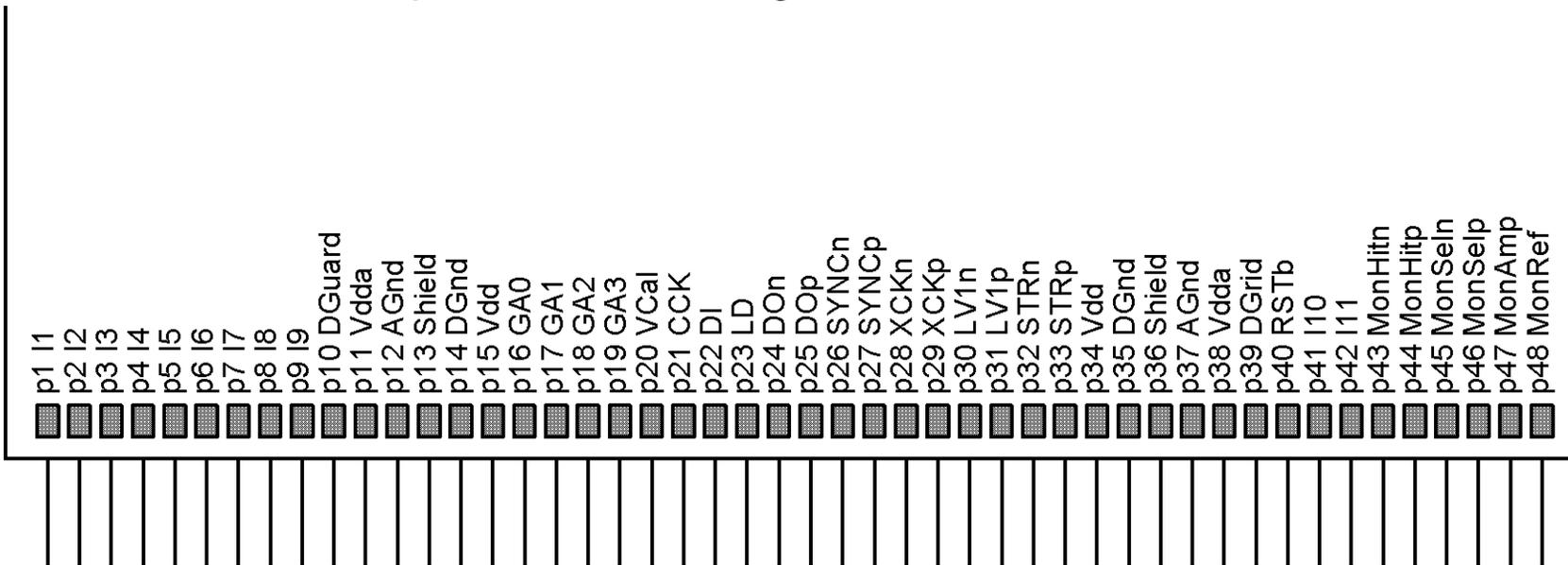
p45, p46 MonSeln, MonSelp

p47 MonAmp

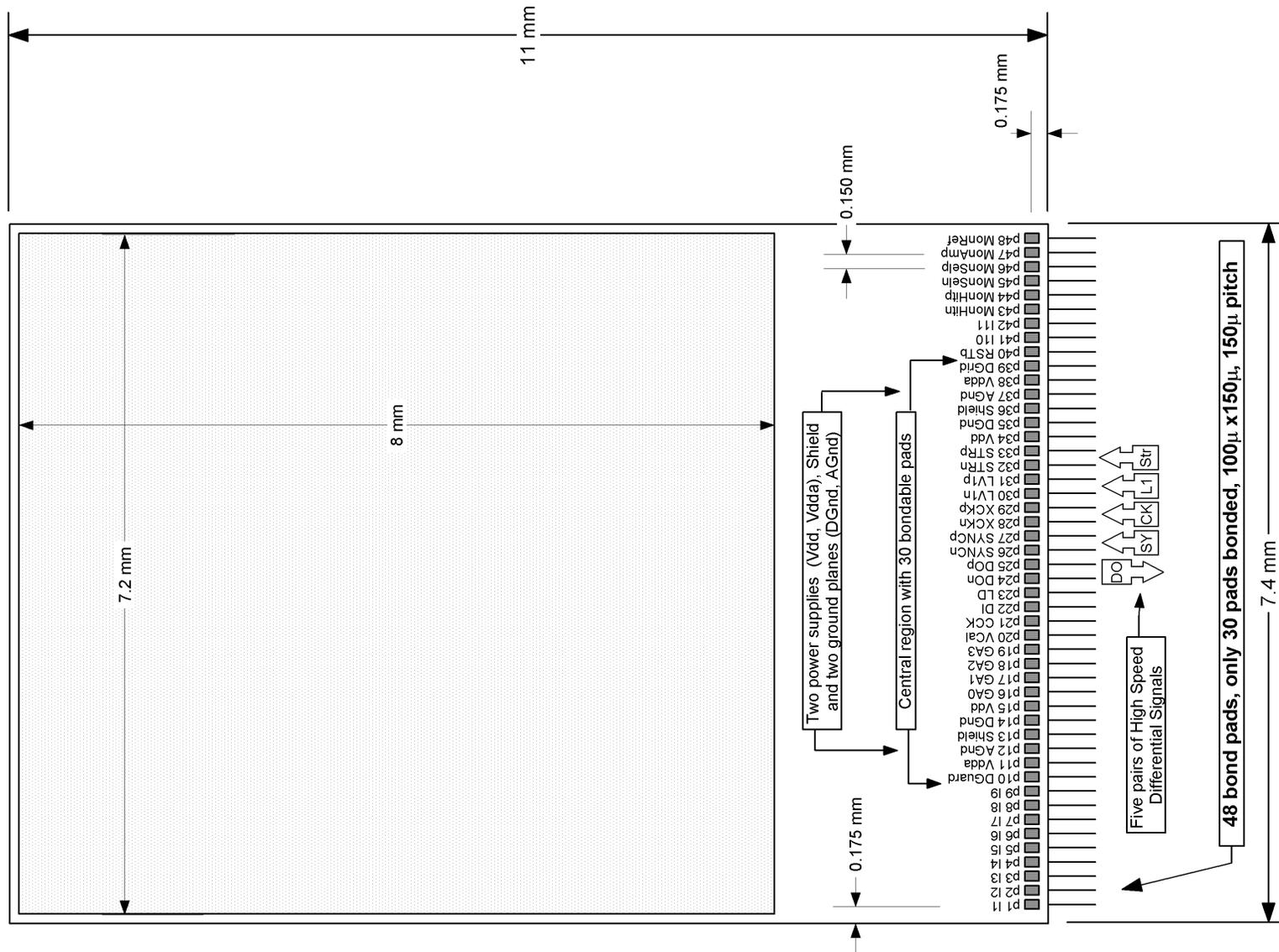
p48 MonRef

Proposed Pad Geometry:

- Increase present pad size to $100\mu \times 150\mu$ rectangle, with 150μ pitch, to provide more pad area for rebonding. Include MCM-D bump-bondable I/O pads with the same geometry used in FE-D (relative to the bottom of the wire bond pads).
- Continue to locate pads close to the lower die edge, as for demonstrator chips.
- The present demonstrator geometry has 48 pads, with centers along a line 175μ above the bottom (referenced to the as-cut die size of $7.4 \times 11.0\text{mm}$). The first pad center is also 175μ from the vertical edge referenced to the as-cut die size.
- Propose that this pad placement would be retained, and only the central 30 pads would be used for production bonding:



Overall Chip Geometry:



Further modifications that could be considered:

- Could reduce pads further by reducing to single power connections. This is probably possible given the internal voltage drops achievable in the 0.25μ processes, but reduces redundancy. This would require power pads to be located in the center of the chip. The redundant bond connections seem particularly important for the digital supply to avoid a single missing wire-bond killing a whole module.
- Could further reduce the extra pads by MUXing many current DACs through a single monitoring pin.
- In order to make an appreciable gain in pad pitch as far as the Flex technology is concerned, would need to go to 200μ pitch. This would reduce the number of bondable pads from 30 to 23, which is difficult to achieve in this pinout. Eliminating one set of power connections completely, plus VCal, is only six pins.

First Information on Power Budget for FE-I/MCC-I

- For new FE-I front-end, it looks like the front-end design will need a typical current of about $21\mu\text{A}$, with perhaps a worst case of $28\mu\text{A}$, per pixel. This translates to about 970mA typical VDDA current, 1290mA VDDA worst-case current. The previous budget included ($10\mu\text{A}$ VCCA + $8\mu\text{A}$ VDDA) typical and ($15\mu\text{A}$ VCCA + $12\mu\text{A}$ VDDA) worst-case. Hence, the new single supply has roughly the sum of the previous two analog supply currents.
- For FE-I digital supply, it is too early to have any real numbers, but the previous budget was $25\text{mA}/\text{chip}$ typical and $40\text{mA}/\text{chip}$ worst case. We believe we can remain within these figures, but this depends on the power consumption of some of the improved synchronous logic blocks. We are working to reduce the power consumption of the standard cell DFF below its present level. The typical number may increase slightly, so propose 30mA typical.
- For MCC-I, it is again too early to say. The MCC-AMS uses about 70mA typical, and the MCC-D2 uses about 100mA typical. The previous budget was 100mA typical and 160mA worst-case.

For now, propose the following:

- VDDA (per module): typical 1.0A , worst-case 1.3A
- VDD (per module): typical 0.6A , worst-case 0.8A

Flex3 Schematic

Discuss changes needed relative to Flex2 schematic:

FE-I pinout changes:

- Concentrate all bondable pads in center 30 pads of the die.
- Enlarge pad length to 150μ (pads are $100\mu \times 150\mu$ on 150μ pitch).
- Retain power-pin pairs, but eliminate one analog supply (VCCA) and replace the pins by Shield, which is presently intended to be bonded to DGnd.

MCC-I pinout changes:

- Finalize DTO2 location and connect it to pigtail. Do we want to support this connection on all modules, or only B-layer modules? Propose to do so on all modules, as first modules may go to B-layer (depending on schedule), and it provides extra flexibility later.
- Leave Transparent mode pins on production MCC ? Provide access to them at some level for testing purposes ? This was not intended, but it is possible to leave the present “legacy” pads in place on Flex3 if there is space and adequate justification. Note: Flex2 schematic is missing connection for TMbar (should be pulled high for safe operation, or input pad takes care of this ?). Further note: backwards compatibility with MCC-AMS requires inclusion of STRn/p onto Test Connector.

- Presently, isolate external HV input and return from Flex with 10K series resistors (schematic says 100K, but this is too large). Detailed measurements are required to see whether the return to the HV supply needs a lower impedance. Meanwhile, propose to keep the pads for the resistor.
- Connect HV_return, AGnd and DGnd together on module with jumper 0402 parts (schematics says 100Ω, but this does not make sense). Leave present flexibility for commoning connections in place, or hardwire some connections and eliminate the 0Ω resistors ? It is hard to believe this commoning connection is not critical, but pads do provide extra flexibility for now, so try to keep them ?
- Presently, all fast signals driven from MCC to FE (XCK, STR, LVL1, SYNC) are back-terminated at MCC with 100Ω termination. Do we want to leave these external, or move them inside the MCC ? Prefer flexibility of external resistors.
- Presently, connection from MCC to opto-daughter (XCK, DCI, DTO, DTO2) is shown to be terminated with 200Ω at Flex end, and presumably another 200Ω is placed at the opto-daughter end. Would prefer a scheme with only the 100Ω receiver termination (two resistors on Flex for XCK and DCI), but this should be examined in Pigtail electrical simulations. The single termination in 100Ω is appropriate if the connection from driver to receiver is made by a transmission line with 100Ω characteristic impedance. This is desirable, but may not be achievable.

Other Changes:

- Need to decide on correct connection of NTC temperature measurement. Two floating terminals, or locally connected to commoning point ? If there are two dedicated wires for NTC measurements, the local connection to common is a modest constraint. If there is only a single dedicated wire, then strongly prefer separate connections, to avoid coupling of temperature measurement with expected voltage drops in any other ground reference available at PP3 where temperature measurement will most likely be made.

Test Connector changes:

- Do we still have a Test Connector, or is the Pigtail attached to the Flex at an early stage, and all testing uses the Pigtail Connector ?
- Do we retain VCal as a routed signal on the Flex, and connect it to the Test Connector ? This provides a useful cross-check during module testing, but is not required during module operation.

Service Connections:

- **Power (3 pairs):**

- VDD/VDD_Ret, VDDA/VDDA_Ret, VDET/VDET_Ret

- **Sense (2 pairs):**

- Sense_VDD/Sense_VDD_Ret, and Sense_VDDA/Sense_VDDA_Ret

- **Temperature (1 pair):**

- NTC/NTC_Ret

- **Optical (4 pairs):**

- XCK+/-, DCI+/-, DTO+/-, DTO2+/-

- **Test (2 signals):**

- RSTb (referenced to DGnd) and VCal (Vcal does not appear on Pigtail itself)

- **Comments:**

- This list includes separate returns for the NTC, and the two sense lines, as well as DTO2.
- A minimal scheme would eliminate DTO2 (except for B-layer !), and connect the sense returns to the NTC return, saving 4 wires on each Pigtail and 2 wires per module on the Type 1 cable.

Backwards-compatibility with MCC-AMS/MCC-D2

- This is a significant complication, but it can be accommodated.
- Requires a third power supply, because VDD for FE-I will be 2.0V and VDD for MCC will be 3.0V - 4.0V. Recommended approach for the proposed Pigtail connector would be to split the present VDD in two, with one pin for MCC_VDD (typical 100mA, worst-case 160mA), and two pins for FE-VDD (typical 400mA, worst-case 640mA). To retain the grounding scheme, the VDD_Ret should be similarly split.
- In addition, the CMOS lines from MCC to FE will require a “poor-mans level shift”. The lines in question are CCK, DI, LD, RSTb. The diode-connected FET clamps in the FE-I chips will turn on above about 2.5V, drawing a large current for any driver which swings above this voltage.
- A series resistor can be used to limit this current. Assuming this current is about 10mA (do not know the correct number), then worst-case, the resistor should drop $4.0V - 2.5V = 1.5V$ at 10mA, so it should be 150Ω . The most secure method is to diode-clamp the signals with external diodes, using for example three diodes in series to achieve a clamp voltage of about 2.5V. However, the series resistor should be adequate for our application.
- The LVDS interconnections from MCC \leftrightarrow FE should be fine, as the differing DC offsets are well within the common-mode specification of the receivers.

Comments on Sense Wires for High-Current Supplies:

- For power supply lines which carry current, there will be significant voltage drops, certainly at least 2-3V round-trip in our proposed cable plant.
- Ideally, we would like to know/regulate the absolute voltage on a given module to something like +/- 100mV during long-term operation. This particular specification requires further study, and is related to the detailed design, operation, and calibration of the FE electronics.
- For the current-sensing supply control included in the CAEN modules, this requires knowing the cable resistance to about +/-5%. The temperature coefficient for Copper resistance is 0.42%/C. Assuming no other uncertainties, this requires knowing the cable temperature to about +/-10 degrees, particularly in the high-resistance regions of the power cables.
- In addition, we have typically five connectors in the power conductors (one at each patch-panel), whose contact resistance should be negligible, but can evolve with time or fault conditions. This makes current-sensing very challenging.
- Preferred solution would be to run individual sense wires to commoning point on module (basically, the pigtail connection). This wire can be small, imposing very little burden in the cables, e.g., 30 AWG (250 μ , 35 Ω /100m) or 32 AWG (200 μ , 55 Ω /100m).

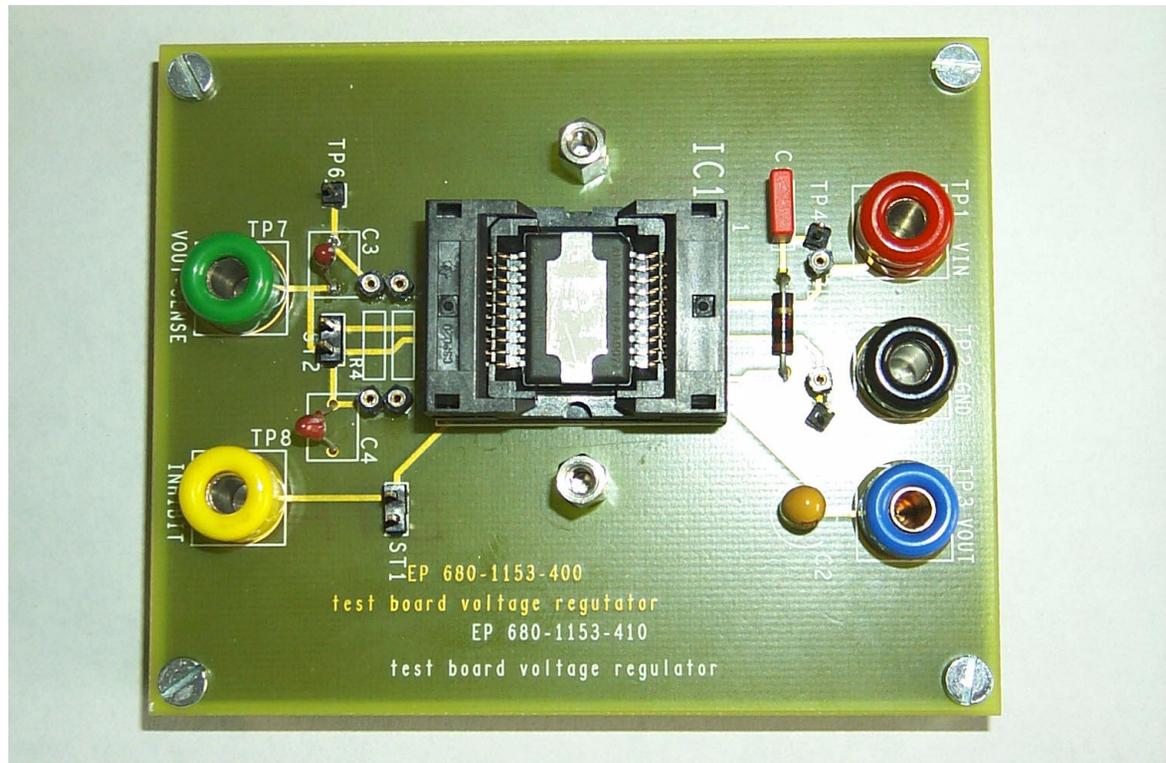
Possible use of Rad-Tol Regulators

- An improved power distribution system could be constructed if linear regulators could be used closer to the pixel modules (7m), instead of relying on passive components alone to filter noise and transients.
- CERN has jointly developed a Rad-Tol LDO (Low Drop Out) regulator in collaboration with ST Microelectronics (LH4913).

Some of the specifications include:

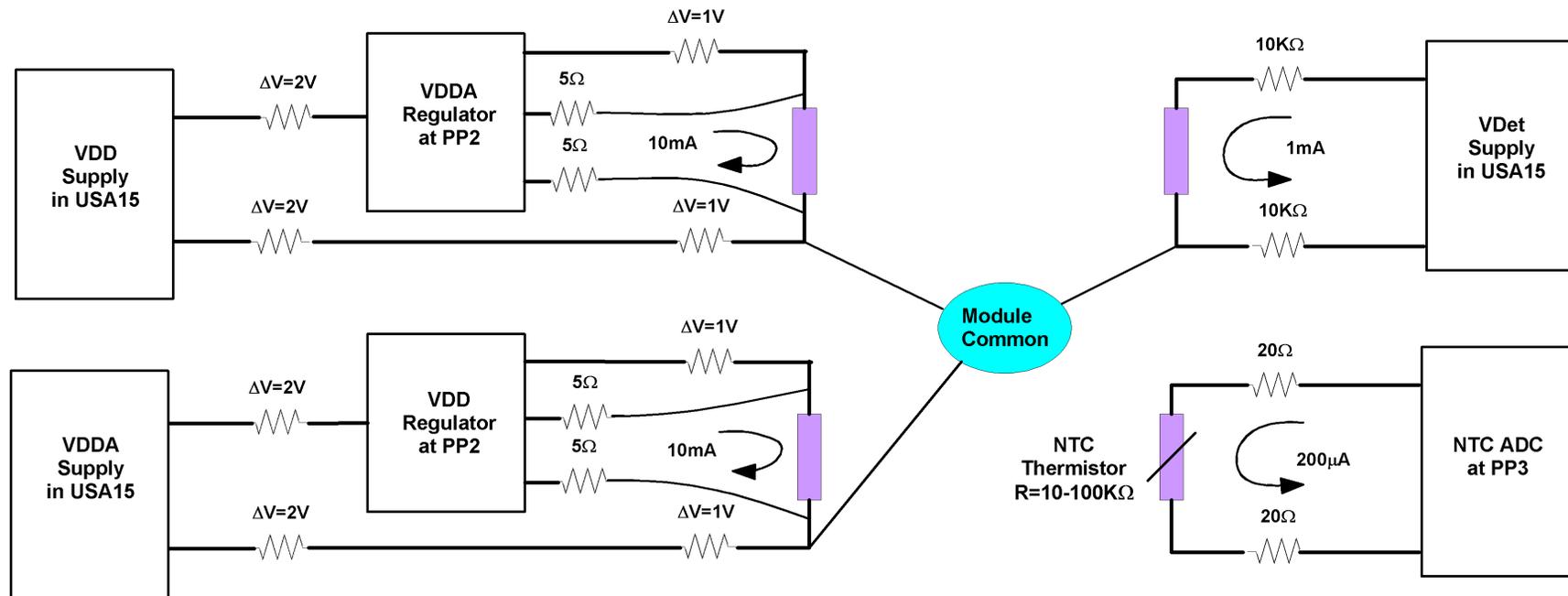
- Radiation tolerance of 500KRad total dose and 2×10^{13} n/cm² neutron fluence. This is achieved by using a high-speed bipolar process from ST which is different from their standard regulator process (high-speed bipolar processes have thinner oxide layers and hence smaller low-dose rate effects).
- Low drop-out voltage of 0.5V for 1A operation (0.65V worst-case).
- Over-temperature, Over-voltage, and adjustable Over-current protection.
- Support of remote sensing, but sense lines do handle some current in this design.
- Part is packaged in special PowerSO20 package.
- First evaluations show design meets specifications, with some minor design flaws which are now being fixed. Production is foreseen to begin late in 2001.
- Cost is modest (about \$25 each in quantity ?)

- Evaluation board is available:



- First irradiations show operation is OK up to 10MRad and $3 \times 10^{14} \pi/\text{cm}^2$.
- For pixels, the total current for a module is about 2A, and a 1V VDO would be needed for safety, so the three regulators/module would dissipate 2W.
- However, my present understanding of the specification for the LH4913 regulator is that it may have up to 1% of the load current flowing in the sense wires, so it would be good to keep the round-trip resistance from PP2 to the module below about 10Ω. For the PP0 prototype, with 3m long, 6mil traces in 1/2 ounce Copper (forgive the units), the trace resistance should be about 20Ω, which is quite high.

Concept for connections to module:

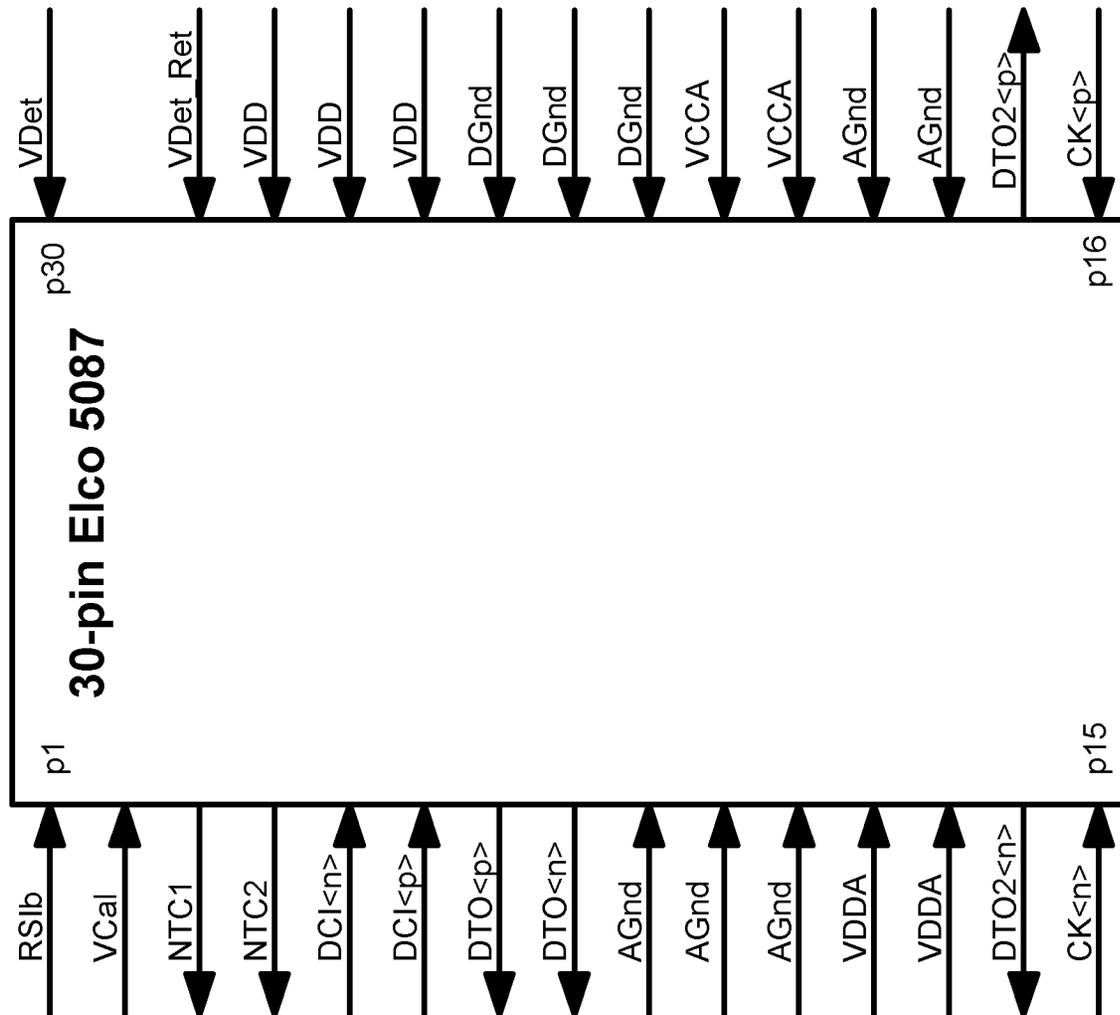


- Ideal situation is to have the Module Common point as the only commoning point for the current flows in the regulator error amplifiers. The NTC ADC (operating in voltage excitation mode with a 2V supply) would be isolated. Both sides of the HV supply are isolated by series resistors (may need to common return line).
- It is claimed that there is significant current flowing in the sense lines (about 1% of load current) used to bias the bipolar error amplifier. In this case, coupling the sense return lines at the module and at the regulator (50mV voltage difference under full-load conditions) will allow current variations in one supply/regulator to couple directly to the sensing network for the other supply/regulator.

- With separate sense return lines, there will be greater isolation between analog and digital supplies. Unfortunately, there are no SPICE models, etc. to simulate and study this, so prototype measurements will be needed. For now, strongly prefer keeping separate sense return lines for the two supplies.
- If the NTC return is also connected to the module common, this should not pose any particular problems. However, the temperature measurement at PP3 will need a ground reference. If this is a power supply return, then one must correct for the large voltage drops (equal to the drop across the thermistor !), and these drops depend on the current being supplied to the module. Using a sense return poses several problems also. First, these lines were intended to end at PP2. Second, if there is indeed something like 10mA flowing in these lines, then they will also suffer voltage drops (which will depend on the module current). Strongly prefer for this critical measurement to be made in such a way that no corrections for currents flowing in other wires are necessary to extract the temperature, particularly since this is a signal used for hardware interlocking as well.

Conductor Count/Pinout for Flex2/Pigtail Connector:

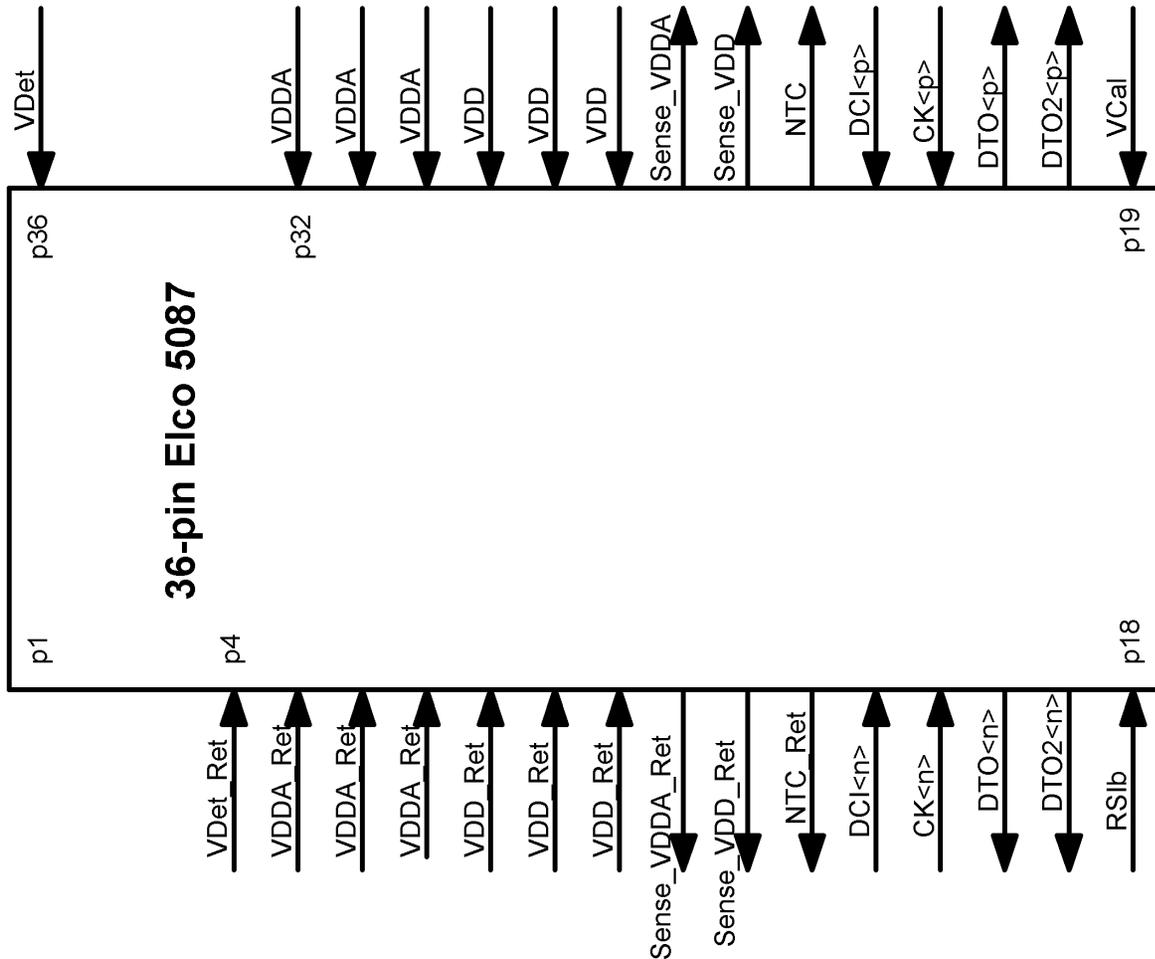
- This diagram is for the Test Connector only. The Pigtail pinout is similar, but not identical, as it is driven by the pad arrangement on Flex2, which is not optimal.
- Present Flex 2.x design is a first pass, based on 30-pin Elco 5087 connector:



- These pin assignments grew out of the layout of the Flex2 hybrid.
- The VCal signal is present only for the test connection, not for the pigtail.
- There is not much room around the VDet connection for 700V stand-off.
- These assignments mix high speed signals and power supplies, making the pigtail layout awkward.

Proposal for Flex3 (assuming double-sided Pigtail):

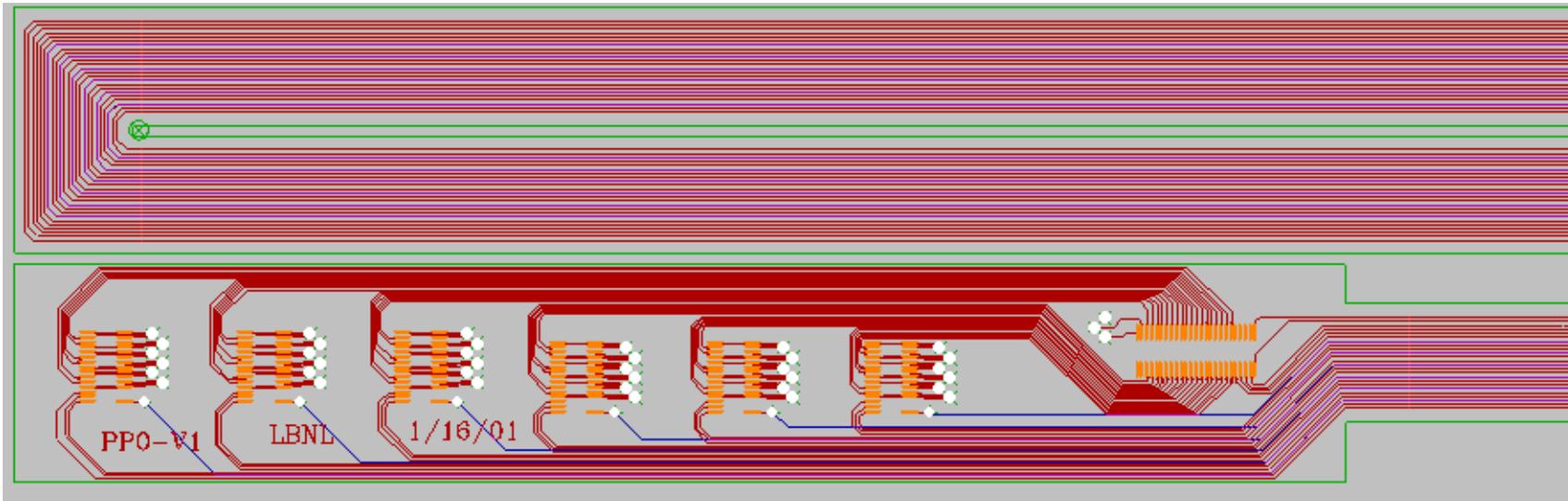
- Organize conductors for optimal layout of Pigtail, separating AC and DC connections, pairing connections on opposite sides of double-sided cable. Assume two module supplies, and leave more space around VDet connection.
- Include sense connections for high current supplies (VDD, VDDA):



- Use next size up in Elco 5087 line (second source?)
- Provide separate returns for sense/NTC lines.
- Assign three pins per supply since contact rating of 0.4A does not achieve 1A with 2 pins.
- Include VCal in list, though it is only needed for test connector NOT for Pigtail.
- Using 2 pins/supply and reduced HV clearance, could use 30pin part.

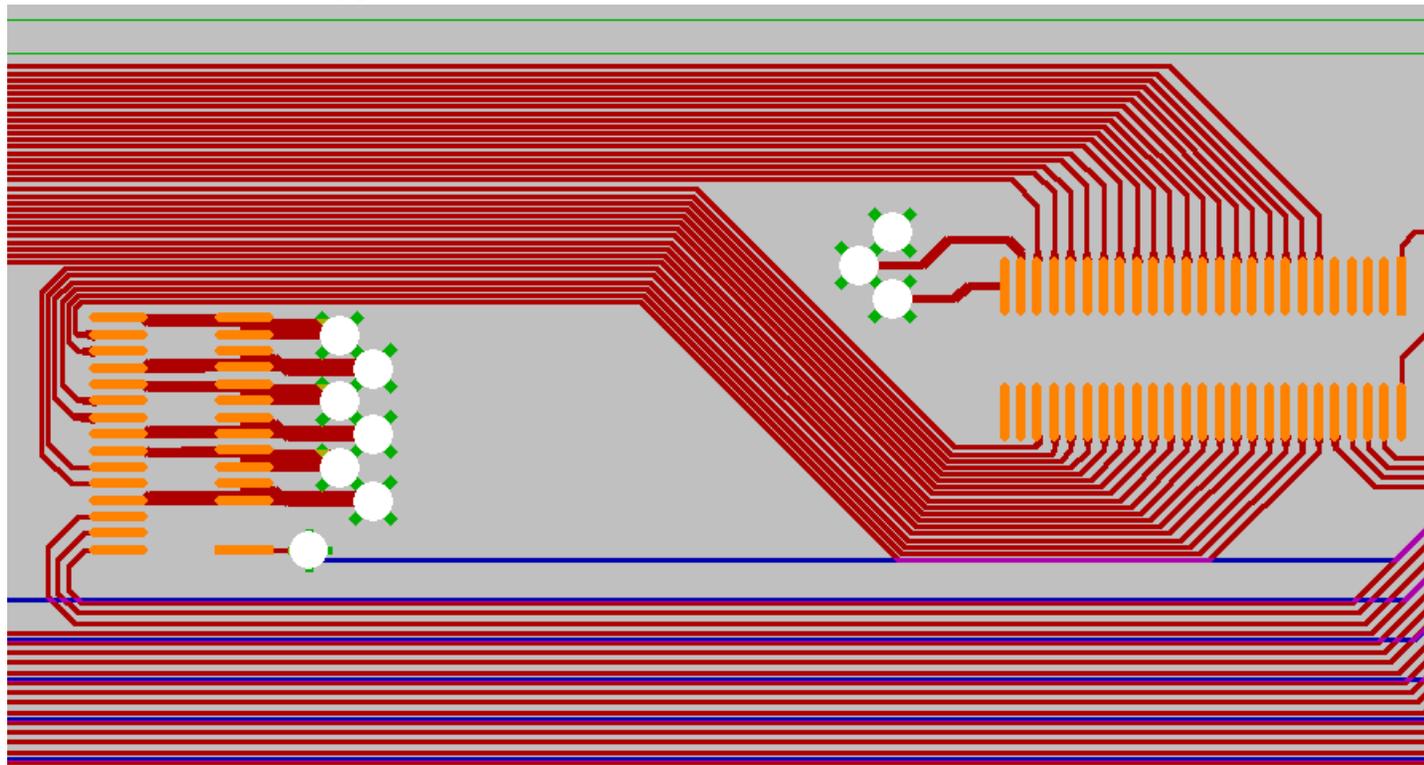
Comments on Type 1 cable connectivity:

- The present PP0 prototype uses a Flex Type 1 cable for signals and HV. The high current supplies (VDD, VDDA, VCCA, VVDC) are all carried on Aluminum wire, which is soldered to the Flex close to the surface mount Pigtail Connector.

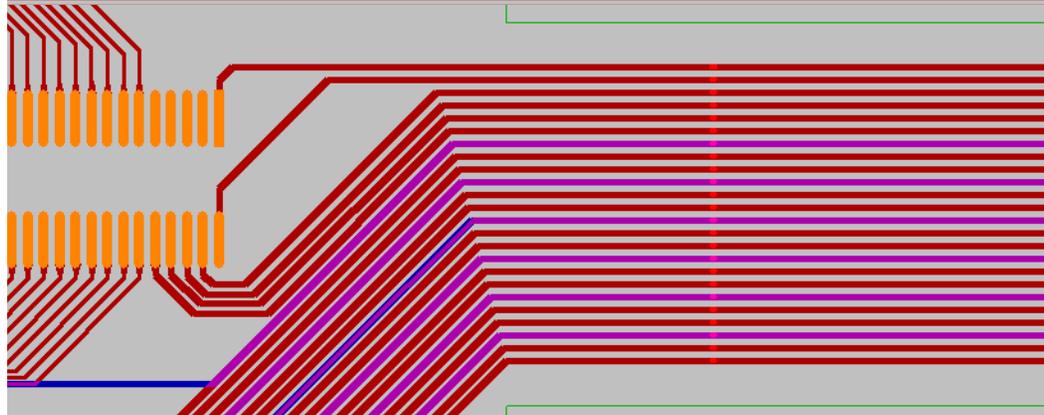


- This concept only leaves room to route about 3 wires per module from the Pigtail Connectors towards PP1 (RST and the two NTC signals), and about 6 wires from the Pigtail connectors to the opto-daughter connector.
- The new proposal would require four additional traces per module to route new sense lines back to PP1. It would also require two additional traces per module to route DTO2 traces back to opto-daughter connector.
- Implementing this will require some changes in the PP0 cable design.

- Implementing these additional connections (and other arguments) suggest that a better design would involve using small HV cables in place of the HV routing on the Flex Type 1 cable. This leaves both sides of the Flex free for signal routing.



PP0 prototype, showing region where traces to opto-daughter card pass on one side (3 pairs per module) and traces for Type 1 cable pass on the other side, filling all available space.



PP0 prototype showing cable region, where HV traces take up much of one side of the cable, leaving little room for more signal traces to PP1.