

Electronics Status

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DMILL Status:

- FE-D2 Testing and Irradiation
- MCC-D2 Results
- DORIC-D2/VDC-D2 Performance
- Next Steps and Decisions

Progress in 0.25 μ designs

- First TSMC submission in Jan
- Second set of submissions in late Feb (IBM MPW) and early March (TSMC)
- June Engineering run

Power Supplies and DCS Issues

- CAEN Prototype Test Results
- Addition of PP2 Regulators

Services Issues

- Issues raised by new Services plan

Status of DMILL Chips from FE-D2 Run

FE-D2 chips:

- FE-D2D and FE-D2S Probing completed, and all statistics sent to ATMEL. Naive digital yield for FE-D2S is decent (about 50%), if one ignores up to several dead channels per chip. Chips have adequate performance to justify further study.
- Six wafers send to AMS/IZM for bump-bonding with pre-production sensors. Get about 1 module and several single-chip assemblies from each wafer.
- Propose to take remaining FE-D2 wafer and back-side grind and metalize, then dice, to allow further studies of analog performance of FE-D2S and DORIC-D2 chips. A more ambitious possibility would be to send this wafer for bumping by IZM after plating to continue studies of back-side metalization effects on noise.
- First irradiations of FE-D2S performed in 88" at LBL. Results were very mixed. Global Register and Pixel Register survived in one chip up to a dose of 50MRad. Digital Readout did not survive in any of three chips beyond several MRad. Very significant increases in digital supply current were seen.
- Further analysis of irradiated chips to be performed, looking at performance of current reference and LVDS I/O in particular. For register tests to operate successfully, the XCK input and the DO output must operate correctly. However, because these are 5MHz operations, they would not be very sensitive to degradation in performance of the LVDS I/O due to bias changes.

- Need to probe internal nodes to check operation of digital readout and verify the quality of the internal waveforms. All of digital readout, including LVDS pad I/O, was simulated with post-rad corner models and all parasitics extracted, so significant failures imply either parametric shifts that are outside the corners (not really seen in June 00 irradiations of individual transistors), or a major flaw in our design/simulation procedure. Will vary supply voltages as well.
- Should try to isolate those block(s) causing failures, and understand what went wrong. This has a bearing on whether DMILL can be used as a vendor for the opto-chips, and also on whether our rad-hard design methodology, or some of our designs, have some flaws that could also affect future designs.
- Once this picture has become clearer, will probably irradiate further assemblies in April at LBL, and possibly at the end of May at PS.
- Do not plan any further FE-D submissions at this time. Producing an FE-D3S almost certainly requires a geometry change to 16 columns of 450 μ pixels.

MCC-D2 chips:

- Genova has spent quite some time testing 19 packaged MCC-D2 die. Of these die, only two pass all basic digital tests (command decoder and FIFO operation). This testing covers roughly 70% of total circuitry in chip. Several minor logic errors found in design, but nothing major so far.
- Problems encountered in operation of event building circuitry which are not yet understood. Behavior of all chips disagrees with simulation, and so expectation is that there is a problem in test setup.
- Given this low yield, do not propose at this time to develop die test capability and provide known good die to collaboration for making modules. Good packaged parts could be distributed for use in operating bare modules. Operating these parts requires upgrading the PLL firmware to support the new MCC protocols.
- With a yield in 5-10% range, would need 300-500 DMILL wafers to produce the chip, which corresponds to a prohibitive cost of 1.5-2.0 MCHF just for wafers.
- Situation with irradiated MCC-D0 is still poor. All 8 irradiated chips were working after 30MRad at the end of the irradiation. Only 4 were working once the part arrived in Genova, and only 1 is now working. Even after 100 C anneal, only one die is working. The behavior of the failed die is consistent with the XCK input failing. Further checks on whether failures are in the I/O pads or the core will be performed by looking at the CMOS test pins on the MCC-D0.

- Will concentrate on understanding all errors in the chip, to develop correct Verilog for synthesis of 0.25 μ version of MCC. Genova believes this can be done without building any modules, but operation of bare modules seems minimal check required.
- This means that we will have to continue to rely on MCC-AMS for the remaining FE-B modules. The supply of these die needs to be carefully monitored (roughly 100 tested good die remain). Some additional testing software for implementation in PixelDAQ is needed to allow verification of MCC-AMS “in-situ” during lab module operation.

DORIC-D2 and VDC-D2 chips:

- VDC-D2 chip was basically unchanged from the previous submission.
- Present version shows poor control of Dim Current (current sent to VCSEL for digital 0 input). The current value fluctuates significantly between die, and it depends on the ISet current. A fix for these problems is straightforward and will be implemented in the upcoming 0.25 μ version of VDC.
- Irradiations of VDC-D1 showed apparent problems with the current reference used for the LVDS I/O (factor 3 variation in output current, depending on whether reference is held reset or not). These problems need to be studied in more detail if we want to continue with DMILL versions of these chips.
- DORIC-D2 chip had many minor improvements from previous version. It now appears to operate correctly, but suffers from DC offsets in the preamp.
- First measurements have shown it to have a significantly higher noise or cross-talk level than the corresponding SCT chip (DORIC4A). This leads to poor Bit Error Rate performance for modest input signals (60-70 μ A PIN current). Very recent results indicate that this may be largely controlled by placing DORIC-D2 very close to the PIN diode (much closer than required for DORIC4A). Further studies of this “feature” are required to confirm that acceptable performance can be achieved. Possible studies with back-side plated chips are of interest, as this can affect analog-digital cross-talk. Improved preamp design should control DC offsets, and improved pad design from ABCD on input pads could help crosstalk.

- Results up to this time suggest that DMILL continues to be a viable vendor for the opto-chips. April irradiations of DORIC-D2/VDC-D2 with OSU opto-board will provide a clearer picture of this.
- There are difficulties in a 0.25 μ version of the VDC (worst-case VCSEL bias post-rad claimed to be 2.7V). Either one uses the thick gate oxide to allow 3.3V operation, with significant (but not well-characterized) reduction in radiation hardness, or one uses the thin gate oxide and the chip cannot be operated beyond 2.5V. Addressing this requires different design, with VDC in series between VCSEL and ground, possibly posing new problems. A 0.25 μ DORIC should be OK, but a mixed DMILL/0.25 μ solution would require dual-voltage operation for opto-cards, further complicating the services and power supplies.

• **Two possible paths:**

- DMILL remains the baseline, and the 0.25 μ effort is carried forward as a back-up. Priority should be to fully evaluate the DORIC-D2 and VDC-D2, improve the designs, and then submit a new version. There is a LArg MPW run likely to take place this summer, which could provide the opportunity we need. In general, it will be difficult to prototype. In this case, natural to have a thorough review of D2 generation of chips once irradiations and lab testing are completed, and prior to submitting the D3 generation (June/July ?)
- Concentrate on 0.25 μ version, in which case, ideally would schedule a review to check these designs in May, prior to submitting the engineering run in June. This review schedule seems to aggressive, so review would be later in the year ?

Next Steps and Decisions:

- Have reviewed these present results with ATMEL contacts during the last week at CERN. We still need to provide more detailed summary of probe data (at die level), and information on test structures placed in streets for evaluating leakage from poly over trenches.
- Present activity on ATMEL side is the exploration of impact of substrate material on the process yield for both ABCD and FE-D. Presently running a full lot, with 50:50 split between new and old epi vendor. Expected wafers-out date is in Week 22 (last week in May).
- We will characterize these test wafers for FE-D2D and FE-D2S yield. However, the present thinking is that the types of defects that might occur in the epi deposition could possibly explain the low yield of FE-D2D dynamic circuits, but would not be expected to affect the yield of static nodes significantly (hence FE-D2S and MCC-D2 yield would not be expected to change).
- The combined results from FE-D2S, MCC-D0, and VDC-D1 irradiations suggest that there are design problems with the LVDS I/O which need to be understood. These will be investigated further in the coming months.
- Propose that we continue our test program for the present chips. This includes evaluation of bump-bonded assemblies, and irradiation of FE-D2S, DORIC-D2 and VDC-D2. Do not see any strong need to irradiated MCC-D2 at this time, but this could still be considered for July PS run if this seems appropriate.

- Have already told ATMEL that we do not foresee any further engineering runs in this calendar year. If this is not the case, we need to provide schedule and quantity information to them for their internal planning.
- Do not presently see the need for more formal statement on future of FE-D and MCC-D efforts, although practically speaking, these two efforts seem to have reached a dead-end.

Status of 0.25 μ Design Effort

- Status of FE-I effort, including test chips to be discussed in more detail.
- Propose to schedule review of design in May, prior to the engineering run in June.

Status of MCC-I effort:

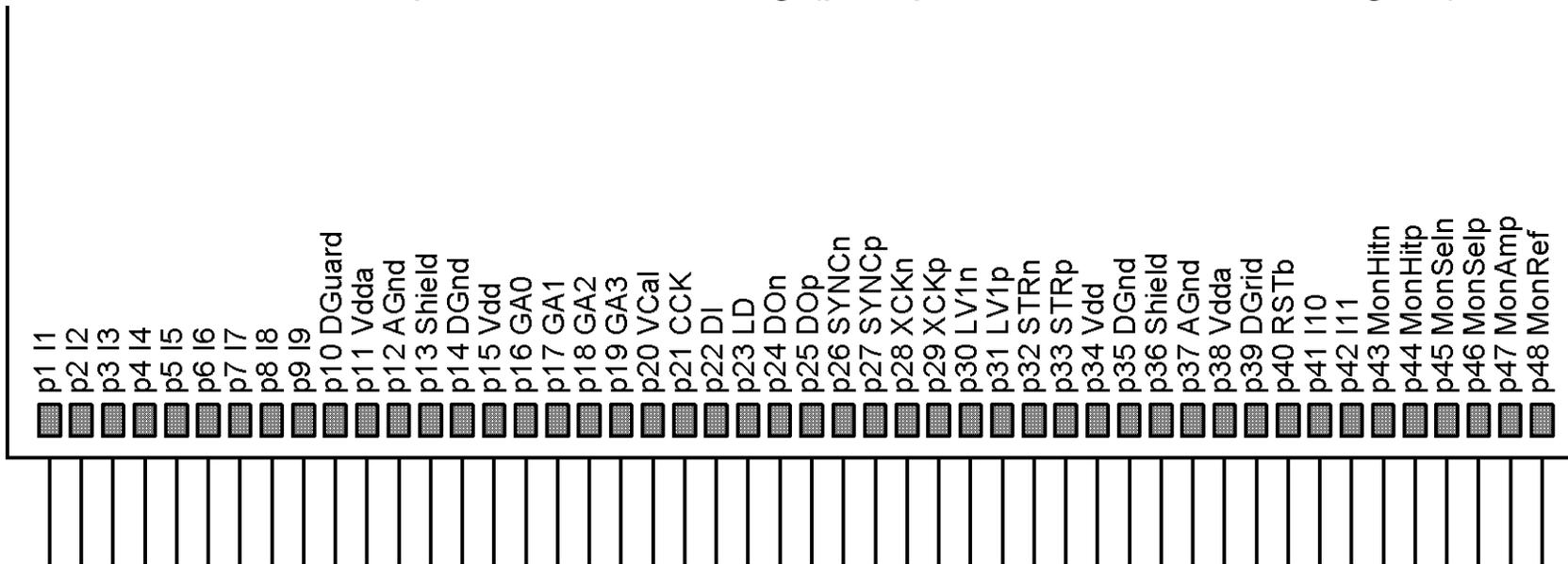
- Basic design will remain unchanged from MCC-D2, unless some major new surprise appears in the event-builder debugging. Continued work to understand this part of the MCC-D2 chip is critical to ensure that the starting Verilog for MCC-I is as bug-free as possible...
- Plan is presently to use RAL standard cells, plus CERN dual-port RAM block, plus conversion of delay block designed by Peter Fischer for MCC-D2 into 0.25 μ . Some technical issues to resolve on this path in the very near future.
- Schedule is very aggressive at this time, with only about three months to prepare final GDS (reserving some time at the end for final verification and DRC checks). In order to meet this schedule, Genova will need to throw all available resources full-time into this effort.
- Alternative is to perform a second engineering run just for MCC-I. This will result in delay, extra costs for second run, and more chips than are needed.
- Have wanted to review this design for some time. This was postponed for MCC-D2 due to lack of time before submission as part of FE-D2 run. It seems impossible to review the MCC-I before submission. This is not very comfortable.

Status of DORIC-I and VDC-I effort:

- Siegen and OSU have been working on prototype submissions for Feb 28 MPW run. This would include two VDC designs (standard one, plus one with improved Dim Current generation), and an improved DORIC (feedback for preamp to eliminate effect of DC offsets in input devices).
- This would naturally lead to submission of improved designs as part of FE-I engineering run in June.
- We need to clarify whether any basic configuration changes are needed for final opto-cards (changes in chip aspect ratios, improved pinouts, multi-channel versions of chips) very soon, so that such modifications could be included for June.
- As mentioned before, we need to clarify the relative priority of work on DMILL and 0.25μ versions of opto-chips. This would determine the focus of the opto-chip design groups over the next 6 months.
- The opto-chips should be reviewed fairly soon to understand whether the design and performance of the present chips meets all of our requirements. Would prefer to do this before June, but this schedule seems too tight, as key reviewers are tied up in other efforts until that time.

Proposed Pad Geometry for FE-I (almost finalized):

- Increase present pad size to $100\mu \times 150\mu$ rectangle, with 150μ pitch, to provide more pad area for rebonding. Include MCM-D bump-bondable I/O pads with the same geometry used in FE-D (relative to the bottom of the wire bond pads).
- Continue to locate pads close to the lower die edge, as for demonstrator chips.
- The present demonstrator geometry has 48 pads, with centers along a line 175μ above the bottom (referenced to the as-cut die size of $7.4 \times 11.0\text{mm}$). The first pad center is also 175μ from the vertical edge referenced to the as-cut die size.
- Propose that this pad placement would be retained, and only the central 30 pads would be used for production bonding (p10-p39 are in bondable region):



Test Chip Program

Take advantage of frequent runs, rapid turnaround of TSMC:

- Earliest date for useful submission was Jan 8.
- Goal of the initial submission was to include several of basic blocks from FE-I, and evaluate their performance.
- Check that we understand design rules, agreement of performance with SPICE, and behavior during irradiation (SEU) and post-rad (total dose) is as expected.

List of blocks included:

- Current reference and current DAC used in bias control.
- Redesigned LVDS driver and receiver blocks (only driver included).
- Pixel RAM block with 32 memory locations and sense amplifier readout.
- Several basic shift registers, for evaluation of SEU performance. Designs included: standard cell version, CERN SEU-tolerant version, improved Bonn SEU-tolerant version, and three-fold majority logic version.
- Preamp test block with first version of preamplifier design.
- Miscellaneous test structures for gate rupture, and other ideas.

A small chip of 12mm² was submitted at 13:00 on Jan 8.

- Estimated wafers out date advanced to Feb 21 (8 weeks turn-around !)

Proposal for testing, in light of known errors in design:

- Cutting three traces using FIB should allow application of digital power, and testing of 3 shift register blocks (standard cell, Bonn SEU-tolerant, and CERN SEU tolerant) plus the Pixel RAM block.
- There seems to be little hope for testing analog blocks without vast FIB effort.

Next Steps in Test Chip Program:

- Originally planned to make second TSMC submission on Feb. 5. This was to be the equivalent to the Analog Test Chip prepared by Peter Fischer for the DMILL runs. We were not adequately ready for this date, and have postponed.
- Meanwhile, CERN has significantly tightened their MPW submission rules with the goal of more reliable turn-around dates (now claim possibility, but not guarantee, of 12 week turnaround), and has added a second April run. Given this, we decided to participate in the Feb IBM MPW with a 16mm² die, in the hopes that we might receive the test chips by June 1. Note this is a 3M run only, so some modifications from the full test chip are required.
- We intend to also send this test chip to TSMC on Mar 5.
- These two submissions should give us significant feedback on fairly final aspects of our analog design in middle to late May if turn-arounds are good.
- Present status is that Peter F. has sent almost complete layout to LBL for checking, and expect to finalize core early this week. Schedule looks OK for IBM.

Milestones in overall schedule:

- Some slippage over original very aggressive June 1 schedule, but believe this can be limited to a few weeks. Critical phase will be verification, which is largely still to come.
- Submission should still be during June (we have reserved a run during Q201, and if we slip beyond this, there will be a 30K\$ penalty to submit in Q301).
- In order to get the guaranteed turnaround, the design would need to be DRC-clean, requiring us to begin foundry-level DRC checking (using Hercules) at least several weeks earlier.
- We are already running the Cadence (Dracula) and the Mentor (Caliber) for IBM, but we have discovered that the Dracula rule set is not complete (ESD rules missing). Will make comparisons with Hercules soon we hope.
- Worst case thirteen week turnaround in the frame contract would give wafers during the month of September. This might allow some testbeam and irradiation studies at CERN before shutdowns in early November. Most optimistic schedule would be an 8 week turn-around, that would give wafers during August.

Power Supplies and DCS Issues

CAEN Prototypes:

- First evaluation results from Wuppertal and Milano show unacceptable ripple performance, and very poor power conversion efficiency.
- The differential ripple is in the range of 60-140mV, which is too large, but our specification of 10mV ripple may also be too strict. The ripple relative to chassis ground is very large, in principle less important, and should be easily improved.
- The power conversion efficiency for single channel operation seems to be only about 10%.
- Significant set of measurements underway, and will know much more soon.

Other prototypes:

- Will be receiving DPS LV/HV prototype and ISEG HV prototype. These will need to undergo evaluation as well.

PP2 Regulators:

- Variety of reasons why placement of regulators at PP2 is attractive. These include: relaxing ΔV specification on long conventional cables, much improved transient protection, improved noise reduction in sub-MHz region, local voltage sensing over 7m loop instead of remote current sensing over 140m loop.

- Many of these issues are particularly critical for the 0.25 μ chips, where there is very little margin for errors in providing supply voltages. Believe that use of these regulators at PP2 is essential. Possible fall-back is to place them at PP3 instead.
- The advantages need to be balanced against the risk of including additional components in a rarely-accessible region of ATLAS. This proposal depends critically on the existence of the ST Rad-Tol regulators (as do the LArg FEB boards). The prototype quality for these parts has not been converging as rapidly as expected, but should see something of production quality by late 2001.
- Implementation in PP2 appears feasible. Propose prototyping effort (as part of power supply/power cable evaluations) be carried out. Compatibility of services still needs study, as it appears that the sense lines carry significant current for ST regulator scheme.
- We would make a final decision after completing studies of complete power distribution system. Meanwhile, we should keep both options open as possible.

March 8 ID power supply review:

- Review to cover present power supply and service specifications/descriptions.
- Goals include: examination of services in gap to provide input to gap dimension adjustment in near future, improved uniformity in ID powers supply designs, and cost reduction in these areas.
- We will have a significant presence there, and will provide documentation of power supplies and services.

DCS Issues:

- Need complete enumeration of all monitored quantities, along with corresponding requirements for LMB boards and sensors. There are many environmental monitors for temperature of structures, cables, etc.
- This information should be integrated into the evolving Services Document.

Services Issues:

- Significant progress in detailed definition of services inside PP2. Documented description in preparation (thanks largely to Marco), to be edited by Marco and Kevin into first complete draft in time for the power supply review.
- Some issues were raised during preparation of this document, most of which could be resolved without much controversy. Have now agreed on a scheme in which there are only two supply voltages for the module, and there is full sensing for each module at least to PP0, and preferably to the end of the module Pigtail.
- Opto-links issues need broader consideration. They include possibility of a dual-technology opto-card (DMILL+0.25 μ) which would need two VVDC supplies, and the level of redundancy required in opto-card controls and supplies. These issues have significant implications for services, power supplies, and opto-chips.
- Proposal was made to divide non-B-layer opto-cards into two (3+3 or 4+3 modules) for extra redundancy. For B-layer, prefer individual module redundancy. In the absence of any detailed information on failure modes, proposed redundancy is only in extra VVDC connections (assuming shorted chips is major fault source). Other voltages (VPIN, VISET) remain common for each opto-card.
- Questions include: do we continue to use single-channel opto-chips, or move to 4-channel opto-chips (this is somewhat package dependent).
- Second question: do we make all aspects of system (Flex design, Pigtail design, PP0 design) B-layer compatible, or move to separate designs for these parts ?