

FE-H Status at LBL

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Organization of Basic Tasks:

- What they are and who is doing them.
- Note that progress on this chip has clearly been significantly reduced by the large effort to debug and re-submit FE-D. Clearly, because of this, the Bonn contributions to FE-H will be reduced below our initial expectations.

Status:

- Quick overview of present status, highlighting recent progress on digital readout in the column pair.

Gerrit will give separate talk on details of his work on FE-H.

Organization

Basic Tasks for FE-H:

- **Front-end design:** preamplifier and discriminator.
- **Miscellaneous analog cells:** current and voltage DACs, current references, VCCD/VTH amplifiers, FE bias generation cells, LVDS drivers and receivers, and calibration chopper.
- **Control logic:** command decoder, global register, pixel register, pixel control logic, hitbus OR tree, column mask logic, output MUXes.
- **Pixel readout logic:** hit logic, LE/TE RAMs, address ROMs.
- **Bottom of column logic:** sense amplifiers and CEU logic plus buffering.
- **End of column logic:** EOC buffers, horizontal sparse scan, plus buffering.
- **Peripheral digital logic:** grey generator, reset generator, clock generators, self-trigger logic, readout control logic, trigger FIFO, TOT subtractor, serializer.
- **Overall integration and floorplanning:** placing all blocks, routing all interconnects, and assessing global signal distribution issues.

Status Summary:

- First pass of assignments have been made for these tasks.
- TAA agreements are ready, and Honeywell should have distributed design info.

Status

Overall:

- Layout rules have now been finalized with Honeywell. Gerrit has updated his Cadence files to support layout (including nice p-cells for transistors) according to these rules. We still do not have the Dracula rules we would like, but this is much less critical.
- Gerrit working on layout for Standard Cell library (similar to that of AMS). The intention is to perform higher quality Verilog simulations (including output drive strength), and also to use automatic place and route for non-critical circuit blocks where possible (control logic and digital peripheral logic) to accelerate schedule.
- We would like to move to the next major Cadence release (our present 9502 release is no longer supported or distributed by Cadence). The exact sub-version is likely to be 4.4.2. One issue remains doing ELDO netlisting, where new versions are required, and real purchases may be necessary.

Front-end Design:

- Laurent has TAA paperwork complete. He should be able to start on FE-H front-end work as soon as he is comfortable with the HSOI process...

Analog Cells:

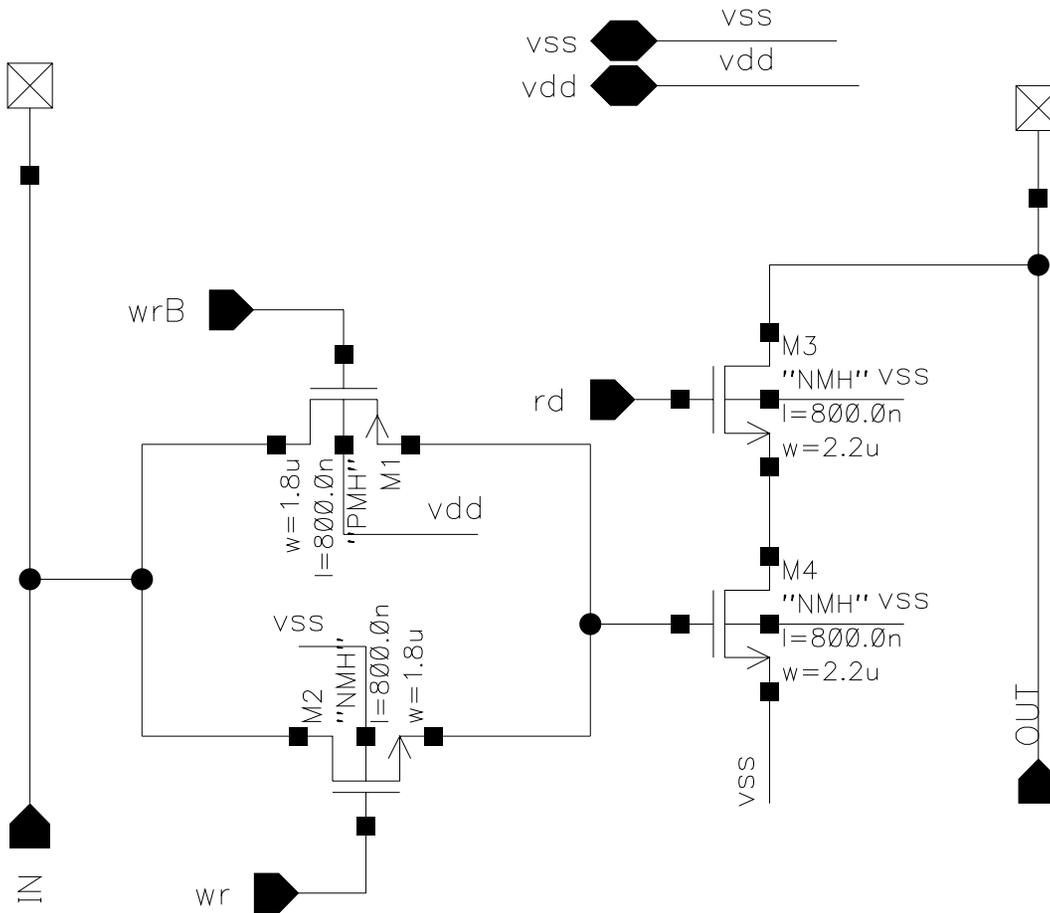
- For FE-D, these were designed by Laurent and Peter. There are several new issues to look at, including a CMOS current reference, and a more compact DAC design. In DMILL, there is guaranteed space available under analog power busses. In HSOI (3-metal) this is less attractive, and we need to find space for extra EOC buffers. This work would be shared between Bonn and LBL, depending on manpower and FE-D re-submission in particular. Final validation of these blocks would of course involve Laurent.

Control Logic:

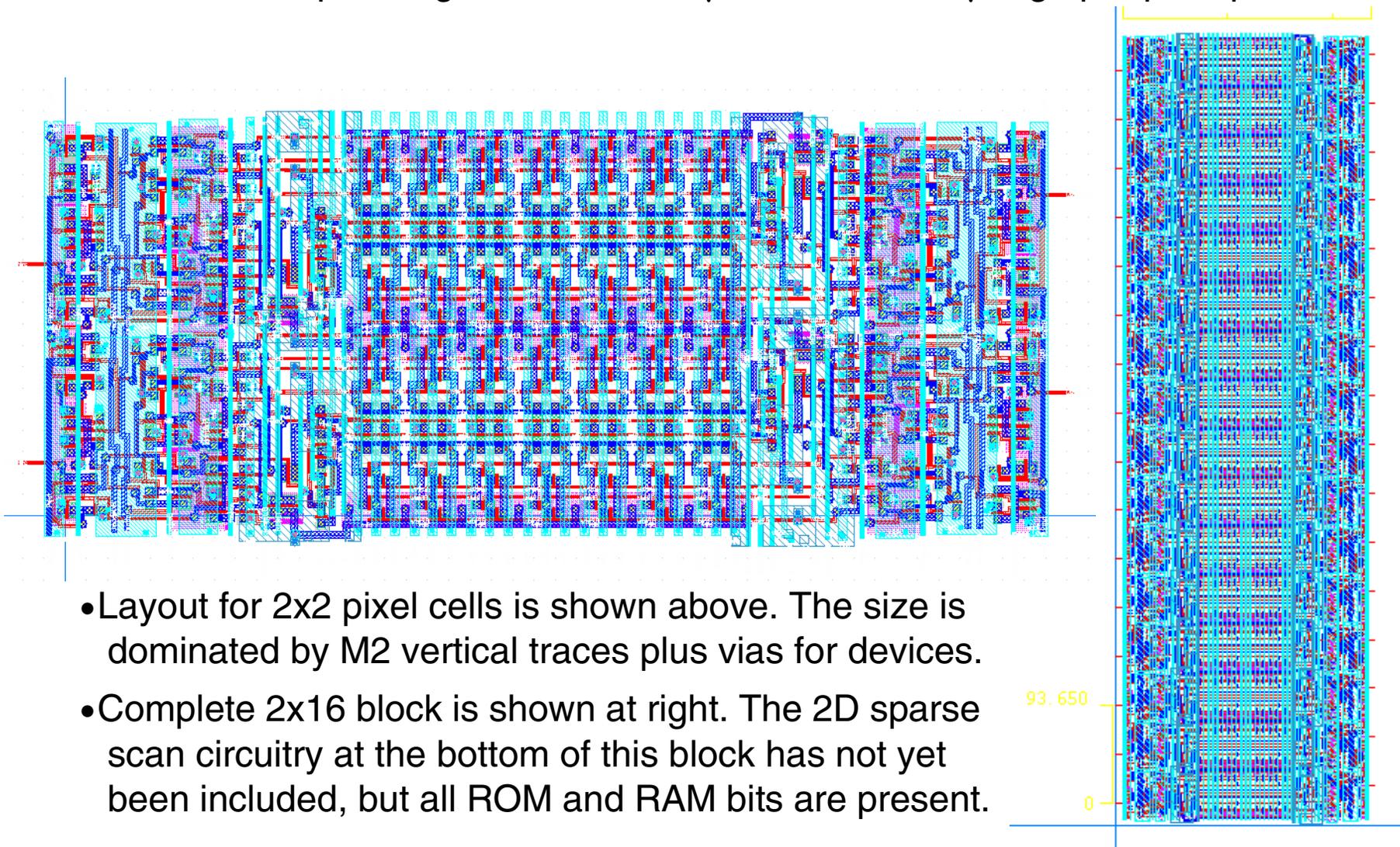
- This was all designed and implemented by Bonn for FE-D, and it is natural that they would do some of this again. We hope to gain by using Synopsys and Gerrit's standard cell library for some of this work, in which case Bonn would only have the custom layout blocks to worry about (basically the control block in the pixel cell and the mask enable block at the bottom of column).

Pixel Readout and CEU Logic:

- Emanuele has been working on this. He has improved the hit logic in the pixel to eliminate all significant multi-hit problems (only remaining problem is when a second hit overlaps the 12.5ns wide ClearPix signal), and has improved the RAM cell design with a transmission gate and NMOS instead of PMOS:



- A first pass layout of the complete digital column (DigCol2x16 block of FE-D) has been completed with these improvements. The present size (for a column pair) is 236μ wide, and about 93μ high per pixel pair. For comparison, the FE-D layout after lots of squeezing was about 274μ wide and 96.5μ high per pixel pair.



- Layout for 2x2 pixel cells is shown above. The size is dominated by M2 vertical traces plus vias for devices.
- Complete 2x16 block is shown at right. The 2D sparse scan circuitry at the bottom of this block has not yet been included, but all ROM and RAM bits are present.

- The new design has been simulated with a modified CMOS sense amp design at the schematic level. The next step is to carry out the simulations of a complete column pair with parasitics to make sure that the sense amp readout and the sparse scan logic are fast enough. Note, for now these simulations are being done with HSPICE because we have not yet upgraded our license for the ELDO interface to Cadence to 4.4.x
- Depending on the available space in the end, we could also consider one additional improvement to the hit logic by changing the edge-sensitive dynamic FF to a static version (5 additional transistors). This would make the pixel static, except for the duration of the Hit/Freeze response time, and would eliminate the possibility of the present “row 0” types of problems.
- Note that this readout logic layout, combined with (for example) Franz’s layout for the front-end and control logic, would give about a 270μ pixel size. Therefore, this looks quite promising for achieving our 300μ pixel size goal, but before the complete bottom of column and end of column layouts are done, we will just have to wait and see...

End of Column Logic:

- No work has begun on this yet. The schematic seems OK, and so the major task is to create a very space-efficient HSOI layout. This will also be shared between Bonn and LBL depending on available manpower.

Peripheral Digital Logic:

- This is being handled by Gerrit, who will discuss progress in a separate talk.

Floorplanning:

- Very little has been done on this yet. There is a preference on the part of some of us for a floor-plan more like that of FE-B, in which the bias and DAC blocks are in the bottom of column region rather than the bottom of the chip. This will evolve as the basic blocks come together.