

FE-D Digital Readout Testing

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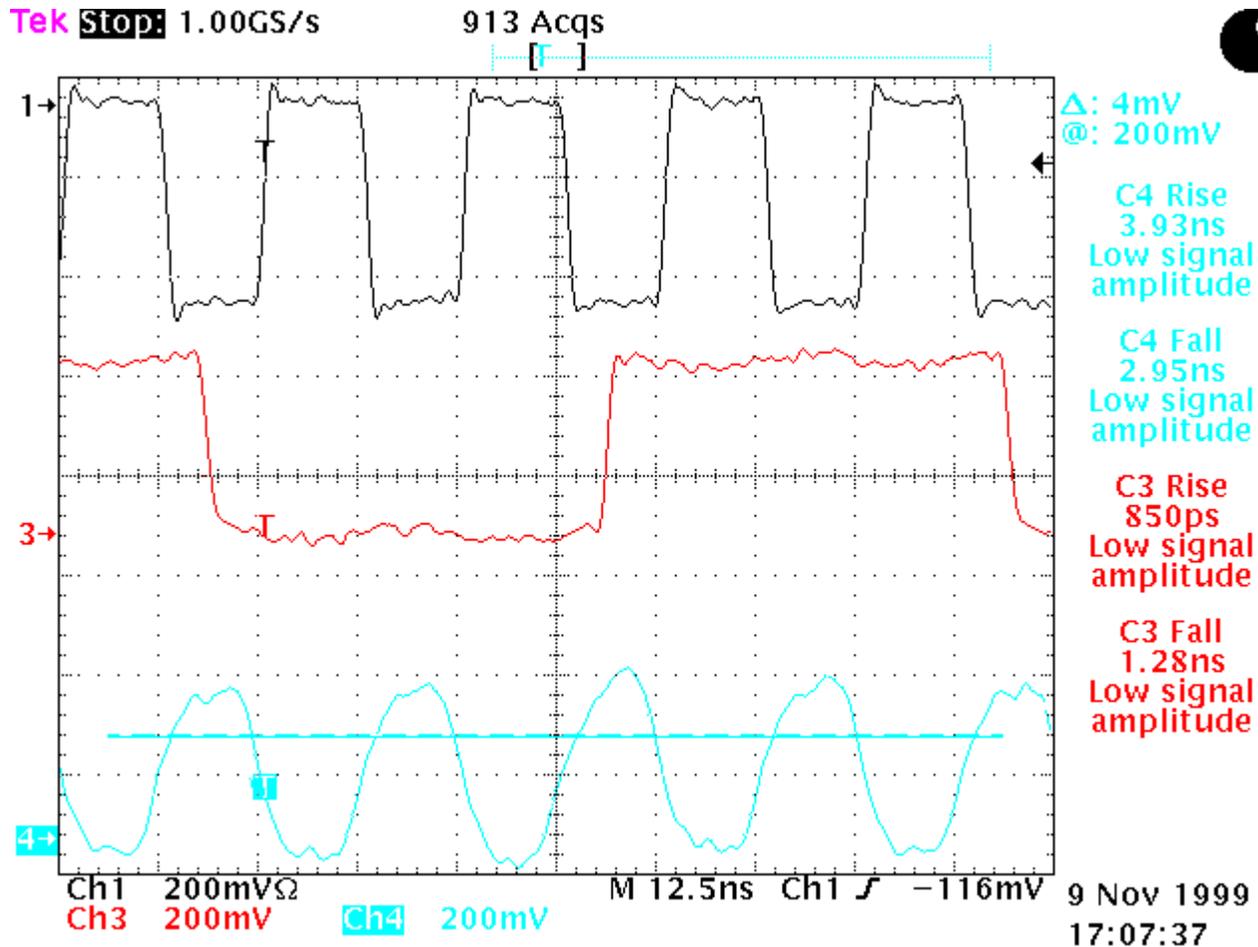
Describe some comparisons between simulations and measurements for several FE-D problems:

- Compare internal XCK in the lab and in simulation.
- Compare internal CLK1/CLK2 in the lab and in simulation.
- Compare internal SDO in the lab and in simulation.

In all cases, the agreement between the simulation and the measurement is fair, but not perfect. It is probably at about the level one would expect for these relatively crude simulations.

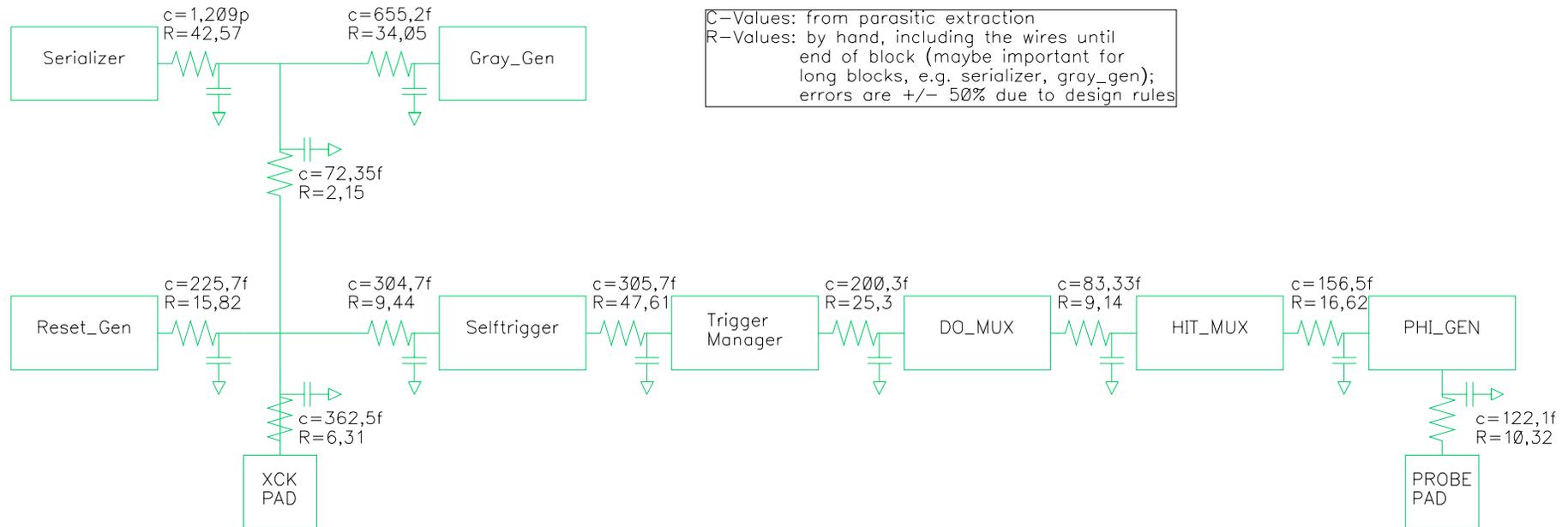
Measurements and Simulations of XCK

- Realized that there is a serious problem with XCK distribution inside FE-D, with relatively small transistors in LVDS receiver driving a fanout to 72 FF over a large, minimum width, set of busses. Total C is about 4pF.



- Observe very poor risetime on internal XCK of about 5ns (10-90%). Duty cycle at VDD/2 is still 50%.
- For reference, TSC0 is also shown. It has a risetime of about 1ns, as expected for the combined Picoprobe and scope bandwidth (500 MHz).

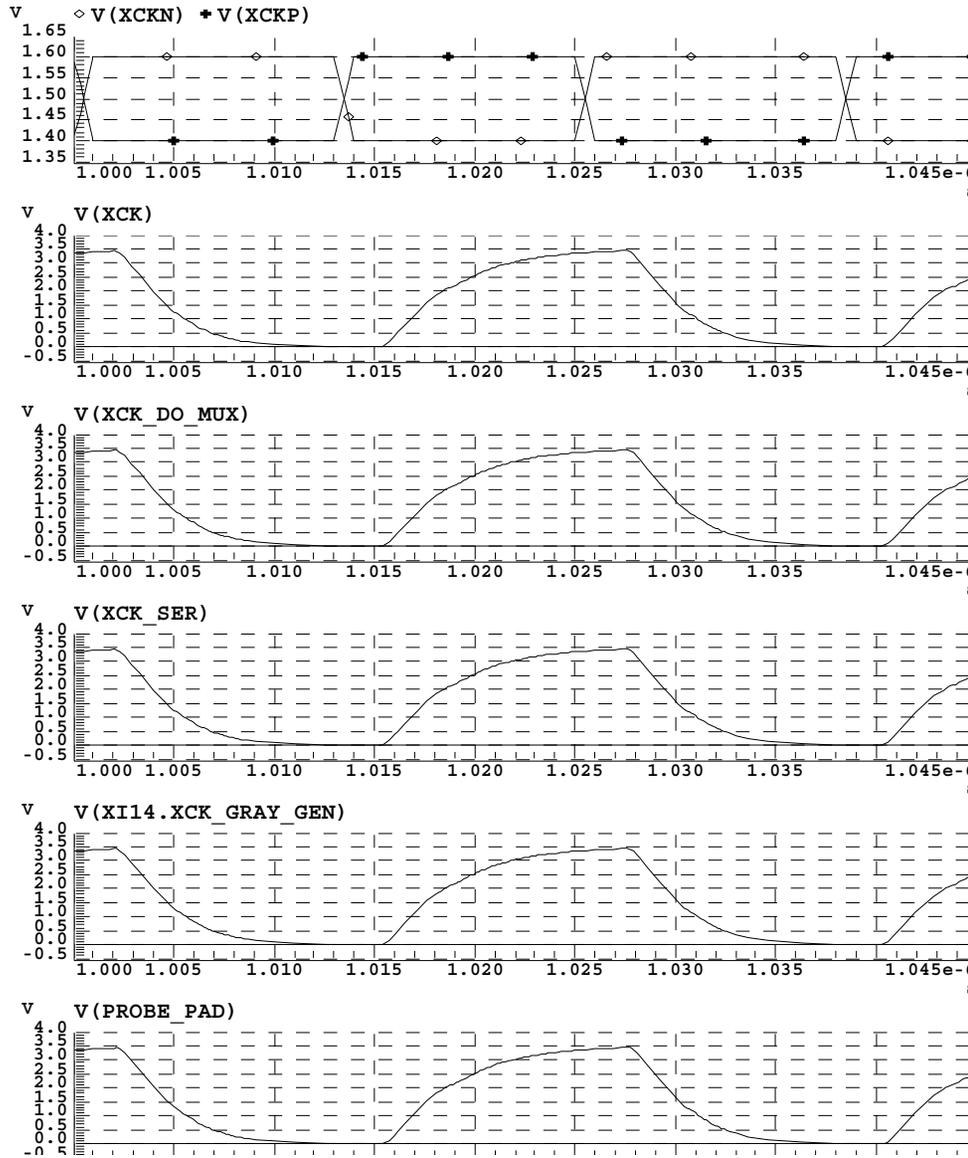
• Simple R and C model of internal XCK distribution (values extracted by Mario):



- This model was included onto the top two sheets of the FE-D schematic, and a new ELDO netlist was extracted (thanks to Gerrit).
- Simulations were done, at both 3.5V and 4.8V VDD supply voltages.
- An additional simulation was done with an externally injected “perfect” XCK on the probe pad, for comparison with external XCK injection measurements. Recall that in the lab, a modest improvement in required VDD was observed with an externally injected clock, but the required VDD was still much larger than 3.0V.

•Results for XCK simulation at 3.5V:

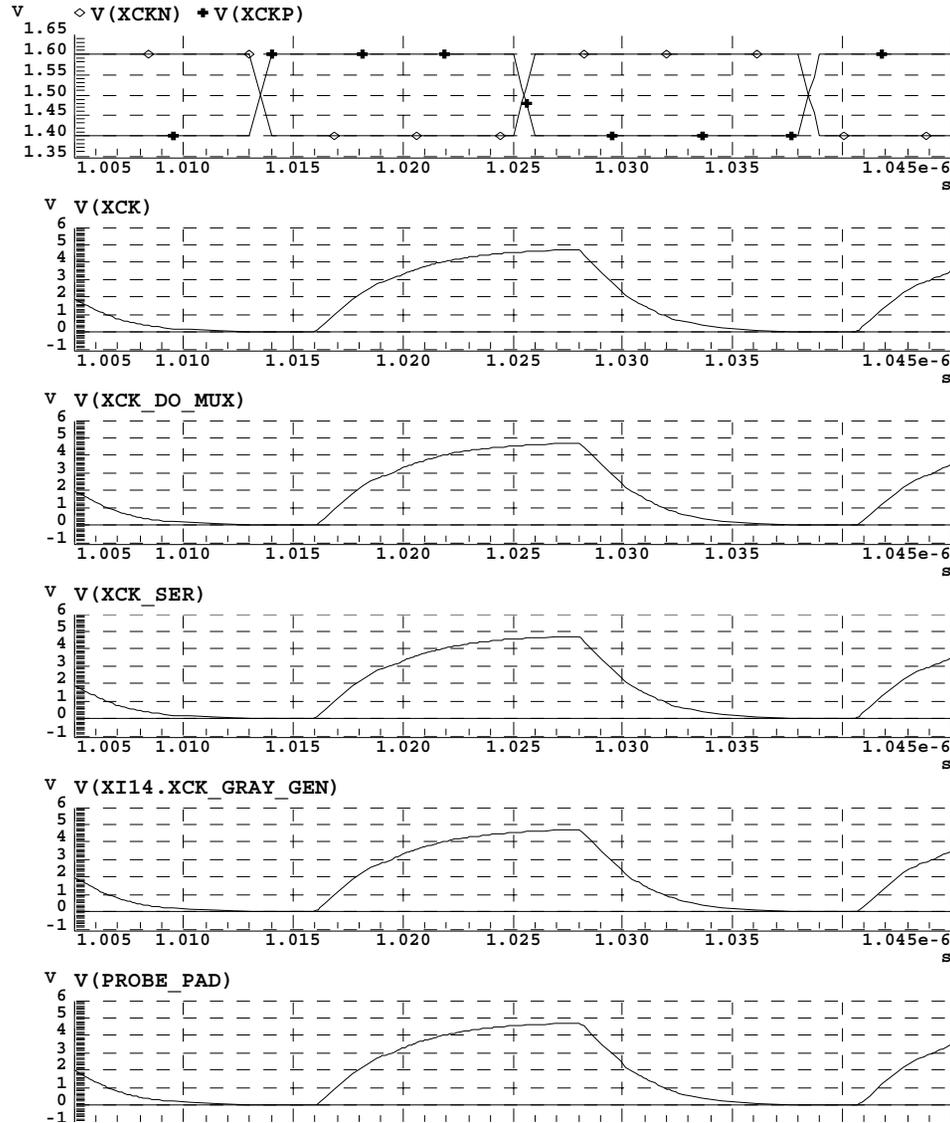
14-Dec-1999 File : top160rc35.cou
 22:22:09 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/VDD/DI



- The risetime from 10-90% is about 6-7ns, in fair agreement with lab measurements.
- Here also, the duty cycle looks close to 50%, so after the first inverter in a given block, the XCK should look fine.
- The waveform looks essentially the same at all nodes.
- The Serializer and MUX nodes are particularly far apart. This suggests that the internal R's are not very important, and the distribution could be approximated well by just using a total value of C.

•Results for XCK simulation at 4.8V:

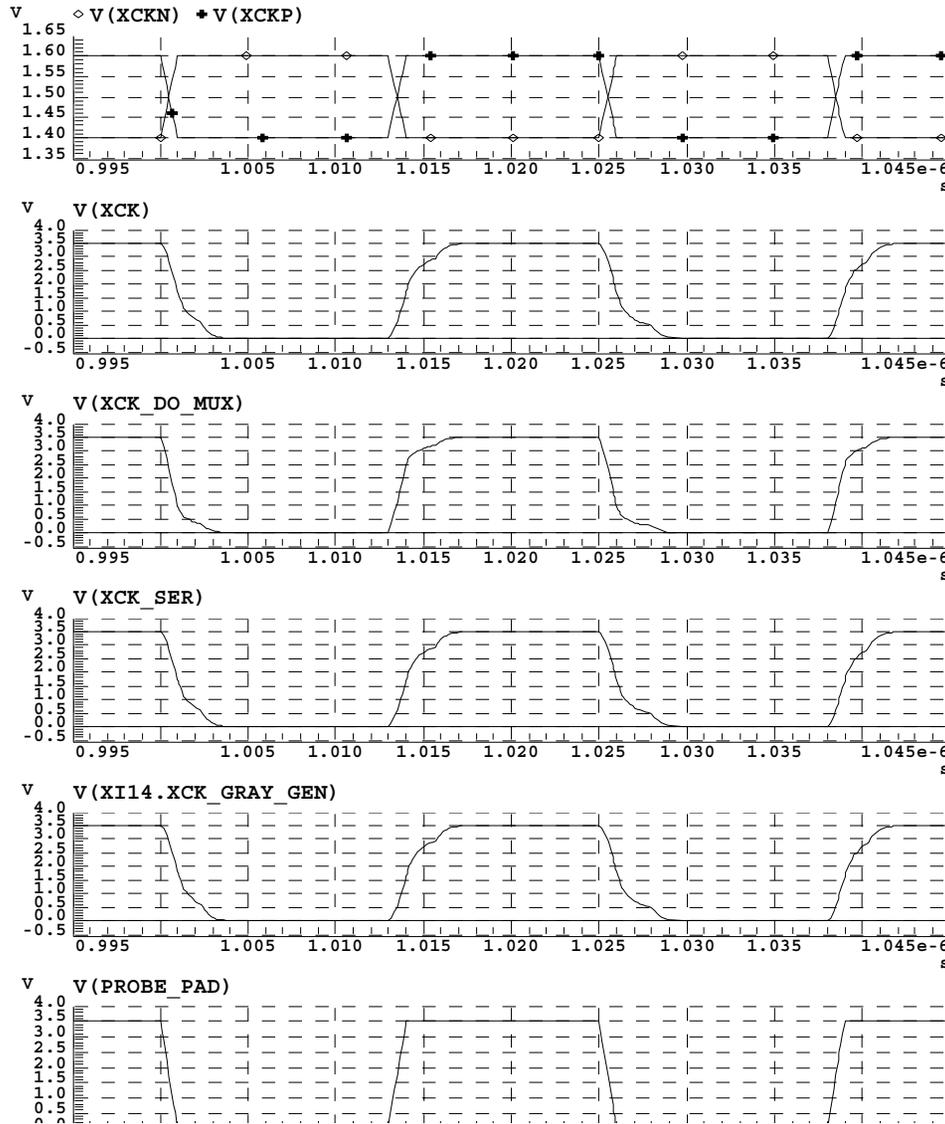
14-Dec-1999 File : top160rc48.cou
 13:39:01 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/VDD/DI



- Results at the higher supply voltage are almost identical.

• Results for simulation at 3.5V with externally injected XCK:

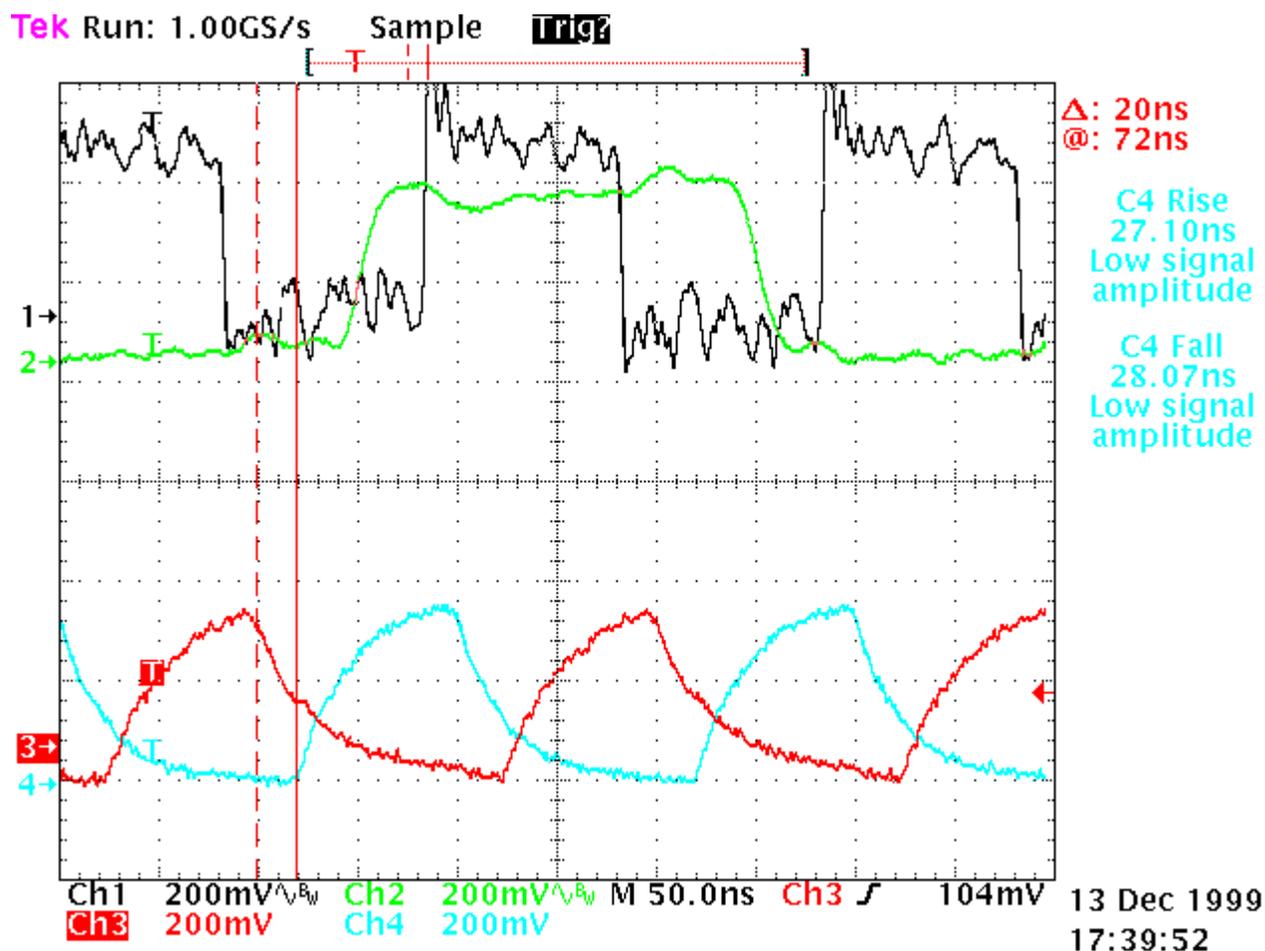
15-Dec-1999 File : top160rcpad.cou
 06:56:58 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/VDD/DI



- The internal waveform is significantly improved compared to that of the internally generated XCK.
- There is little difference between the waveforms at different internal nodes, even those which are far apart on the net like the serializer and the output MUX.
- This suggests that the XCK distribution problem does not explain the major digital readout problems in FE-D.
- Nevertheless, the buffering for this distribution should be increased by at least five for postrad safety.

Measurements and Simulations of CLK1/CLK2

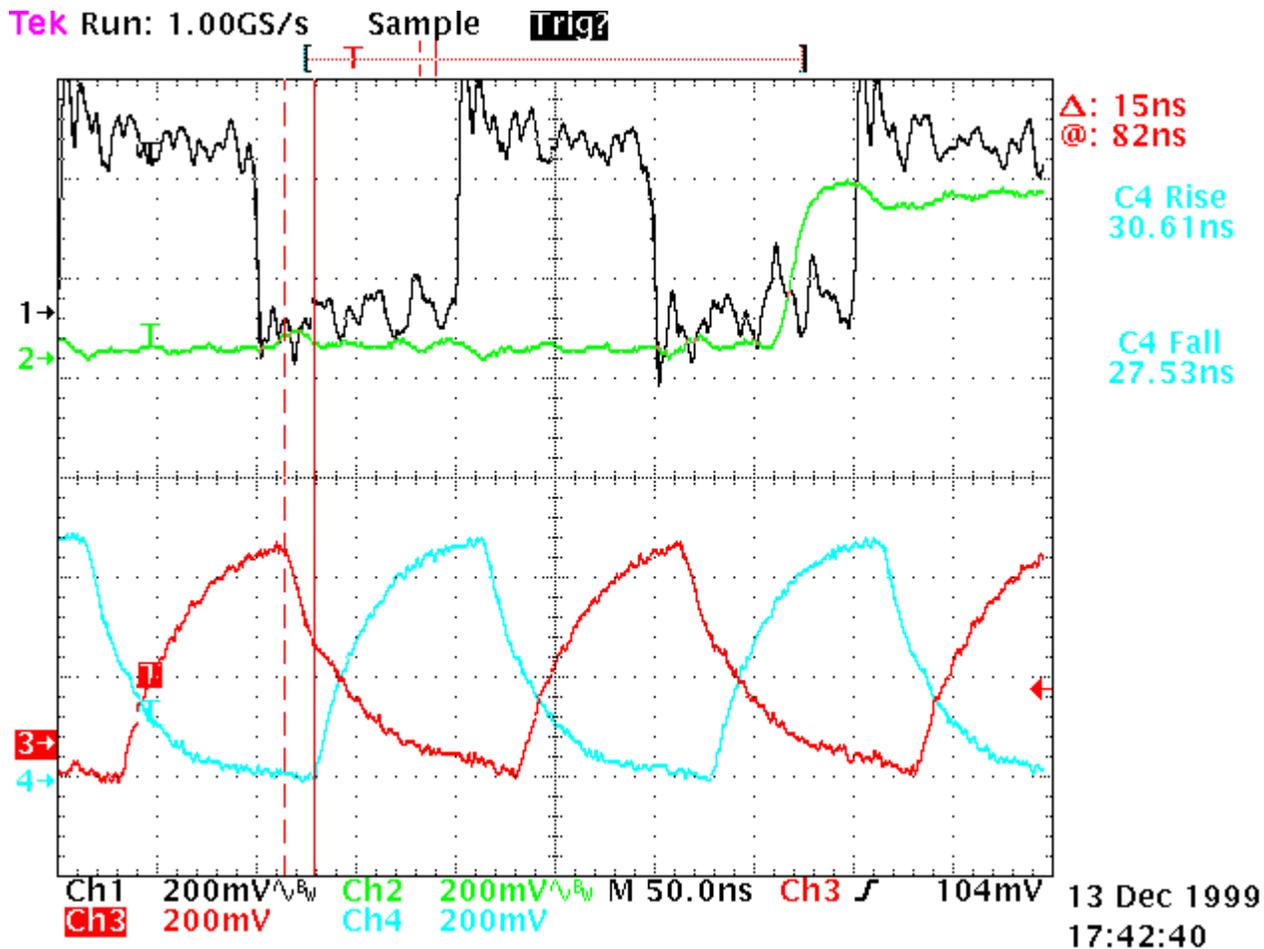
- Measure CLK1/CLK2 waveforms on FE-D using Picoprobes:



- Observe about 30ns risetime.
- Generated non-overlap seems to be about 20ns (measured from waveform corners).
- The actual non-overlap seen inside of a given shift register cell will depend very sensitively upon the thresholds for the two clock phases.

- Observe almost 30ns risetime, but only 20ns “generated” non-overlap time in clock generator at 3.5V, so would expect that the operation is marginal.

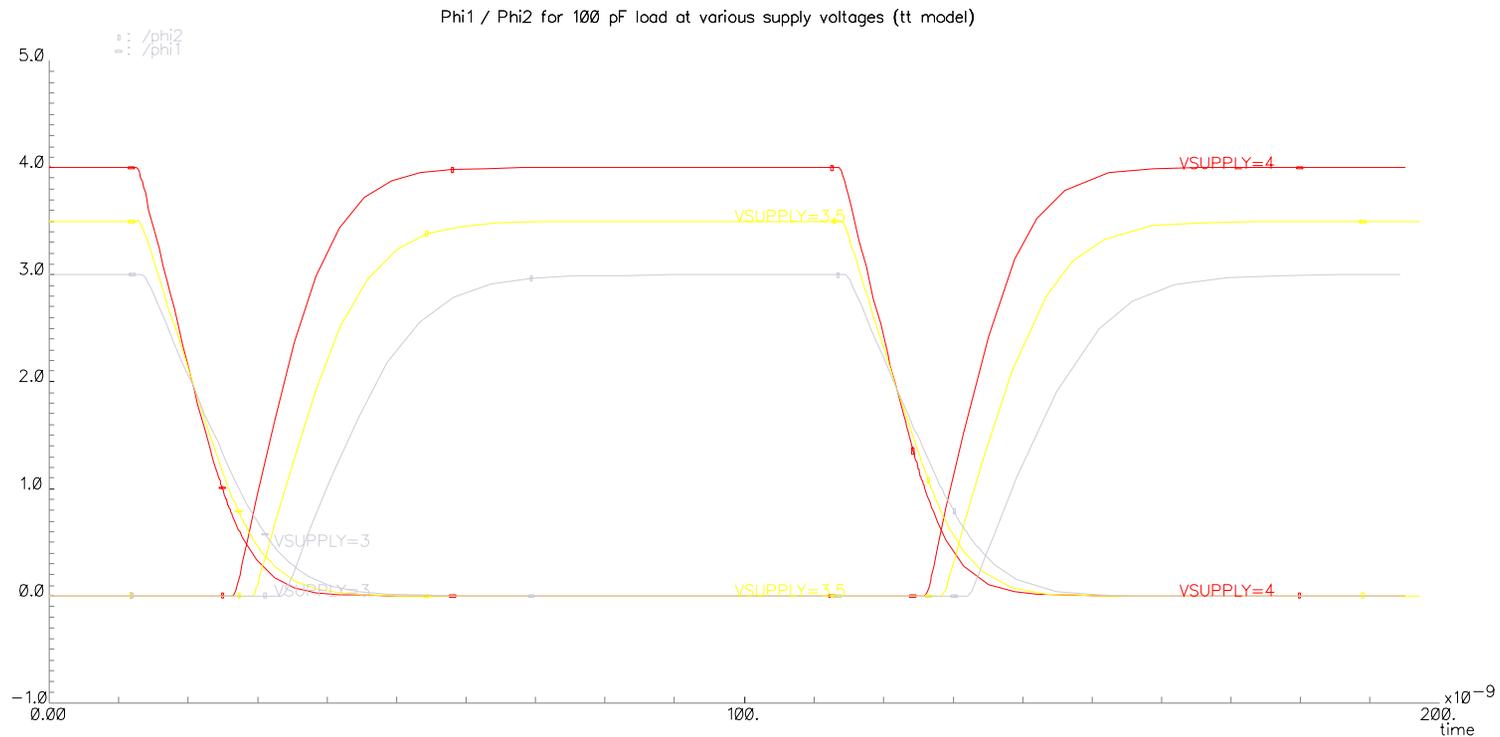
•Measure CLK1/CLK2 at 4.8V VDD:



- Observe about 30ns risetime again.
- Generated non-overlap seems to be about 15ns (measured from waveform corners).
- Actual non-overlap may be very small inside of a shift register cell.

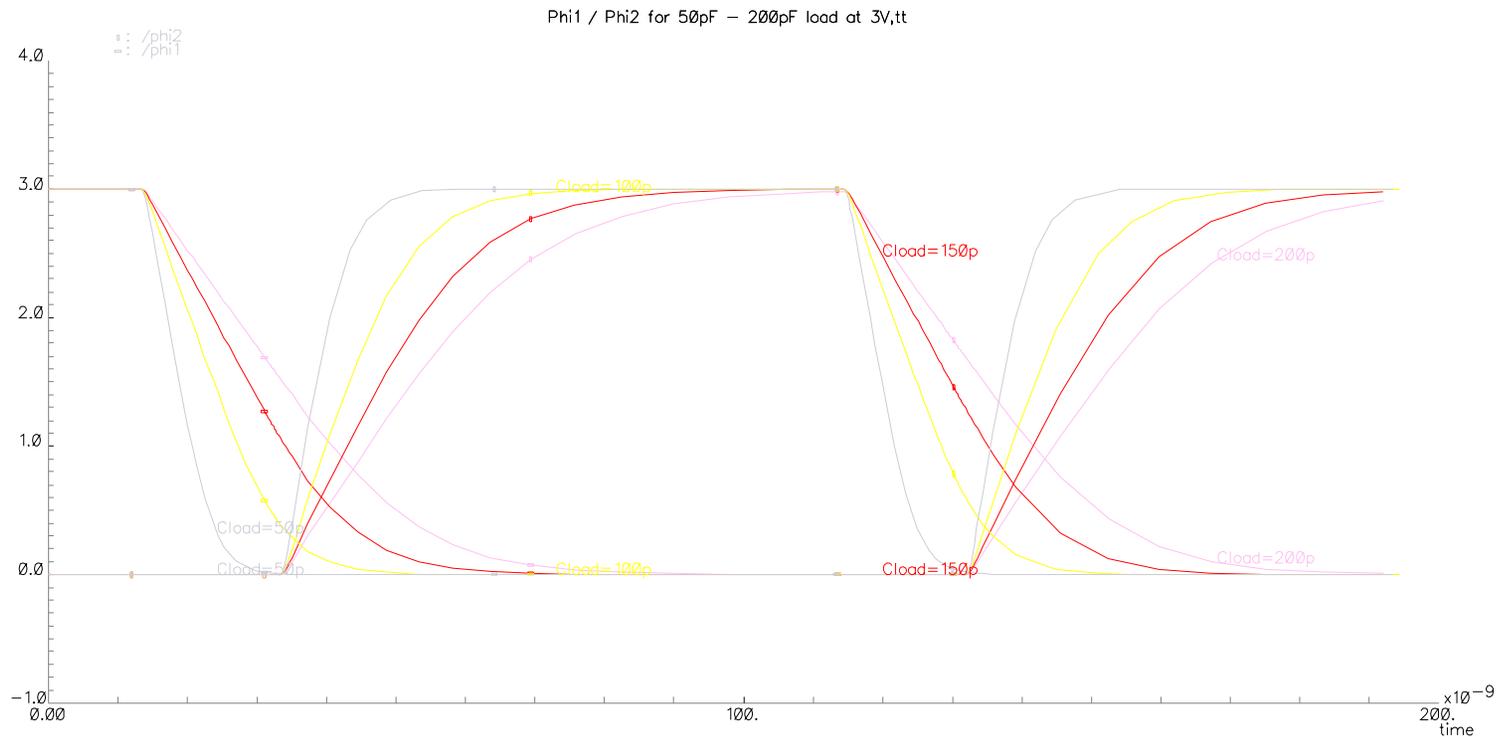
- Observe similar risetime, with non-overlap time of only 15ns. In this case, it would not be surprising if sometimes some register bits did not work, since if the two clocks overlap, a given register bit becomes “transparent” and is not written.

- Simulations from Peter for different VDD and a fixed 100pF load:



- Indicates that the risetime does seem to improve with larger VDD, but only slightly (it increases from about 15ns to 20ns for 3V to 4V). This may not be inconsistent with the measurements.

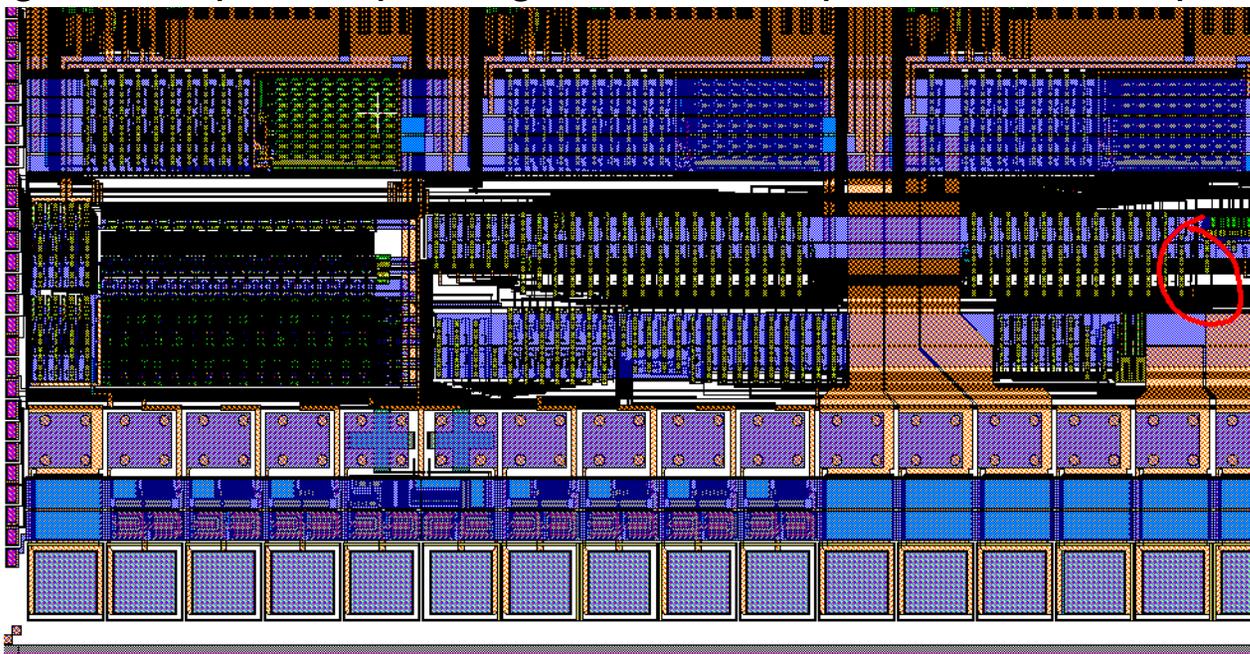
• Simulations from Peter for different load at a fixed VDD:



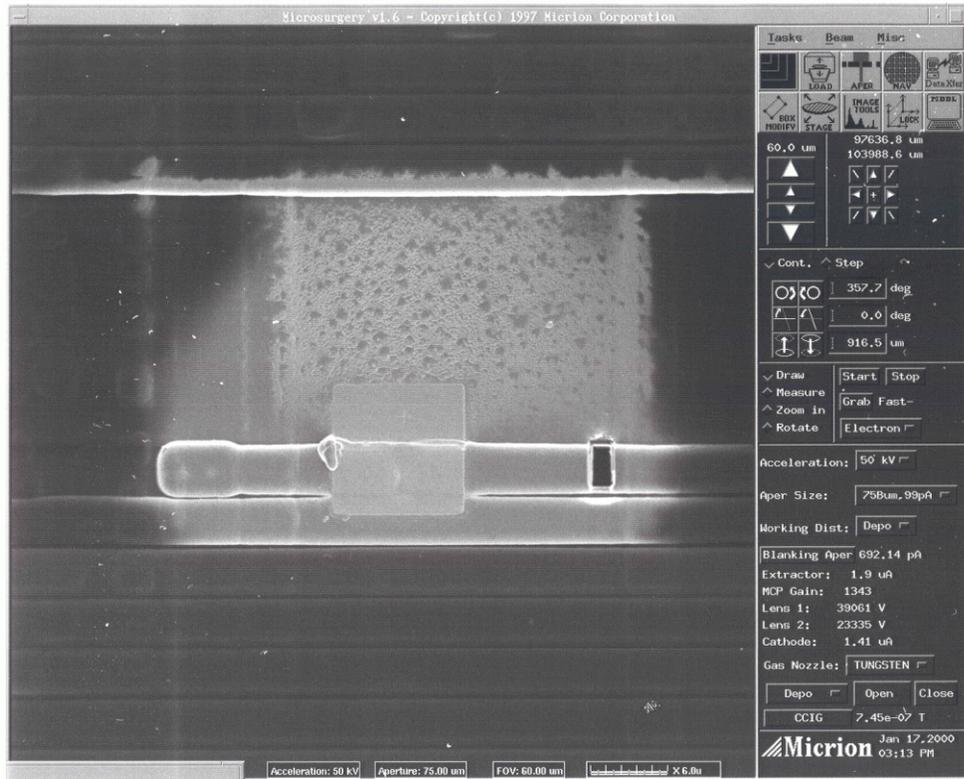
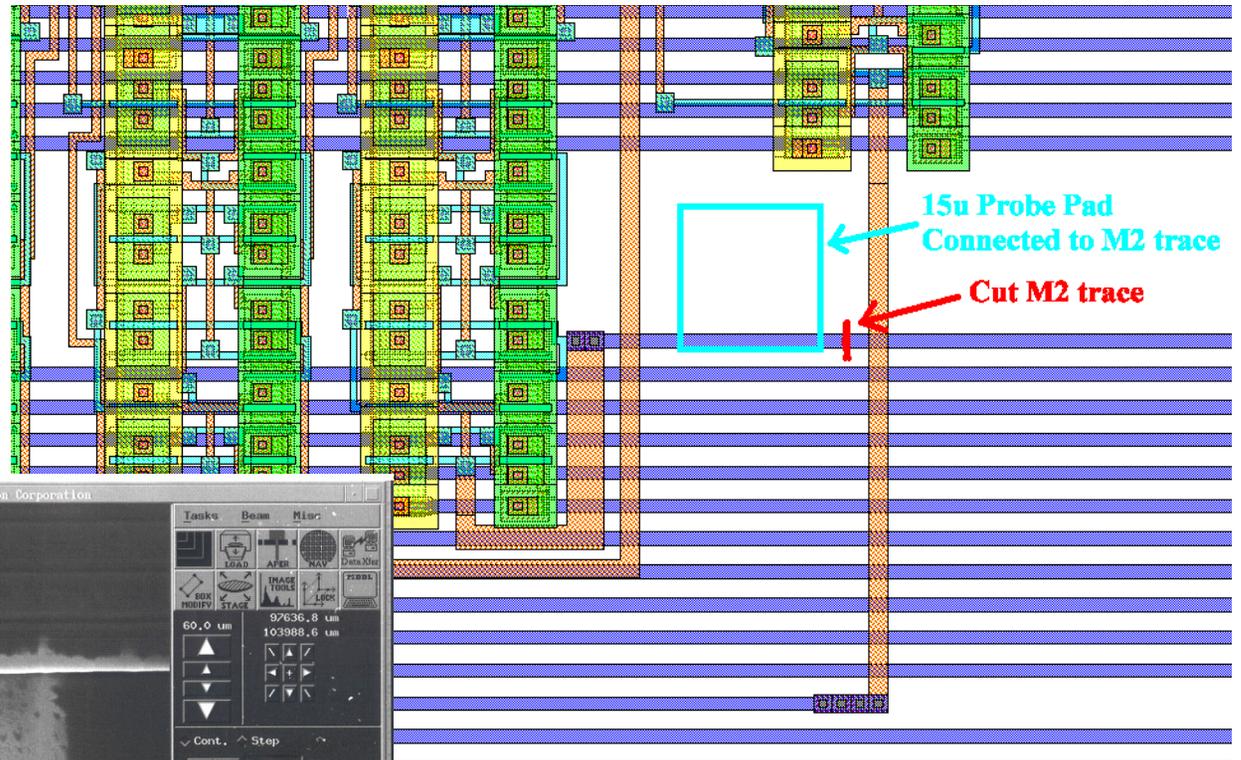
- Here, the comparison should be made for something between 150 and 200pF, but for a larger supply voltage. For VDD=3V, the risetime is in the range of 40-50ns. This could be closer to 30ns for the larger VDD.
- Although the curves are not exactly for the expected conditions in FE-D, the shape as well as risetime for the 200pF curve, perhaps adjusted slightly for the higher VDD, seems to be consistent with what is observed.
- Estimate buffers need to be resized by almost a factor ten to work well postrad.

Measurements and Simulations of SDO:

- This signal is the output from the serializer (unbuffered from a minimum size FF) to the Output MUX. The extracted capacitive load on this node is about 1pF.
- This point can be observed in FE-D on the pad labeled “Direct<3>”, which is one of the MUX inputs. There is clearly a severe problem with buffering on this node.
- After seeing this signal, hypothesized that this node alone could be responsible for the need to run FE-D at a VDD of 4.8V in order to observe correct output data.
- In order to study this in more detail, FIB surgery was performed on several die. The modification consisted of cutting the long SDO trace close to its source, and creating a small pad for probing with a low capacitance active probe:



- The actual modification was implemented as follows:

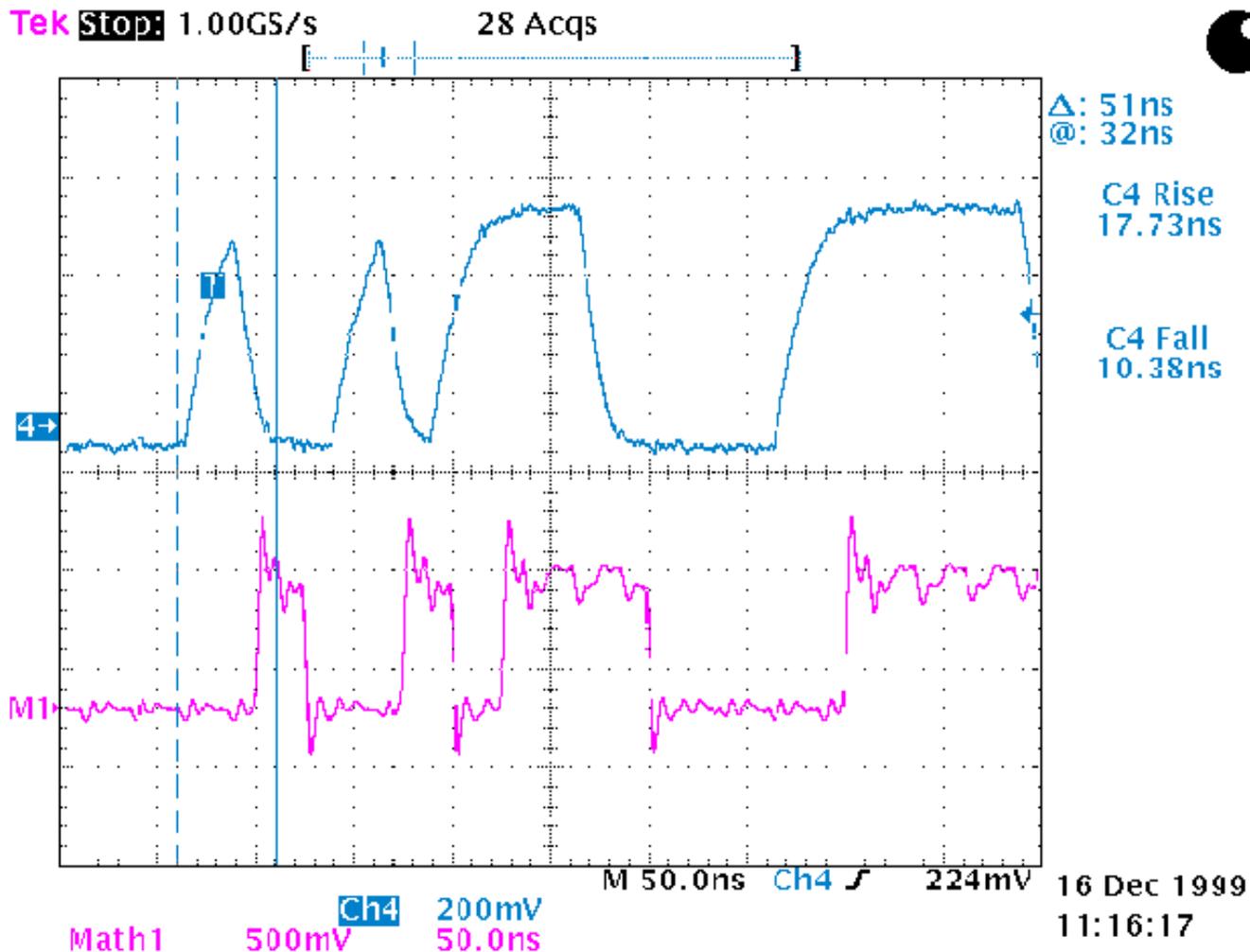


First, cut two holes in passivation. One is for the pad to access the M2 trace. The second is to cut the M2 trace.

Second, deposit the pad as 2000Å of W, 10µ square (about 15 mins).

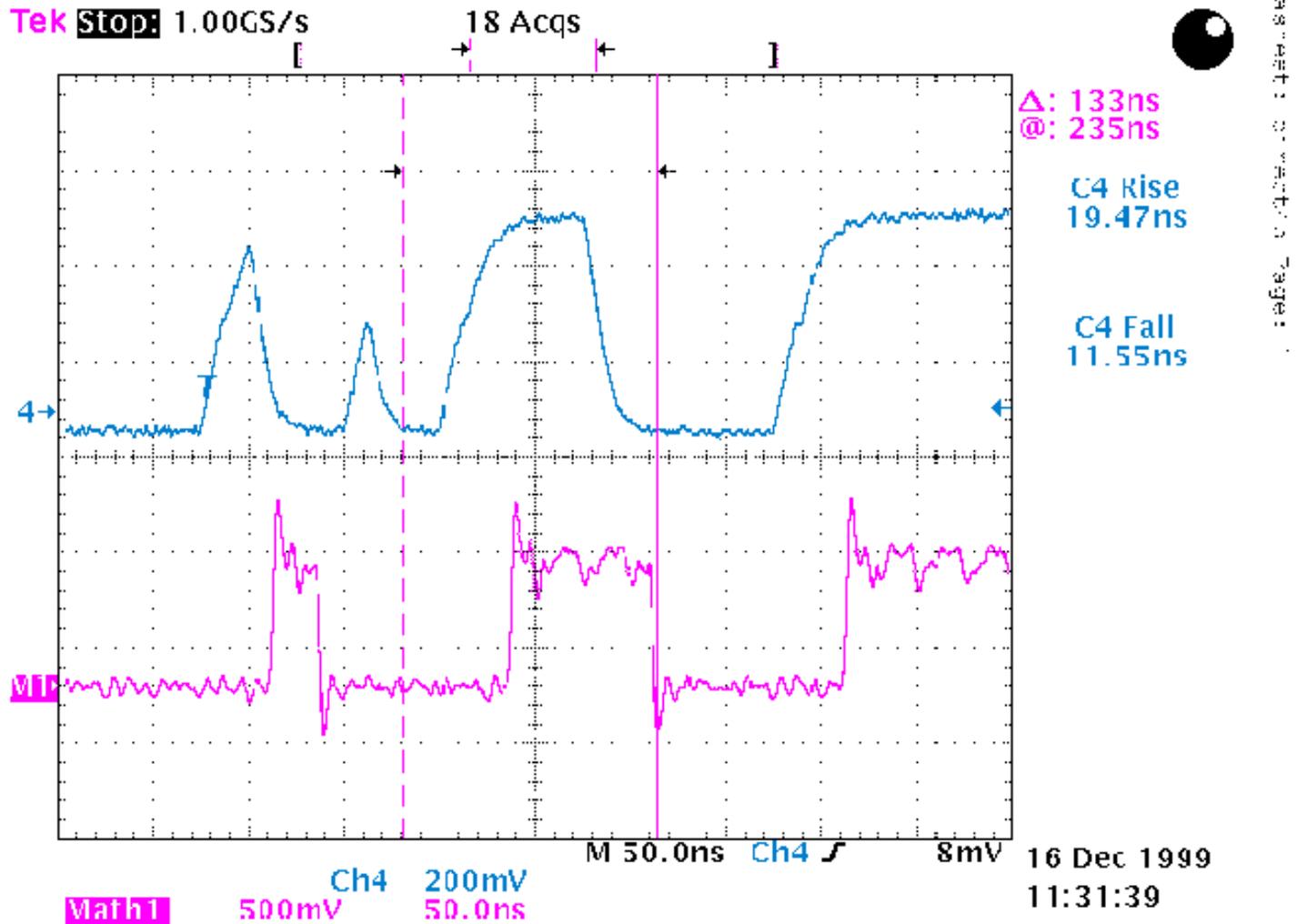
Finally, complete the cut of the M2 trace.

- Measurements made on unmodified chip as a function of the supply voltage:



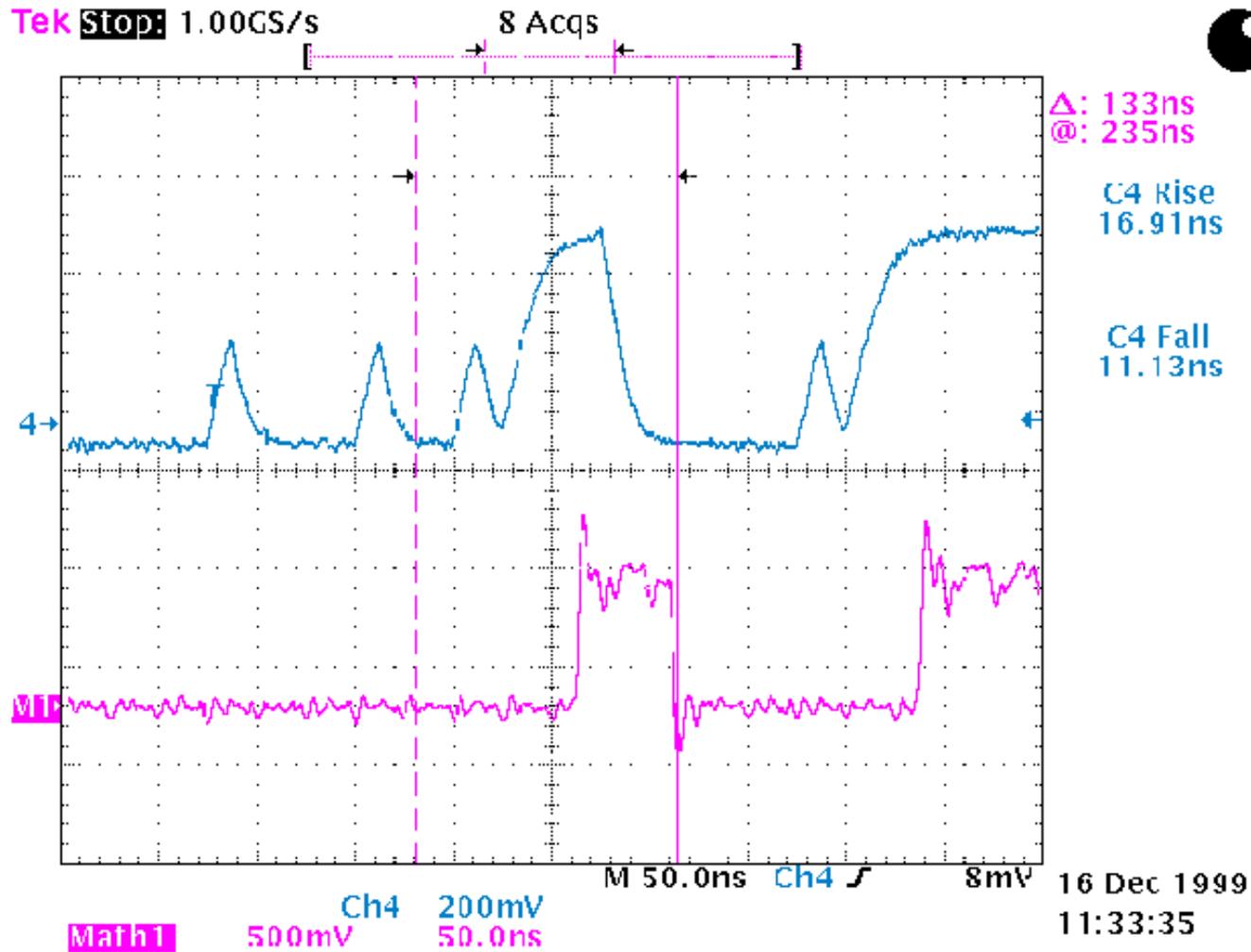
- These waveforms are at $V_{DD}=4.8V$. The upper one is SDO, the lower one is the DO output from the chip. Here, no bits appear to be lost, but the risetime is 17ns on a 40 Mbit data stream, which is clearly very marginal.

- Measurement of waveforms at 4.5V VDD, showing a bit lost:



- This indicates the basic failure mode: when there is not enough drive strength in the FF, it no longer sets a “1”, and the output width is only half the expected one, which dramatically reduces the pulse amplitude.

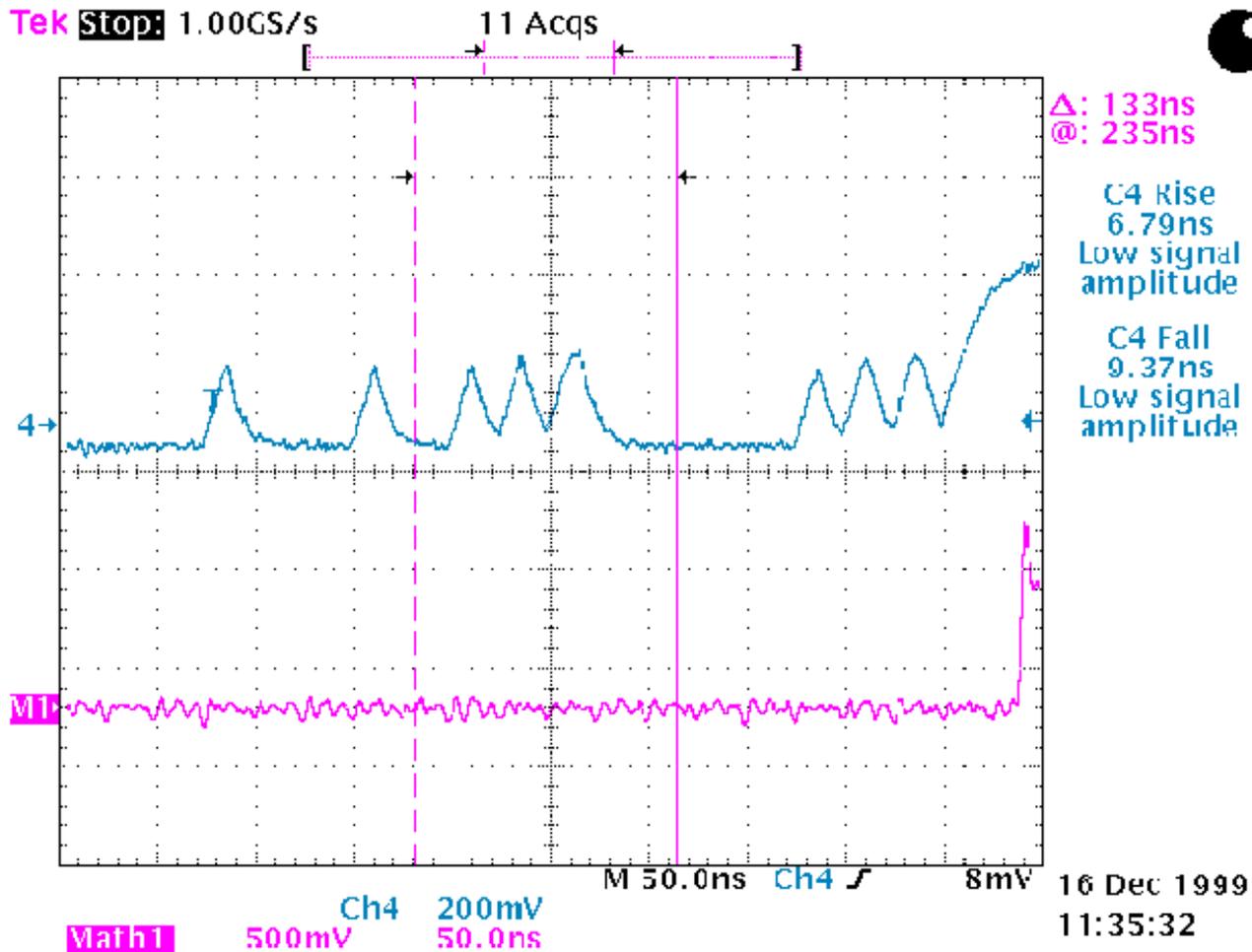
- As VDD is reduced to 4.3V, the waveform already looks worse:



Parameter: 0x00000000 Page: 1

- Now, all of the “narrow” bits (isolated “1”s) are being lost.

- At a lower VDD of 3.7V, things look even worse:

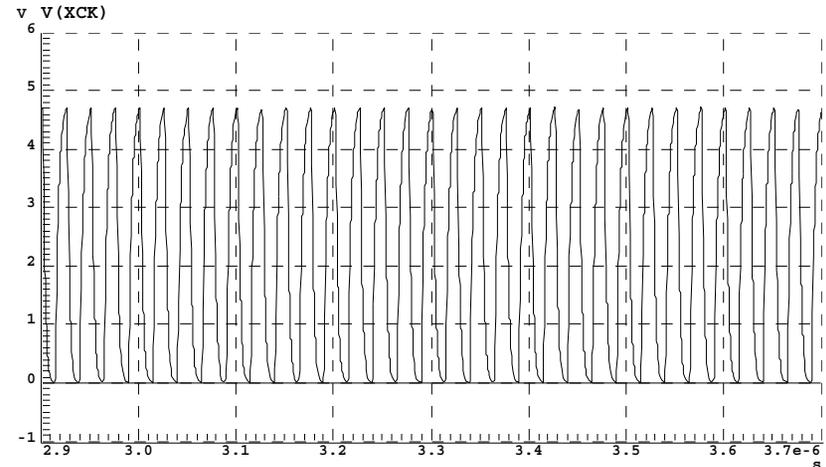
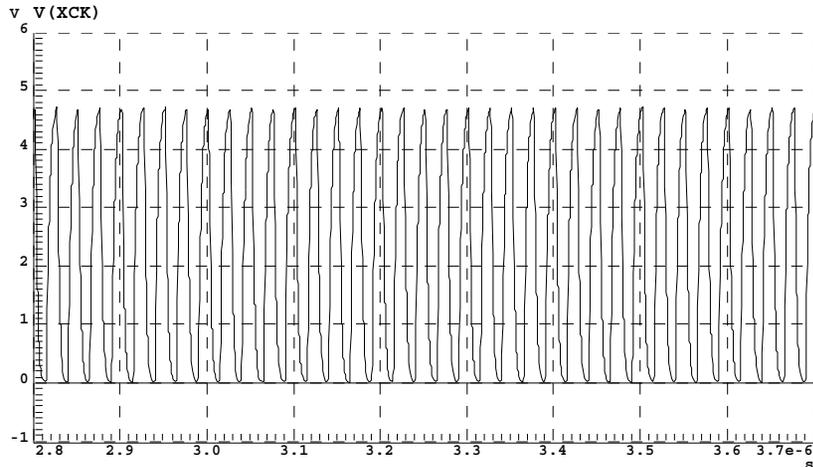
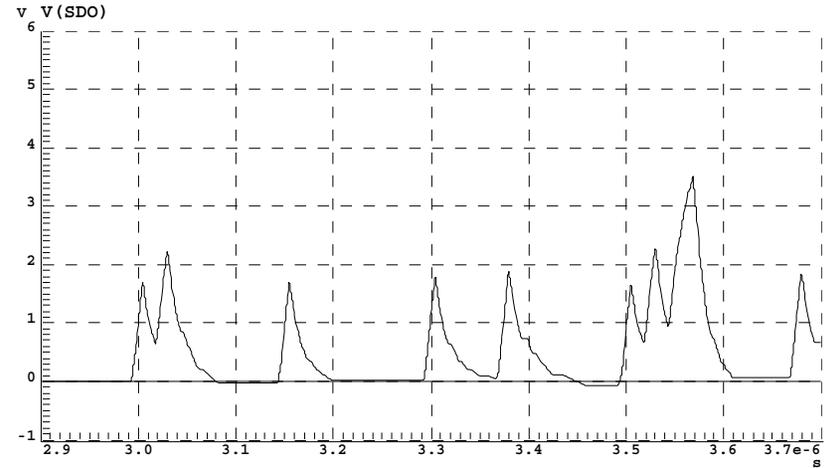
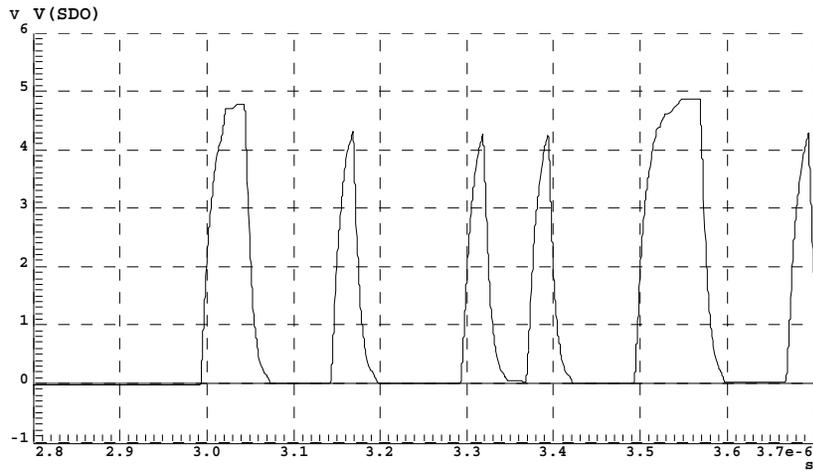


- Now, even the strings of “1”s have been broken up into shorter spikes, and most bits are lost from the output.

- Simulations were done with a single capacitor to ground placed on the SDO output in the netlist, at both VDD=4.8V and 3.5V:

7-Jan-2000 File : top160sdo.cou
06:06:04 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/VT

8-Jan-2000 File : top160sdo48x.cou
07:36:51 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/VDD/DI

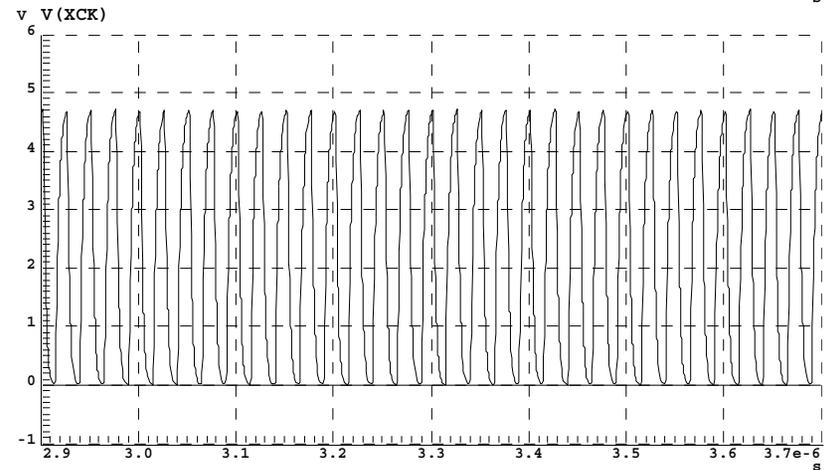
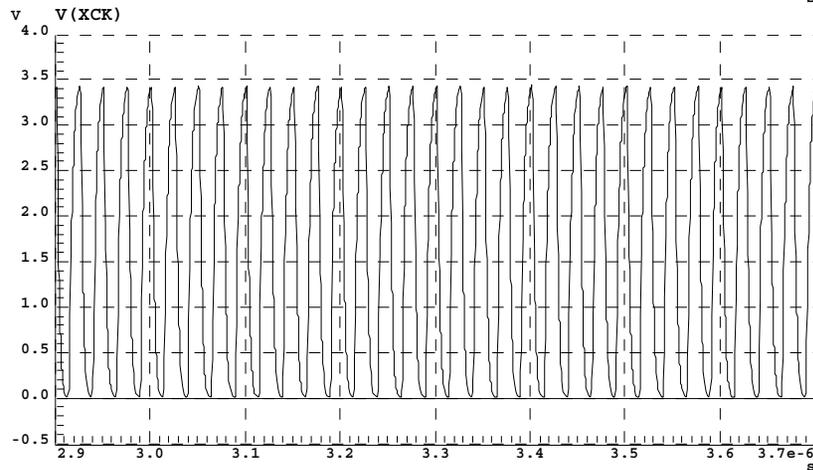
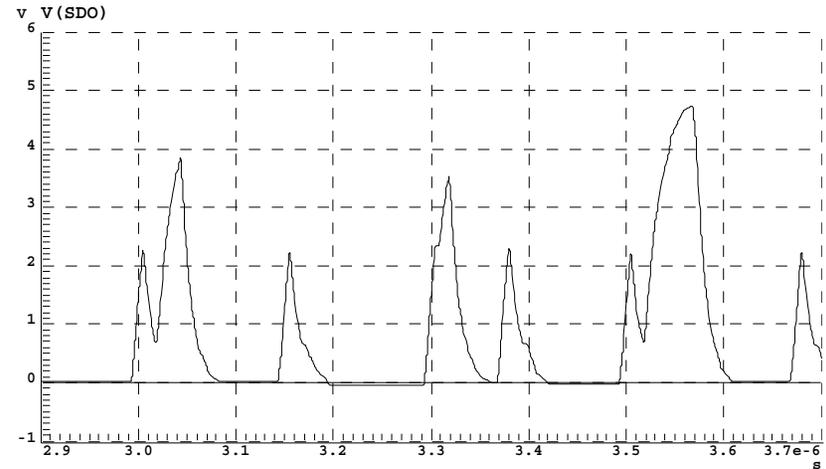
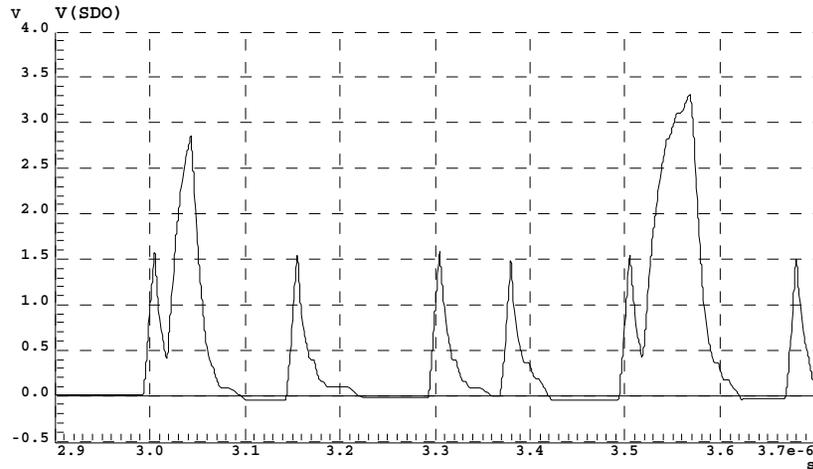


- The left simulation is at VDD=4.8V, and C=1pF. The right simulation has C increased to 2pF. There is clearly significant bit loss for the larger capacitance.

- For a C of 1.5pF, it looks as though there will be bits lost at both VDD=3.5V and VDD=4.8V, depending on the switching point for the Output MUX block:

10-Jan-2000 File : top160sdo35y.cou
 13:52:08 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/V

8-Jan-2000 File : top160sdo48y.cou
 17:54:58 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/VDD/DI

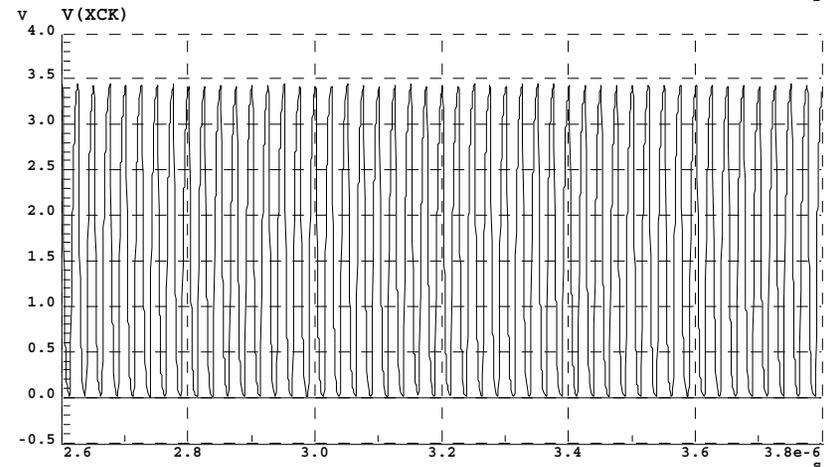
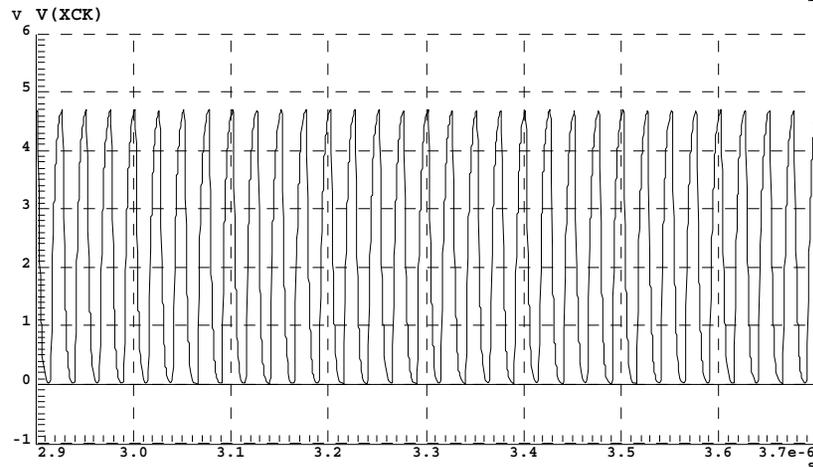
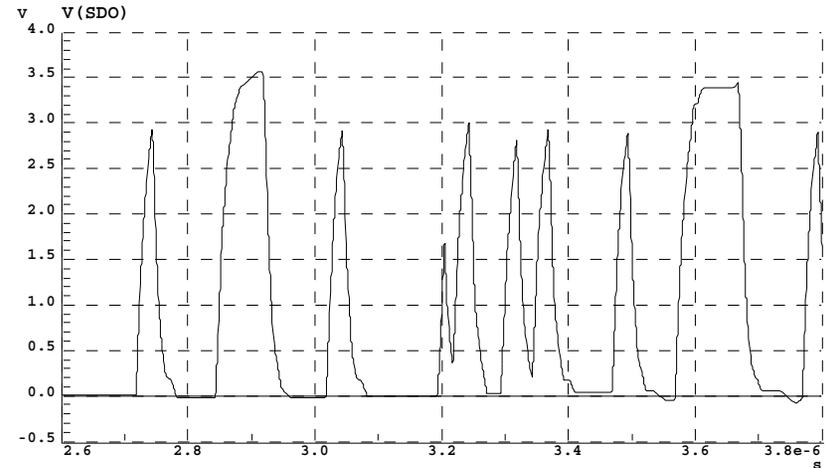
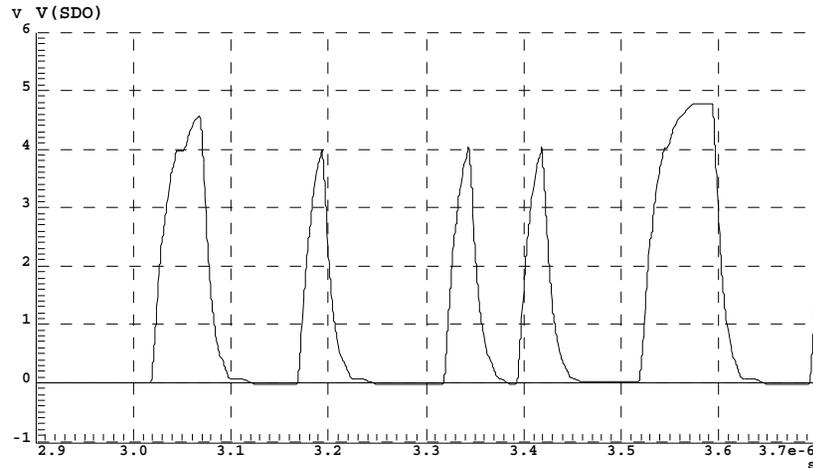


- Unfortunately, Global Register was not properly set for these simulations, so the Output MUX was not passing SDO to the output.

- For a C of 1.25pF, there appears to be a point where VDD=4.8V works and VDD=3.5V loses at least some bits:

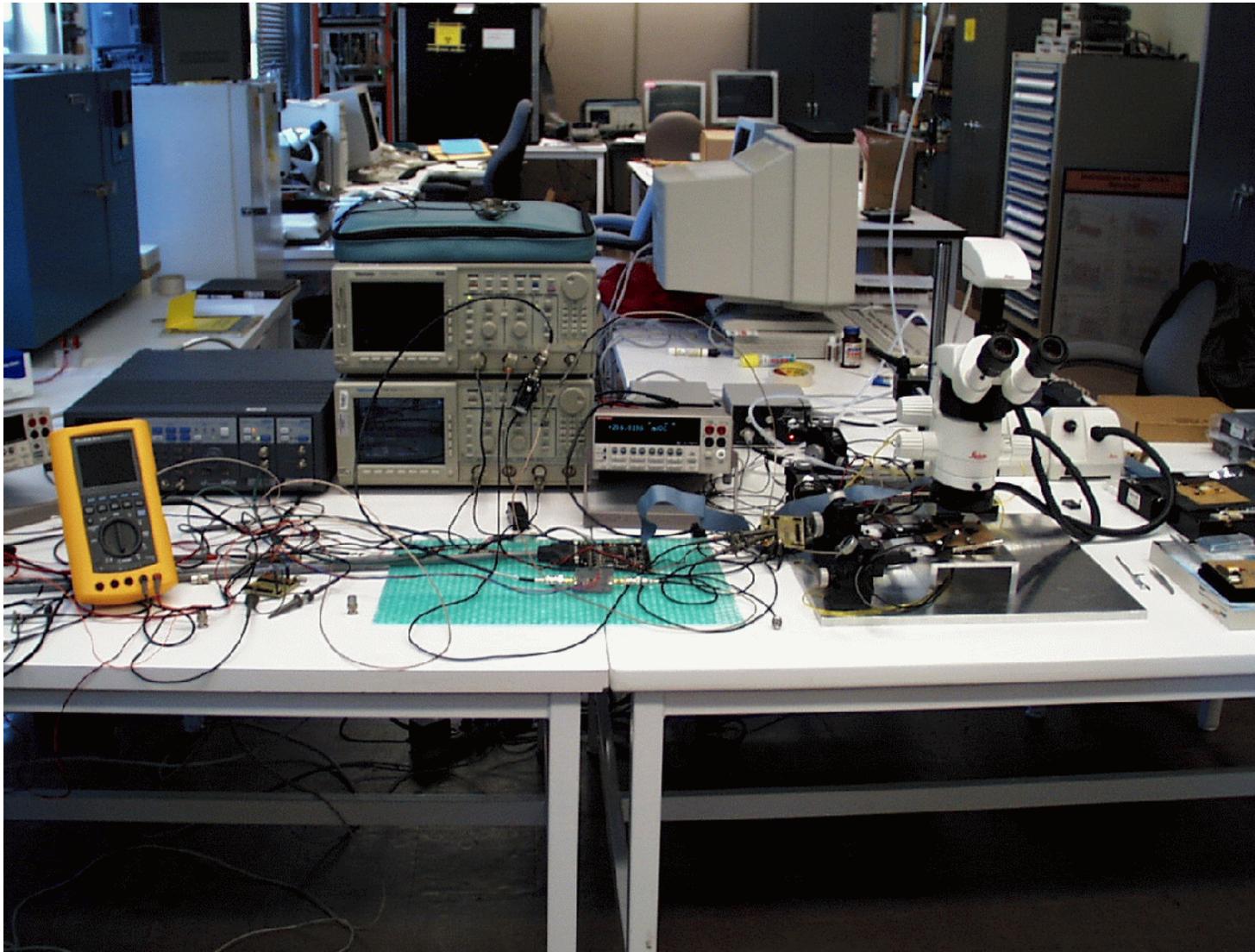
10-Jan-2000 File : top160sdo48z.cou
09:02:22 ELDO v4.7_1.1 (production) : * # FILE NAM

10-Jan-2000 File : top160sdo35z.cou
22:54:23 ELDO v4.7_1.1 (production) : * # FILE NAME: /HOME/VDD/D:



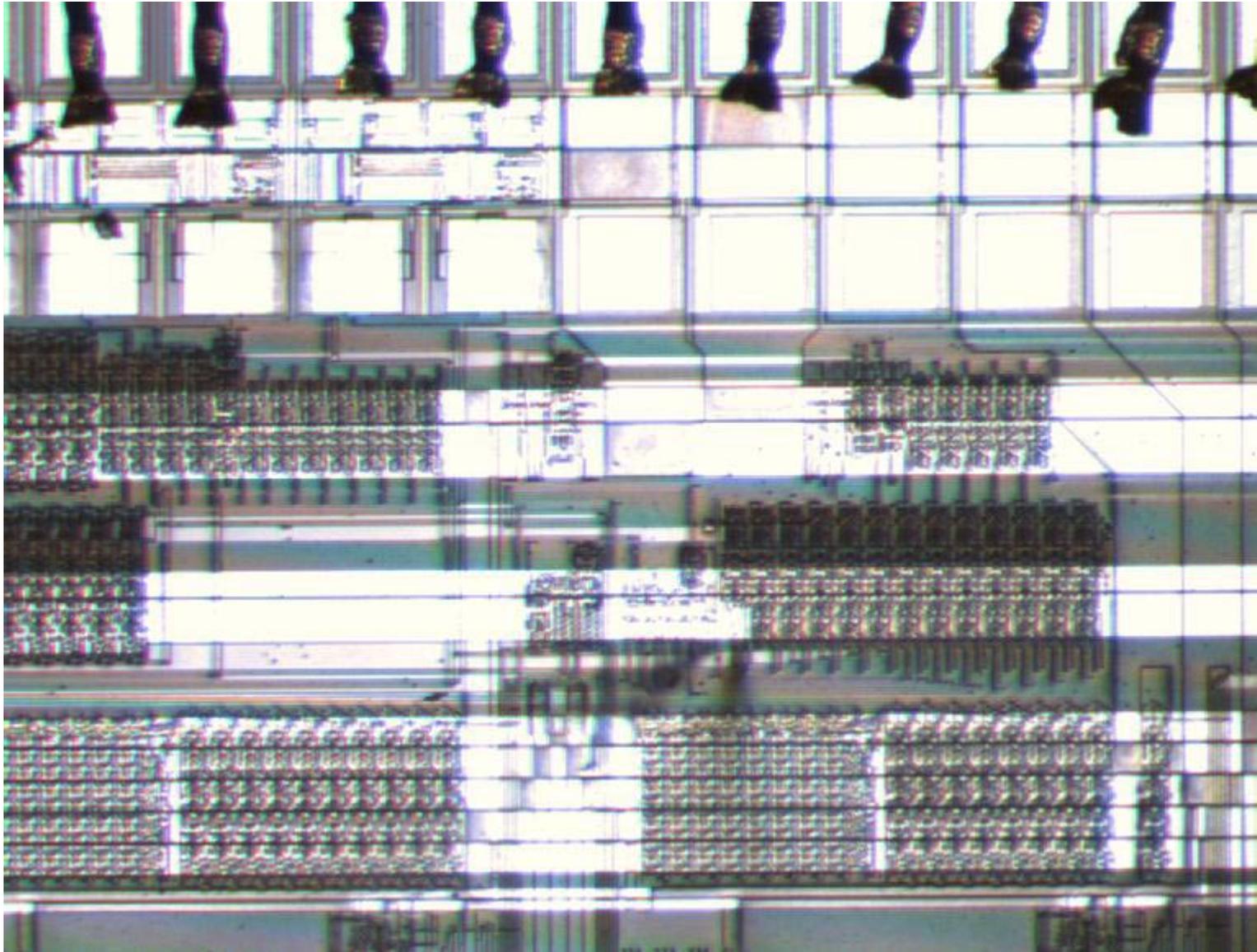
- Finding this point requires fine-tuning the capacitive load, and the VDD dependence does not seem to be very large (different from measurements ?)

Measurement Setup:



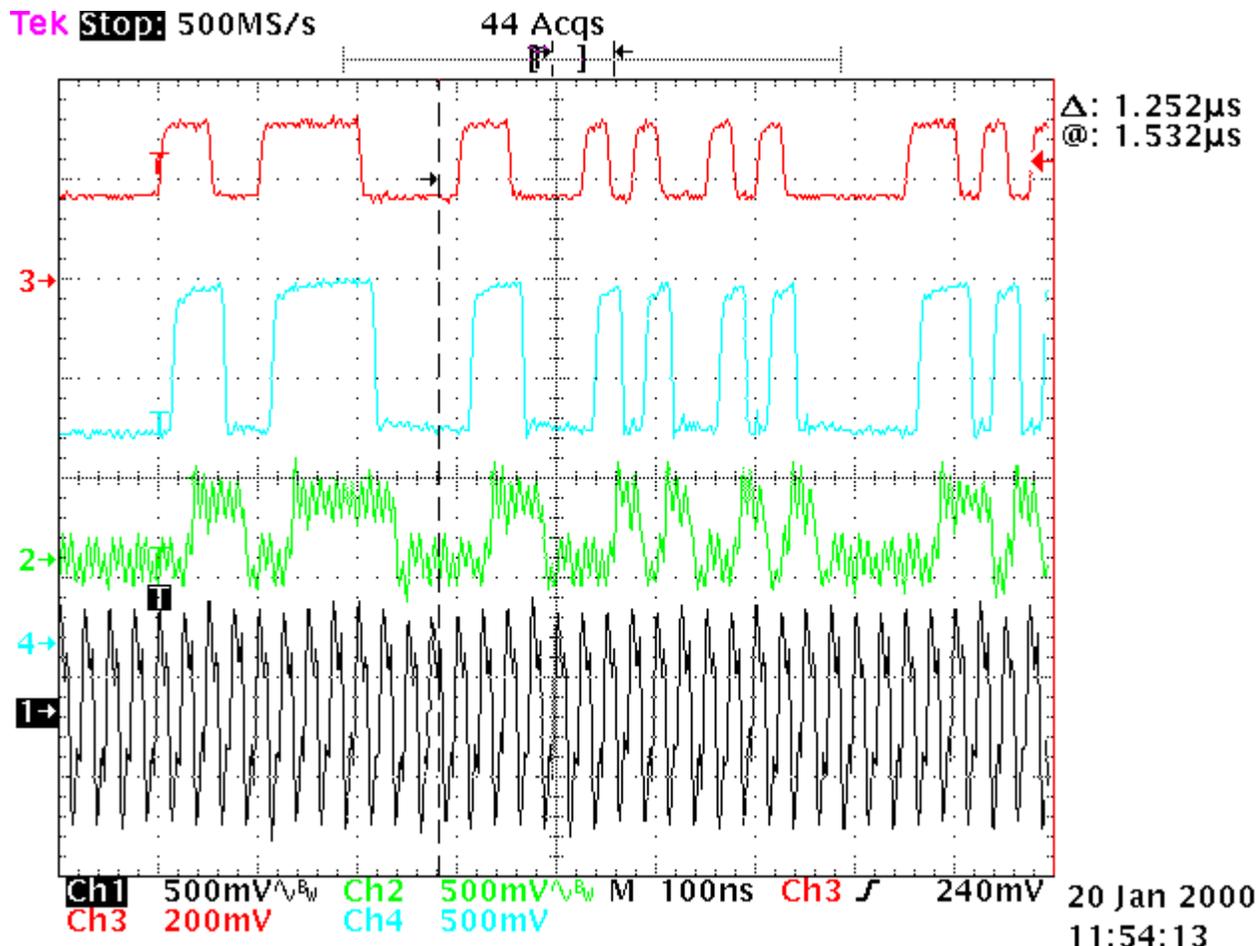
- Picoprobe readout and offset adjust, fast AD8009 buffer in 10x mode, then return to modified support card for CMOS->LVDS conversion and transmission to PCC.

Probe point as seen through optical microscope in lab:



- Tiny pad just visible in middle of image, next to serializer...

•Results for serializer output from FIB-modified die:



- Top trace is SDO from new probe pad, with risetime of 2-3ns. Risetime is much improved with expected load of about 200fF.
- Second trace is amplified version of SDO (after AD8009 fast buffer).
- Third trace is LVDS version of DO, picked off of breakout card on cable to PCC.

•This allows us to take the (largely) unloaded SDO directly from the chip, amplify it, adjust the DC offset, convert it back to LVDS, and transmit it to the PCC (after adjusting the timing relative to XCKR on the same cable). The resulting serial stream is correctly interpreted by the PLL, allowing full testing with PixelDAQ.

- The result is that the modified chip now operates at $V_{DD}=3.0V$ and $sensebias=4$, with the column clock operating at 20MHz. However, already at 2.9V, there starts to be a loss in digital injection efficiency in some regions of the chip.
- At 3.0V, digital injection works efficiently down to $sensebias=2$. Lower senseamp biases cause the loss of hits in certain regions of the chip. The chip operates slightly better with a column clock frequency of 10MHz.
- Basically, this seems to confirm that the digital readout, with the exception of the SDO buffer problem, will operate properly at $V_{DD}=3.0V$ before irradiation (but it is quite marginal). However, there is no improvement in the bad pixels, etc., so these problems are not artifacts of the high V_{DD} required for operation of the serializer.
- Clearly, a real buffer is needed after the serializer, due to the long trace routing to the output MUX.
- In general, we need to go through each of the circuit blocks at the bottom of the chip, and systematically check that there is appropriate buffering between each block. As a rule, we should never use the unbuffered outputs of FF outside of local circuit blocks.