

FE-D Digital Readout Testing and Next Steps

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Initial FE-D testing done at Bonn, and summarized already:

- Many results on performance of analog blocks in chip

Second phase of testing done at LBL, using diced and modified parts:

- First probing survey of complete wafer
- More detailed study of digital readout
- More systematic analog scans of chips done by Markus, Mario, and John

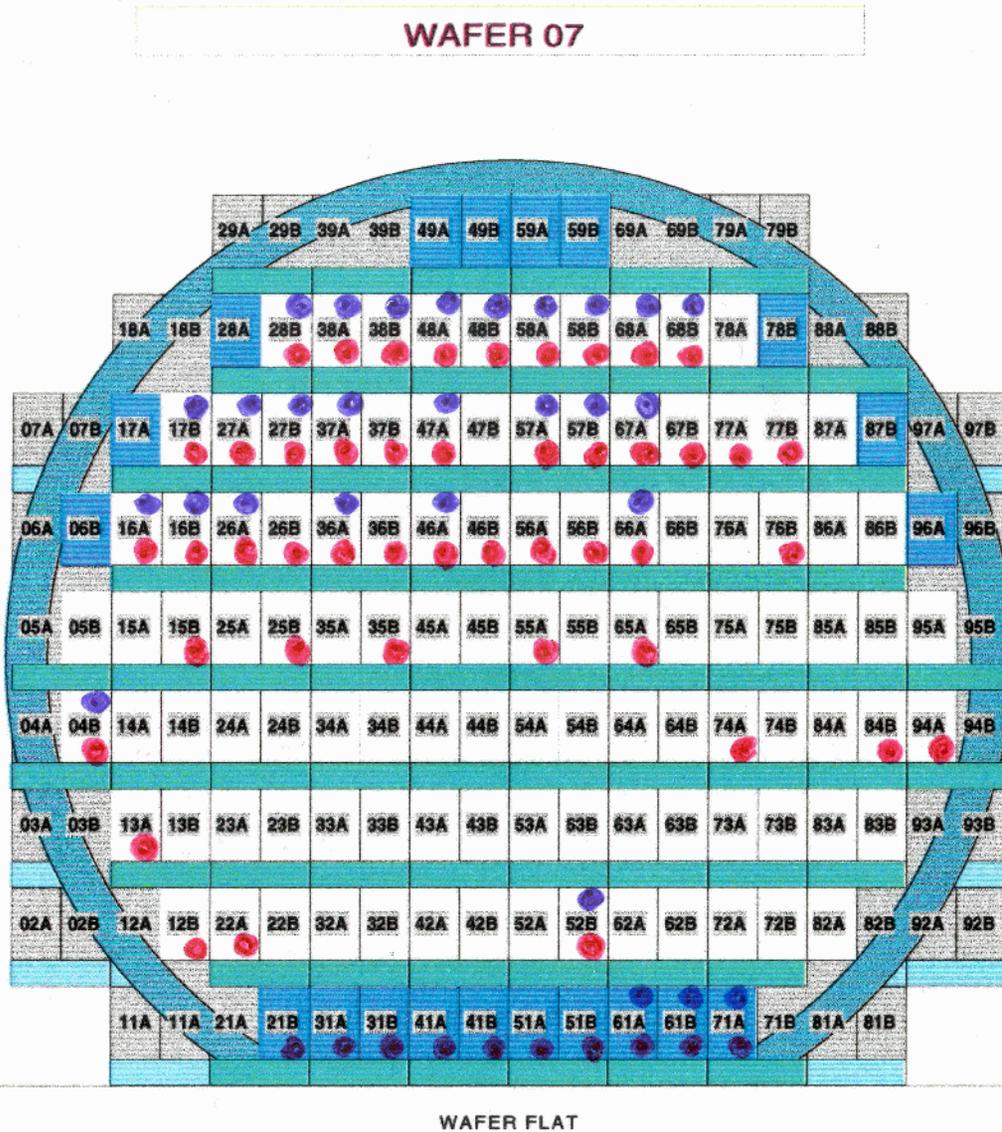
Conclude with some first thoughts on next steps:

- Additional testing and simulation work
- Probe more wafers and send one each to Alenia and IZM
- Organize work for re-submission

Wafer Probing of Wafer#7

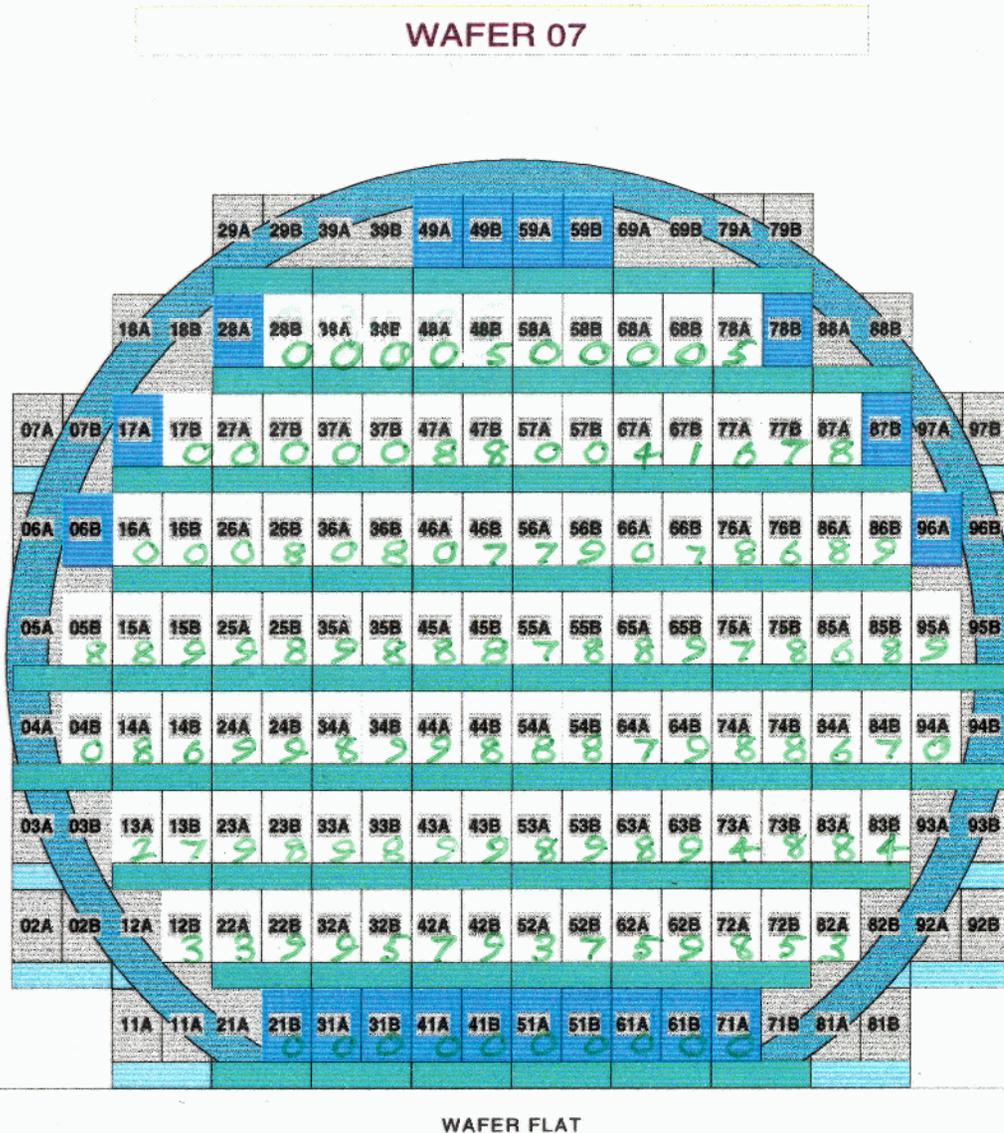
- Operation of Wafer#7 on probe station required significant increase in VDD to avoid problems with EOE word corruption when sending event data. PixelDAQ was modified to perform wafer probing at two voltages. Here used 3.5V and 4.8V. Recall design of FE-D was to operate properly after full radiation dose at 4.0V.
- First performed write/read Global Register test on all 106 potentially good die sites. A total of 25 die failed this test (yield 76%).
- Next observed that most die failed test of Pixel Register. The test was modified so that each column pair was tested individually (using the column enable bits), and the number of good column pairs was determined. This good column pair mask was used in subsequent testing of the die. A total of 22 die had all 9 column pairs working, for a yield of only 21%.
- Finally, digital injection tests were performed on the die. The only requirement was that there were not large numbers of data corruption errors (invalid row/column/TOT values in the received hits). This eliminated a few more die. This test alone has 45 die fail only this test, and there is a fair correlation with failures of the Global Register test (yield 58%).
- The final yield after these three very basic tests was 20 die, or a 19% yield. The distribution of good die was very non-uniform over the wafer.

Wafer Maps



- Blue circles represent chips failing Global Register test.
- Red circles represent chips producing corrupt or missing EOE words during digital injection.
- The distribution of failures is heavily biased towards the upper half of the wafer.
- Any die overlapping the exclusion region appear to be bad.

Wafer Maps

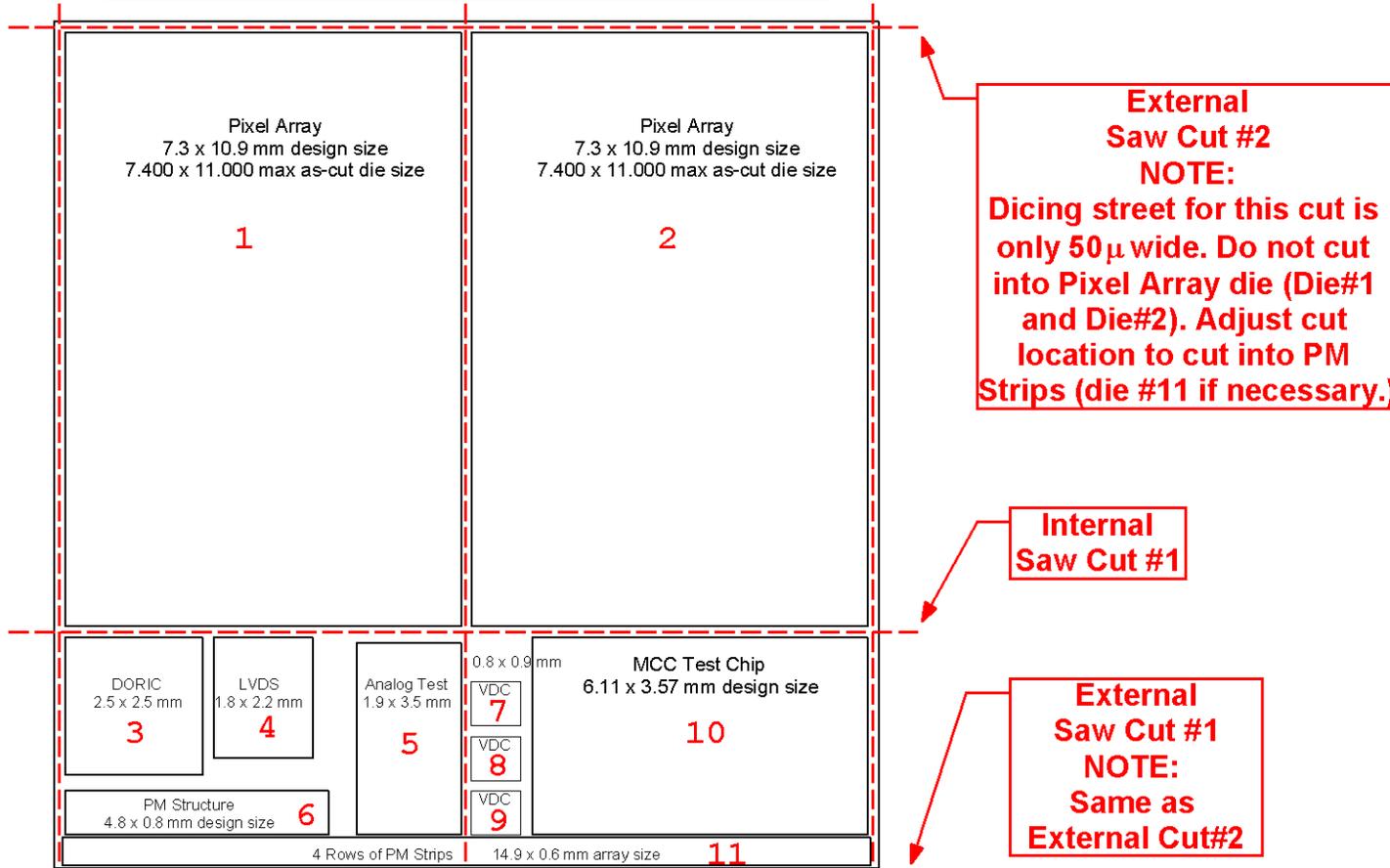


- Number of column pairs passing the Pixel Register test.
- Again, the distribution is very non-uniform.
- There were fifteen good die in the lower half of the wafer. This region was selected for dicing.

Dicing of Wafer #7

- Carried out complete dicing of the lower part of the wafer:

DMILL Reticle Layout (drawn to scale, 200u gap between designs)



External Saw Cut #2
NOTE:
 Dicing street for this cut is only 50μ wide. Do not cut into Pixel Array die (Die#1 and Die#2). Adjust cut location to cut into PM Strips (die #11 if necessary.)

Internal Saw Cut #1

External Saw Cut #1
NOTE:
 Same as External Cut#2

External Saw Cut #3

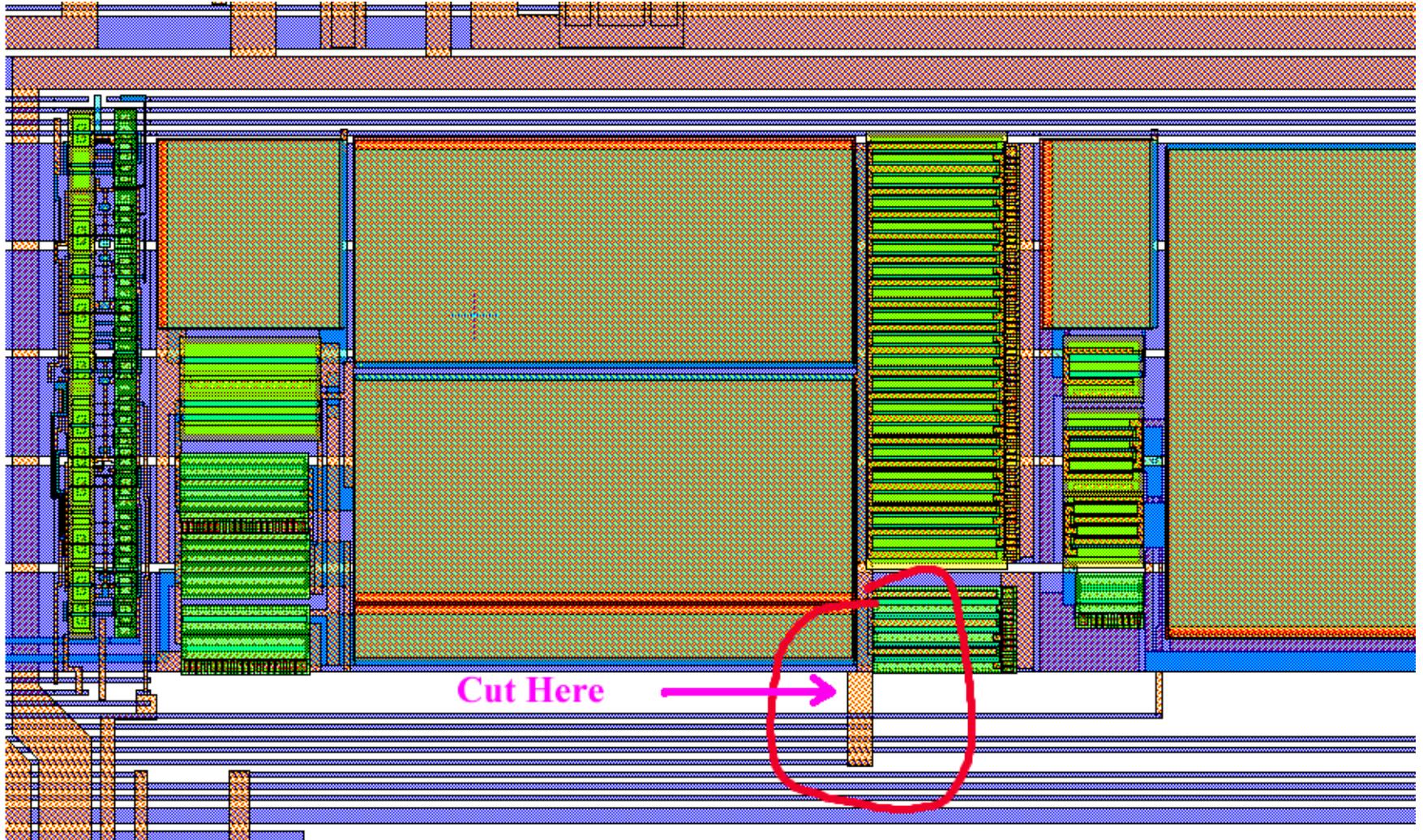
Internal Saw Cut #2

External Saw Cut #4
NOTE:
 Same as External Cut#3

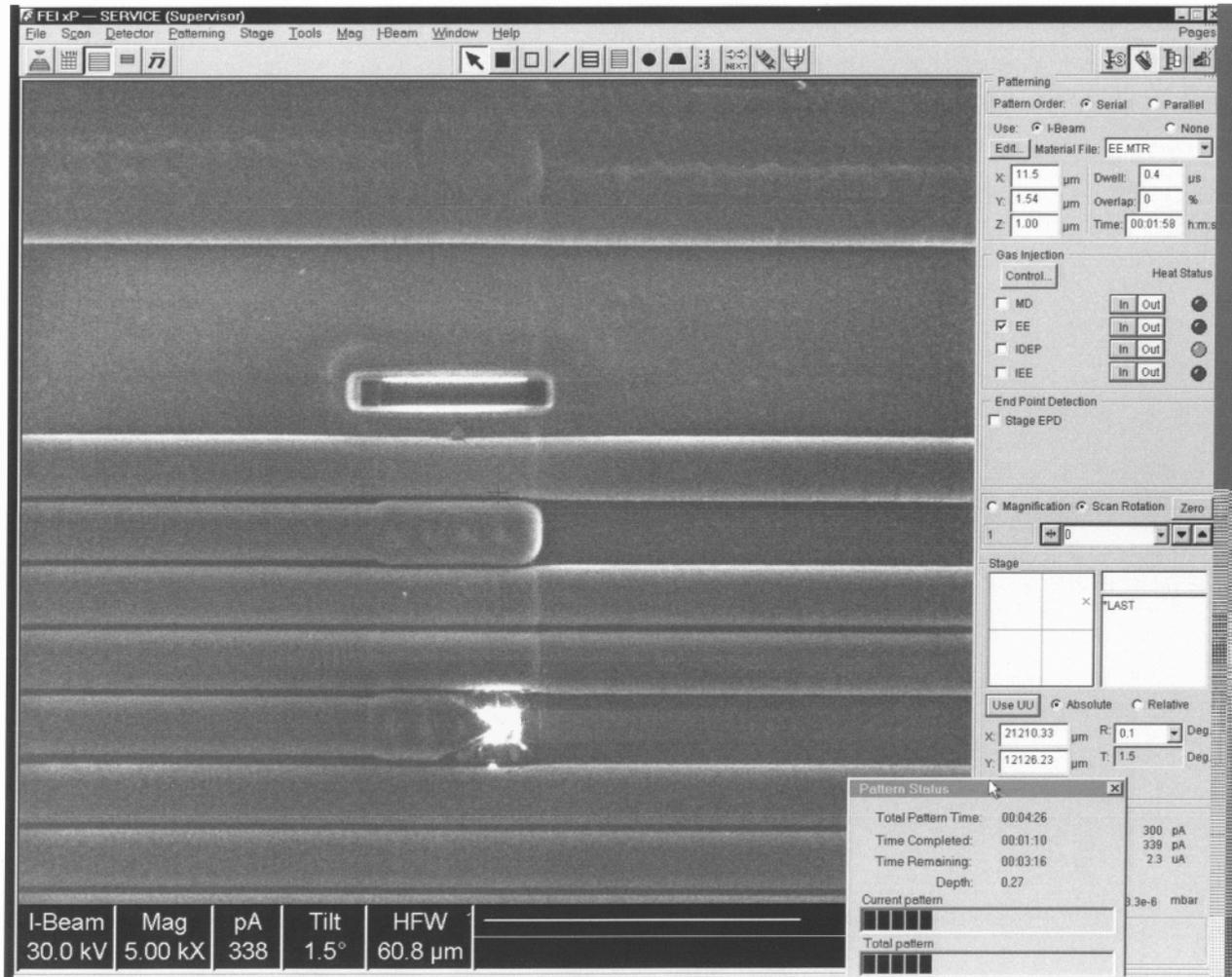
Nominal Rules:
 * Metal1 and Metal2 scribe lines define design size (distance between metal scribe lines)
 * Different designs are separated by 200μ gap between scribes. Reticles are separated by 220μ gap between scribes.
 Reticle stepping increments are: 15.02 (W) x 15.38 (L) mm.

FIB Modification of Wafer #7

- Decided to completely dice the lower half of wafer #7, and to perform FIB modification on 15 die with 9 good column pairs in Pixel Register test in order to allow external supply of VTH for front-ends.



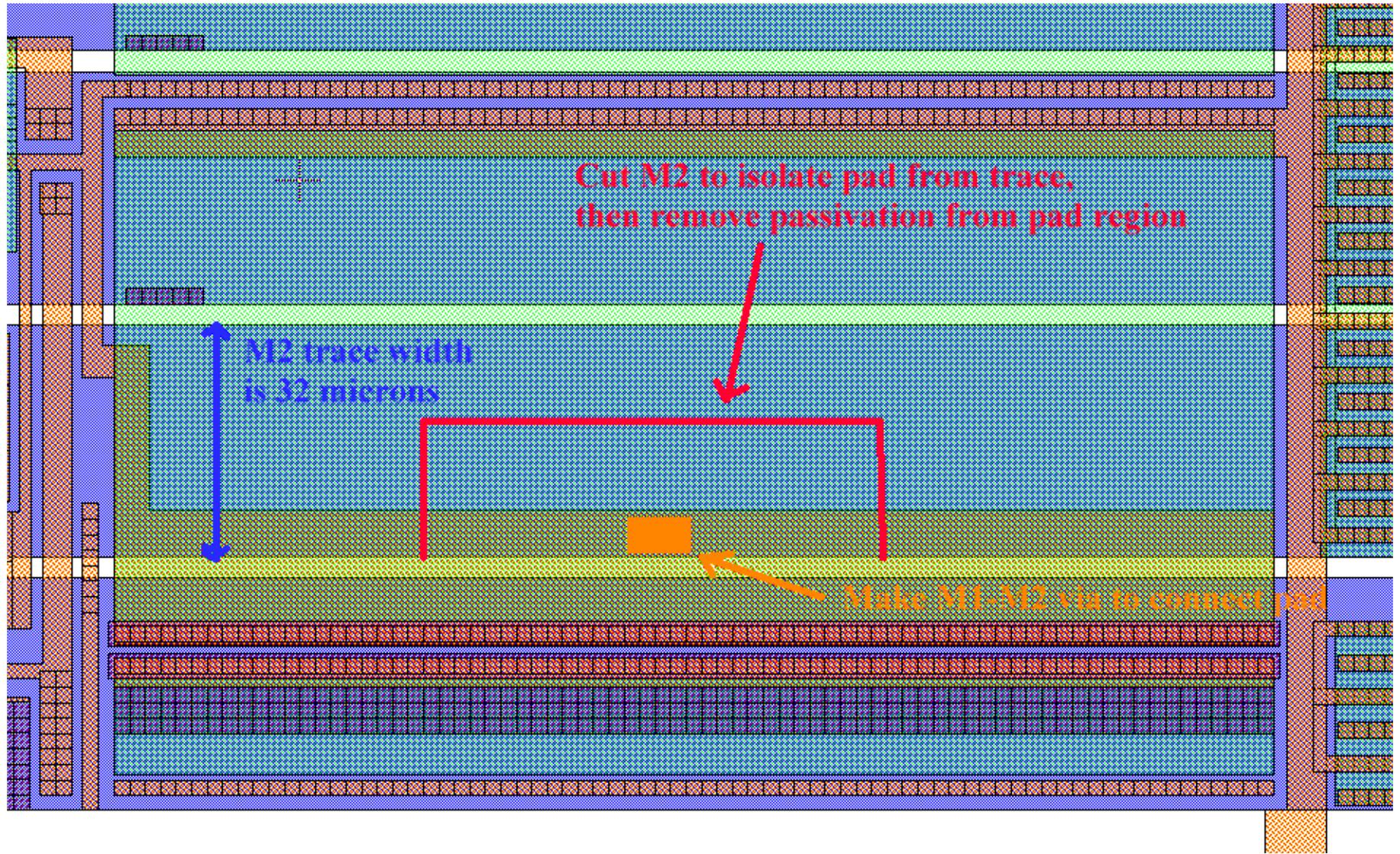
- Modification of each die took about 8 minutes on FIB machine at Accurel:



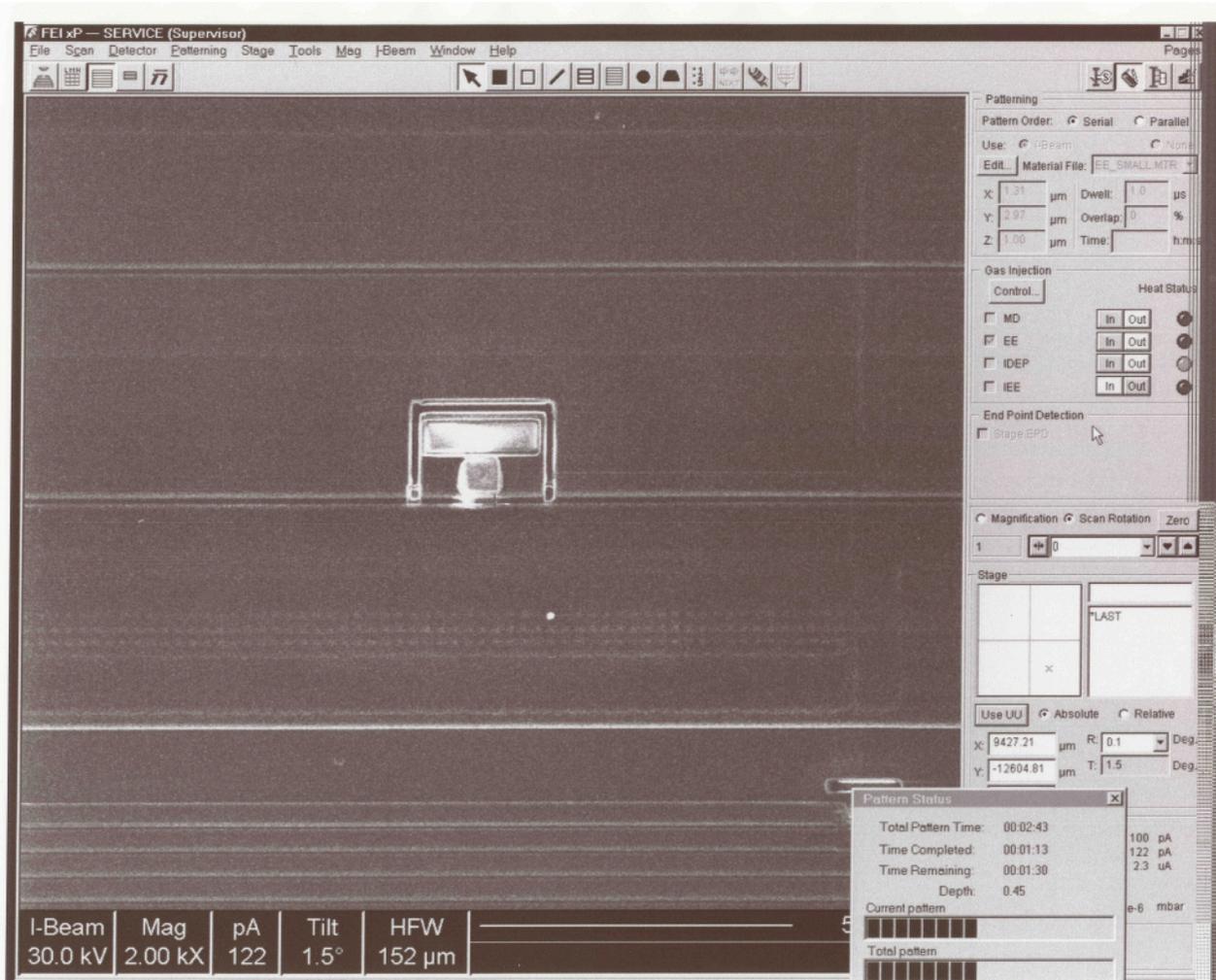
- Cut of approximately 11μ length was made through 9μ wide M1 trace.
- Under SEM, can see the Al remnants of the original trace as bright lines.

- This would suggest that a complete wafer with 106 die sites would cost about 4K\$, but we have not requested any quote information. Note the modification can be performed after flip-chip, since this region remains accessible.

- In order to evaluate further the present hypothesis about the fabrication fault, one die was modified to create a small pad for probing the gate of the output transistor of the VTH amplifier:



- This modification took considerably more time, and resulted in a 10μ by 20μ pad:



- First step was to cut out a small region of the wide M2 trace shown.
- Second step was to make a small via from this new pad down to the M1 trace underneath, by cutting and then depositing Pt via FIB.
- Finally, the passivation was removed to allow probing.

- Testing of this die has not yet been carried out at Bonn.

Distribution of die so far:

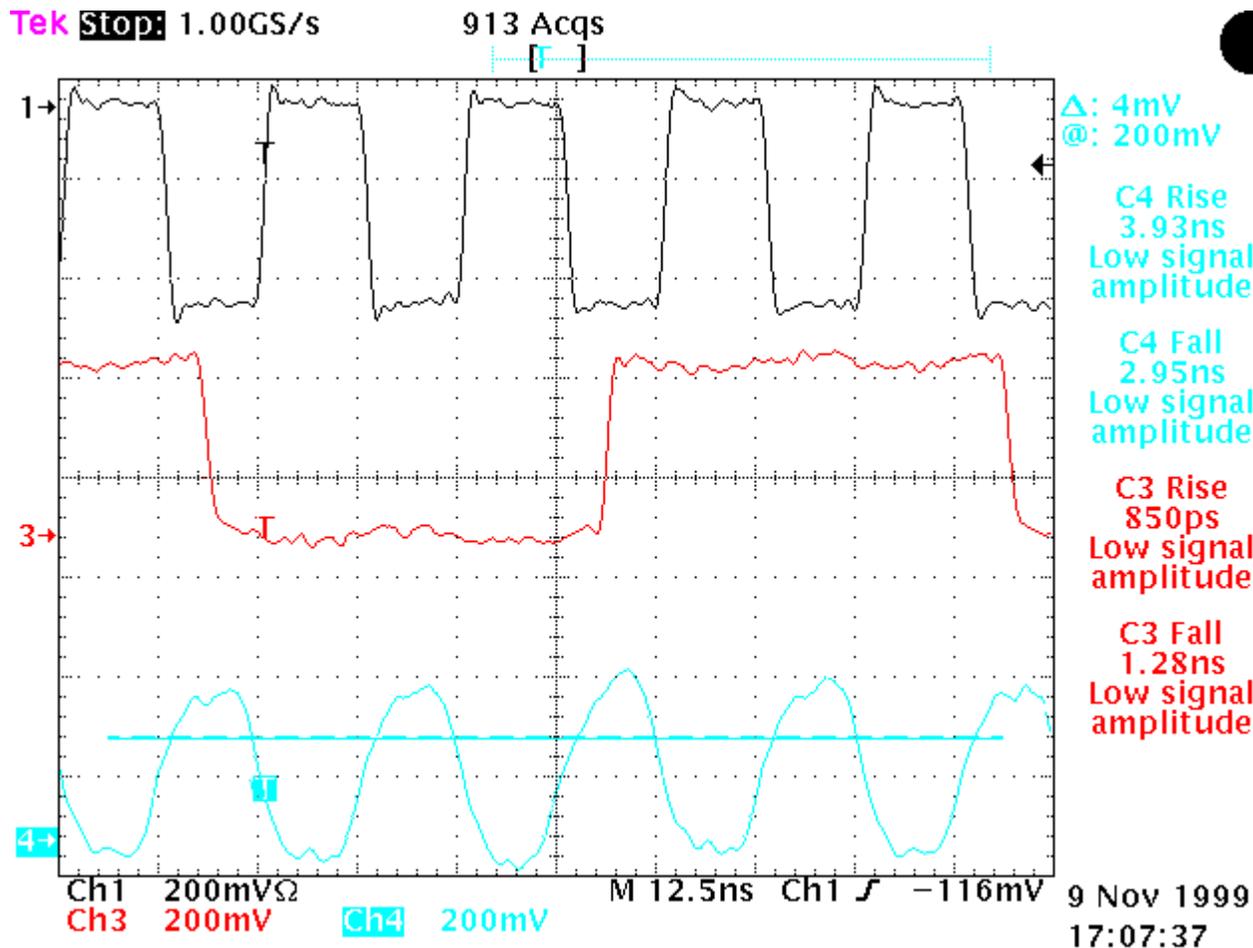
- Have sent 5 modified and 5 un-modified FE-D die to Bonn, as well as 5 analog test chips.
- Have sent 10 MCC-D0 prototype chips to Genova
- Have sent 6 DORIC and 12 VDC chips to both OSU and to Siegen.

Mounted 4 modified FE-D die on single-chip cards at LBL.

- Have looked at VDD dependence of chip operation. Find that operation of chips using digital injection and without data corruption (invalid field values in hits), as seen on the wafer level, requires about 4.8V for VDD.
- Have studied problems with XCK distribution in chip.
- Have examined other problems with command decoder. Main issue here was problem with WriteMask using the PLL. This was traced to be another side-effect of buffering problems in command decoder block (internal LD risetime is 5 μ s). With software work-arounds, all commands seem to work.
- Have examined other problems with digital readout, particularly “Row 0” problem. This lead to a fairly workable procedure for scanning.
- Markus and Mario made many scans (presented separately here).
- John has made some additional scans of overall chip.

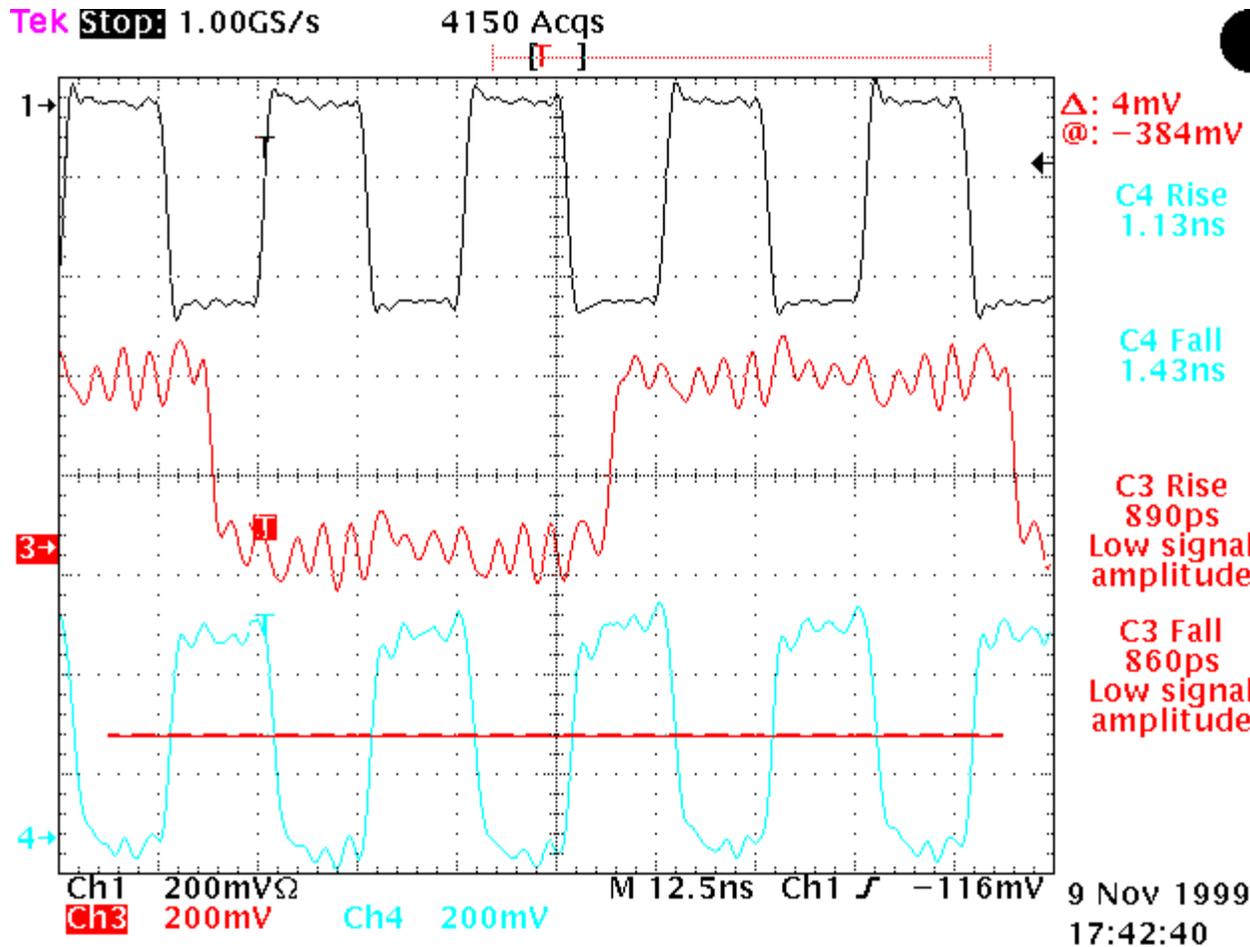
Measurements of Digital Readout Circuitry

- Realized that there is a serious problem with XCK distribution inside FE-D, with relatively small transistors in LVDS receiver driving a fanout to 72 FF over a large, minimum width, set of busses (perhaps 13mm of busses 1.6 μ wide, giving 8K squares of sheet resistance, or about 300 ohms).



- Observe very poor risetime on internal XCK of about 5ns (10-90%). Duty cycle at VDD/2 is still 50%.
- For reference, TSC0 is also shown. It has a risetime of about 1ns, as expected for the combined Picoprobe and scope bandwidth (500 MHz).

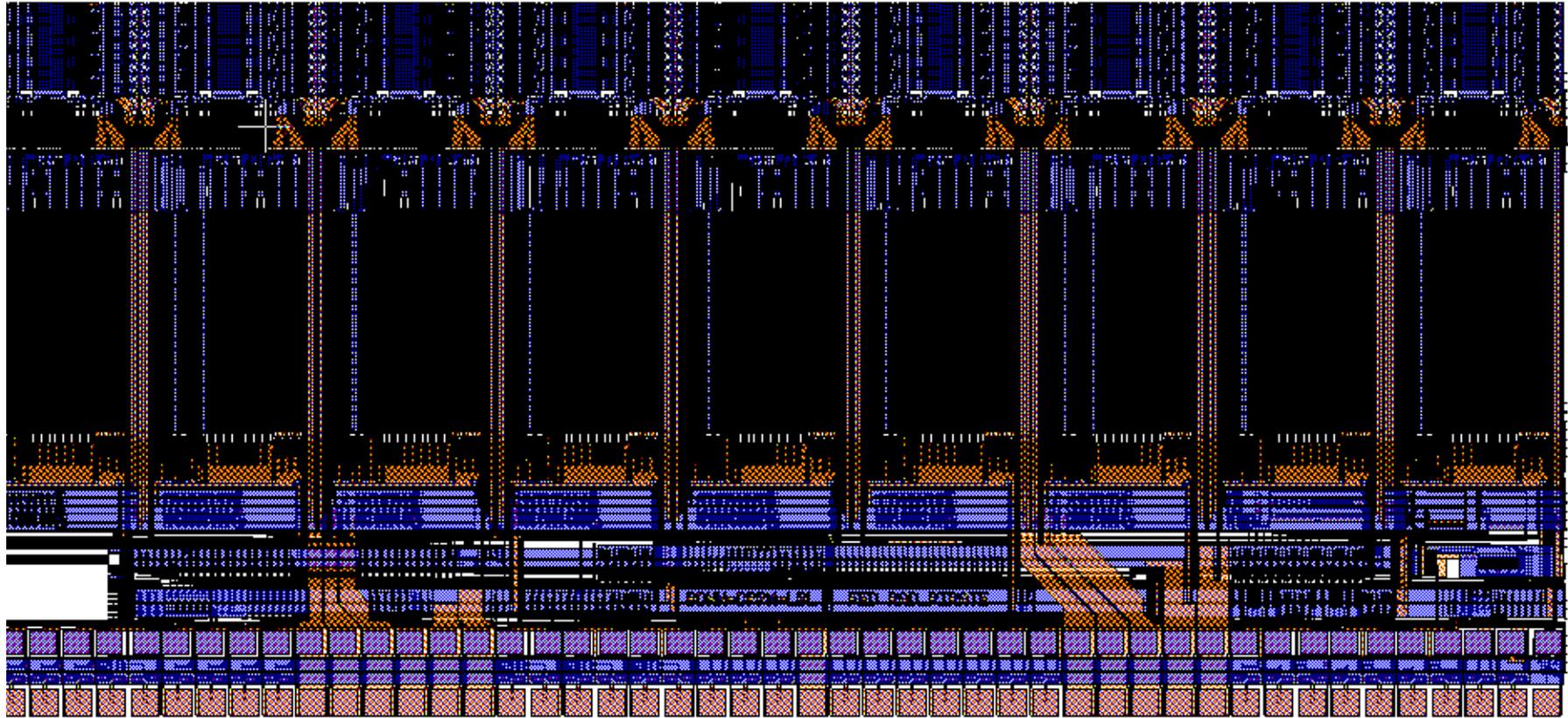
- Have also injected an external XCK from a LeCroy pulser, using a terminated PicoProbe. The phase of the injected XCK was adjusted by placing both the injection probe and an active probe on the same pad, and comparing the phase of the observed XCK with and without the injection needle touching the pad.



- Externally injected XCK looks good at injection point (but there was a minor ground problem which caused the observed ringing).
- In order to achieve good operation of the chip at VDD of 3.5V, the injected clock amplitude as 5V.
- This suggests internal distribution is also poor.

Layout Issues:

- Layout of bottom of FE-D, where XCK is distributed:

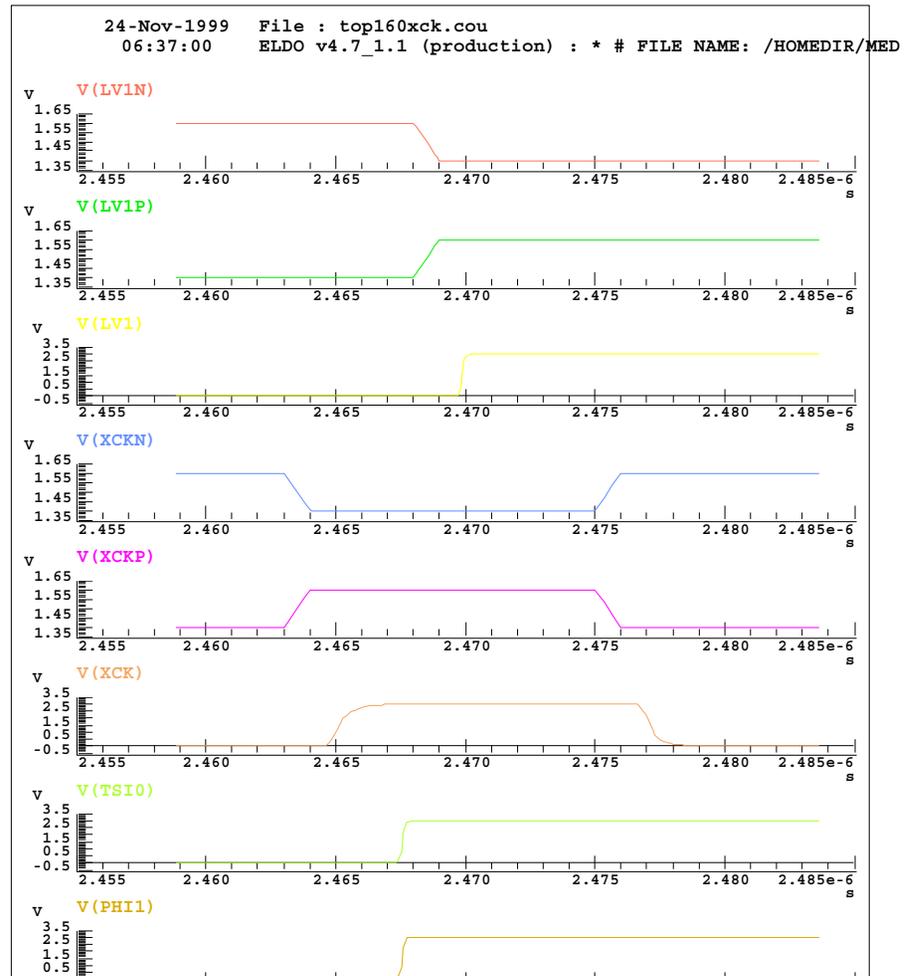
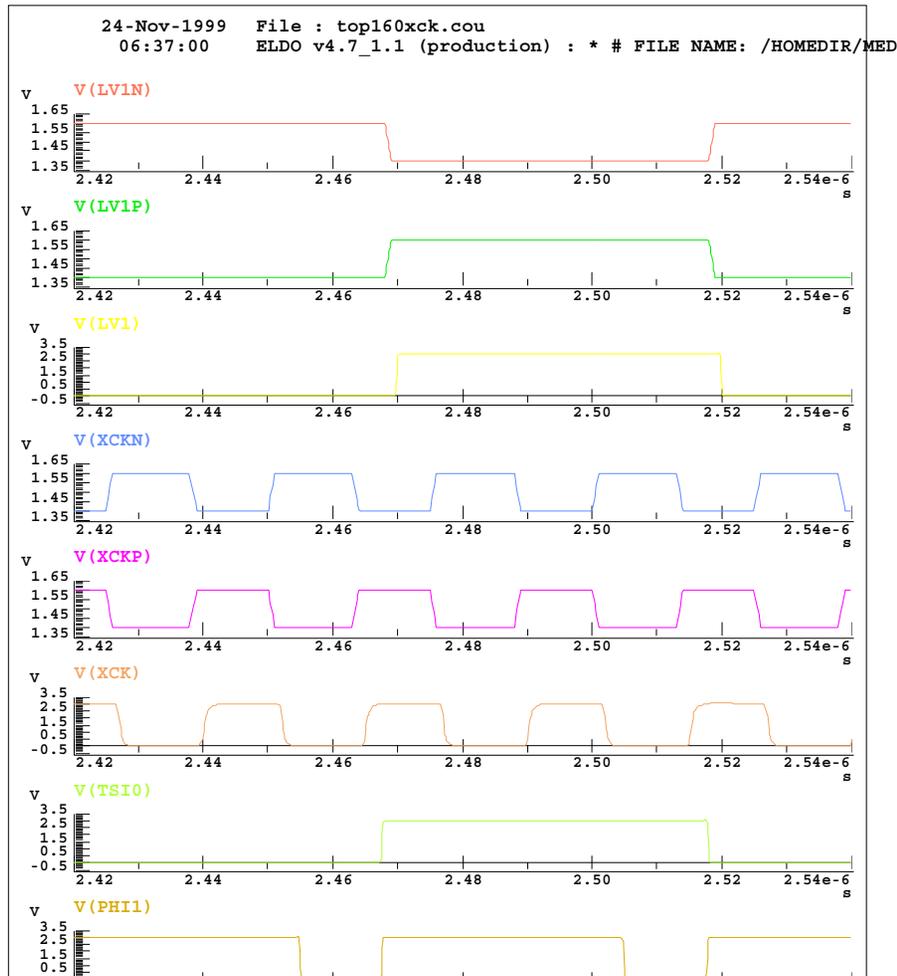


XCK Bus Topology:



Further progress requires better simulations:

- Previous digital readout simulations were extracted from schematics and did not include pad frame or interconnect parasitics.
- First step towards improvement: include pads for XCK/LV1/SYNC in basic column-pair + bottom-digital simulation. No significant degradation seen:



Next simulation steps:

- Extract proper R and C for each segment of the XCK distribution bus, and include this bus as an additional level in the hierarchy. This requires spending some time with the layout.
- In general, we need to create special netlists which are extracted from the layout and include all interconnect parasitics. This requires making special “chopped” layouts, and takes some investment.
- I am willing to do the simulations, Gerrit has extracted the present netlists, but I would like help from Bonn on the layout files and extracted R and C values.

Given the present layout, expect that:

- Present XCK pad does not provide a good point to use when injecting an external XCK. It is far away from much of the circuitry.
- Some internal blocks which we assume are well-synchronized are not that close to each other on the internal bus. They may see rather different clock signals.
- We need to carefully study this whole problem to see how many of the other problems we see can be blamed on this one mistake.

Other Digital Readout Problems

- Once we are operating at a large VDD, and various command decoder problems have been worked around, can use digital injection to study readout circuitry in detail.
- Observe in general that there are many pixels which do not respond to digital injection. This depends on the VDD supply voltage, and also on the sense amp bias (contrary to simulations which suggested that the bias was not important at all before irradiation). Difficult to be sure whether this is a fabrication yield problem, a problem with process parameters, or a marginal design in some way which did not appear in our simulations.
- An additional problem is that when scanning, there are very often extra hits appearing in the output stream which have Row=TOT=0. Their column number is correct, and they occur randomly in time: we issue many L1 per event, and the excess hits are not associated only with the crossing into which we inject real hits. Essentially all bits produced by the pixel itself are 0, suggesting a problem with data transmission in the column.
- For digital injection, this problem seemed to occur only when certain dead pixels were enabled for readout. John introduced a special scan to mask off all channels which did not respond to digital injection, and this seemed to eliminate the “row 0” problem for digital injection. However, it is still present for analog threshold scans.

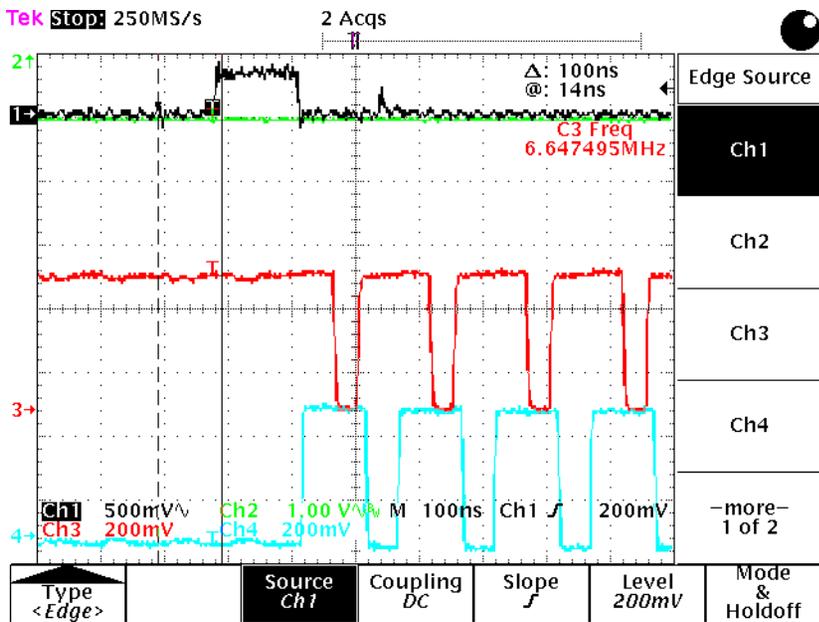
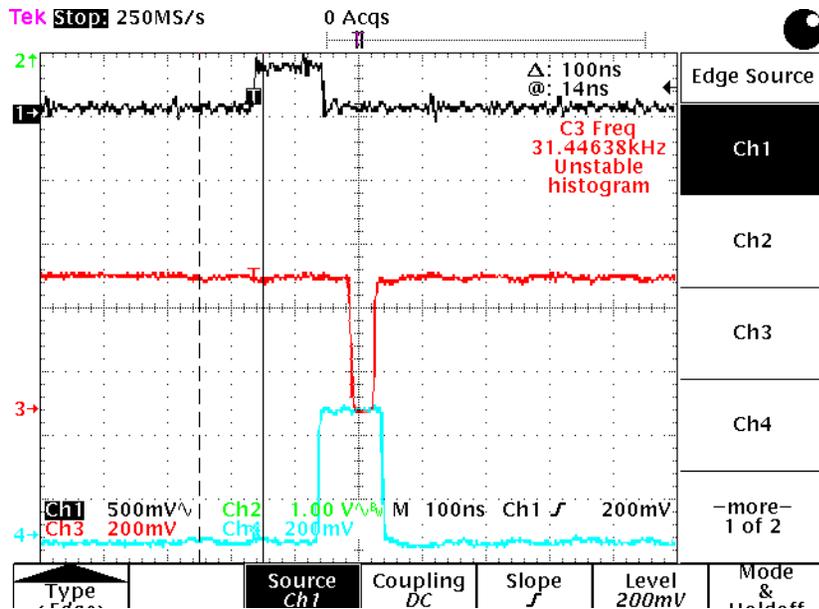
Overview of CEU operation and column readout:

- Hit pixels notify CEU on trailing edge of discriminator signal that they have data using the PriL/PriR signals. Sparse scan and control operates in parallel for two sides of column pair. CEU arbitrates bus using ReadPix signal.
- CEU issues Freeze signal to block entry of new hits into sparse scan circuitry.
- CEU issues ReadPix signal to instruct pixel selected by sparse scan (topmost hit pixel in column) to present its data on the shared bus.
- CEU issues ClearPix signal to instruct selected pixel to clear its hit status. After this, the sparse scan propagates to the next hit pixel in the column.
- CEU will leave Freeze on as long as Pri is asserted (indicating there are remaining hits in the column to read out).
- CEU will issue ReadPix/ClearPix signals to both sides of the column pair until Pri goes away, indicating the “frozen” hits have all been read out.

When “row 0” problem occurs:

- Typically see that at a certain point in a scan (at a certain, normally dead, pixel), the CEU seems to go into a loop of sending Freeze/Read/Clear. Presumably no pixel is selected at this time, so this generates empty hits.
- A stuck on pixel cannot produce this effect (Freeze only turns off when no pixel is asserting Pri), so it requires a strange malfunction of the pixel hit logic...

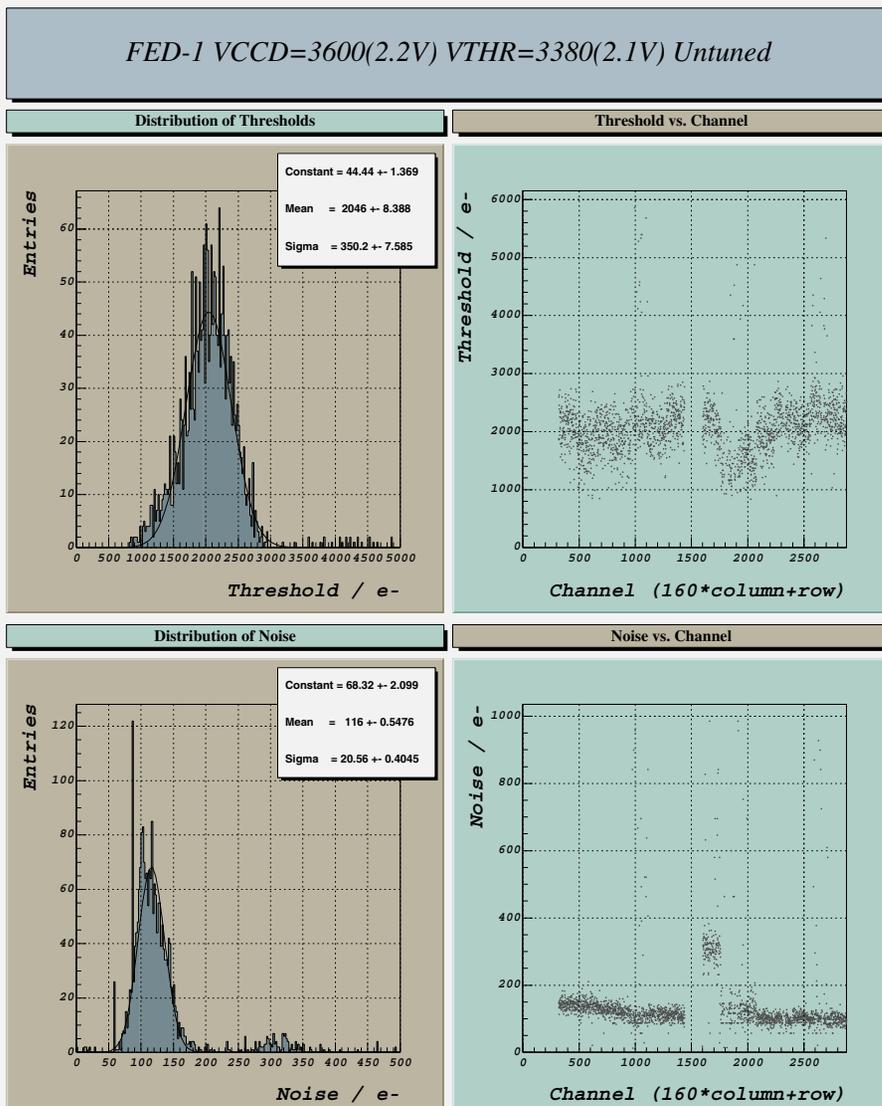
• Example scope pictures of “good” and “bad” pixels:



- For good pixel, see Strobe (hit injection), then Freeze and ReadPix (inverted). A single cycle occurs to read out the data from the single hit pixel.
- For bad pixel, see that present of hit creates a continuous sequence of Freeze/Read signals. They occur as quickly as they can be generated by the CEU.
- This is strange because Freeze will only go away if there is no Pri, and Freeze will only come back if there is a Pri. It is very difficult to understand this if the schematic is functioning properly...
- All signals in the column pair look good (good rise/fall and expected timing behavior).

Examples of Analog Scans

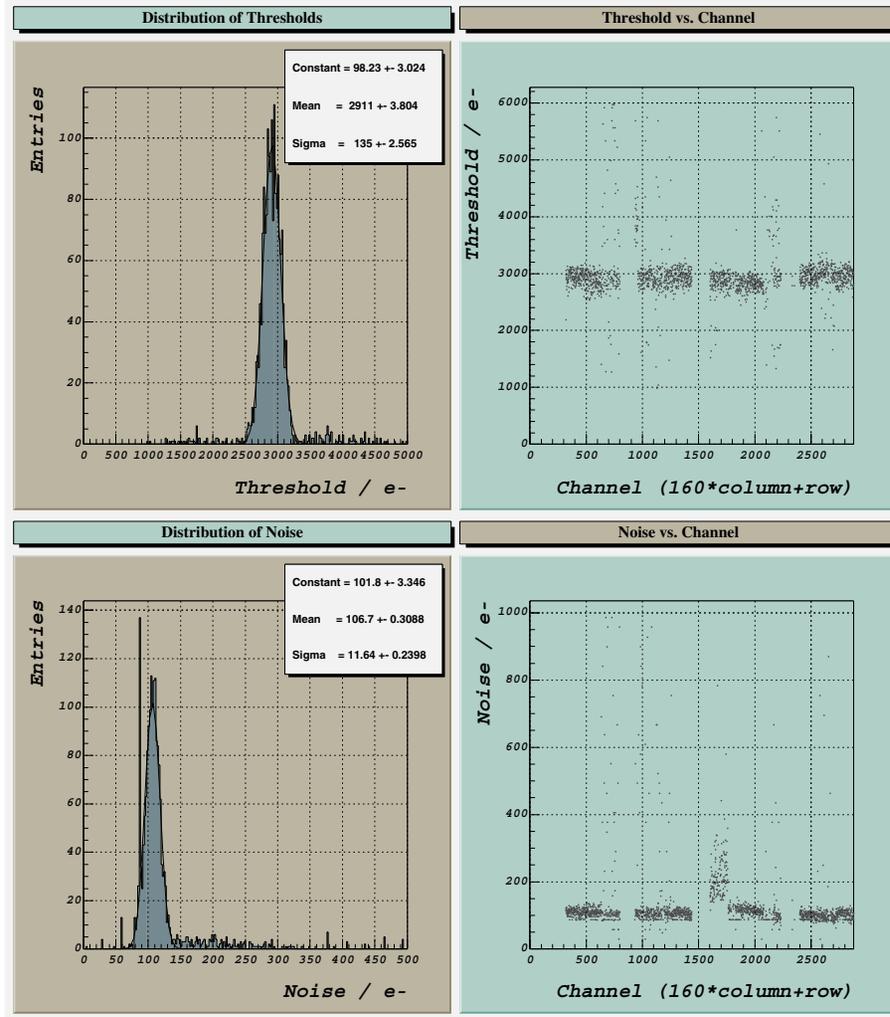
- Use operating point with large VCCD (slow shaping in AC-coupling to reduce noise and dispersion). Scan threshold for FE-D #1 and check TDAC tuning:



- Initial threshold dispersion is about 350e for a threshold of 2000e.
- Noise is about 120e, with one column which is intermittently “noisy”.

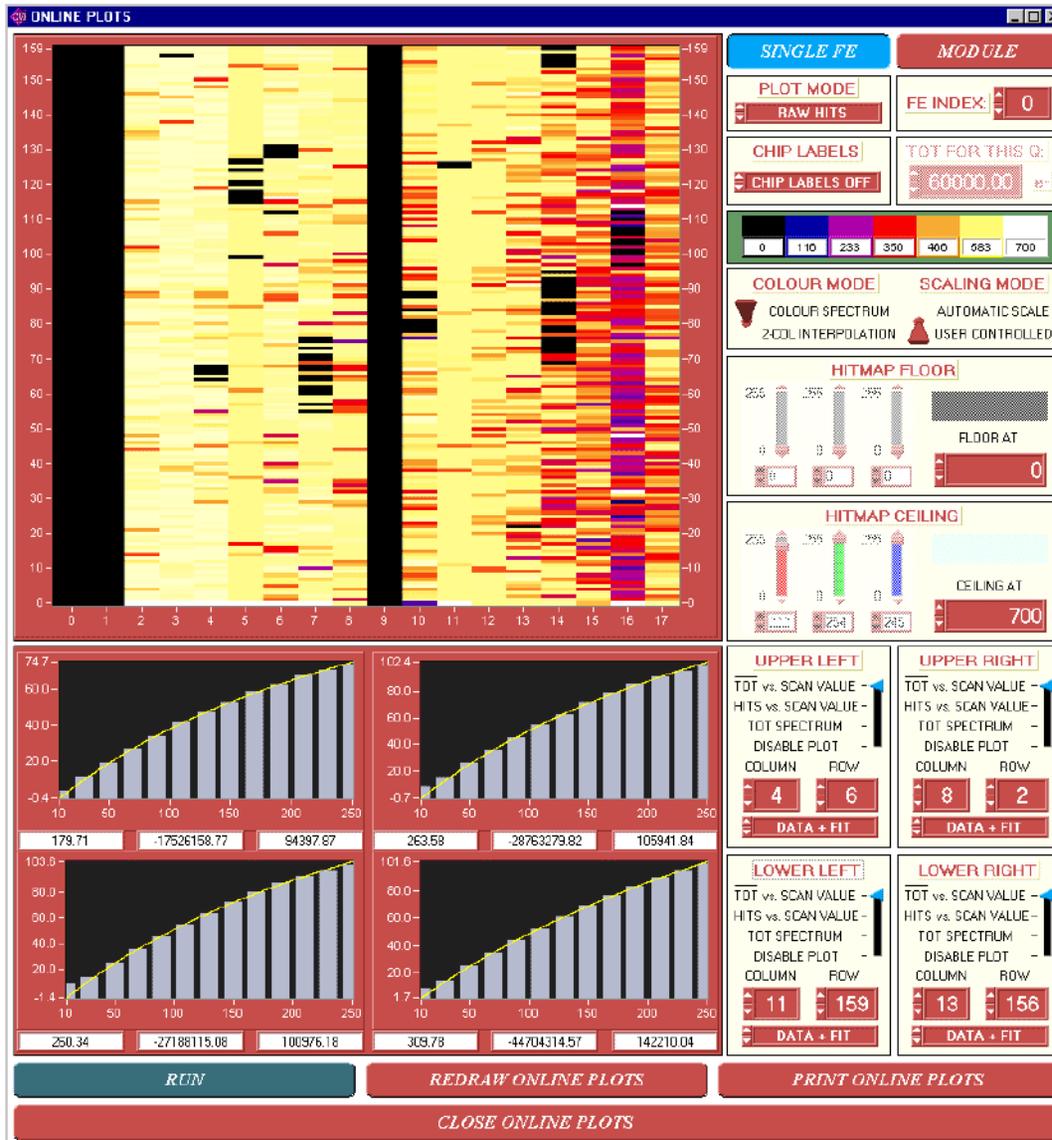
- After tuning, see expected improvement in threshold dispersion, so TDACs are clearly working. To achieve this, the TDAC step size was also scanned to chose a fairly optimal value:

FED-1 VCCD=3600(2.2V) VTHR=3324(2.0V) IF=20 ID=IP=IL=IPS=40



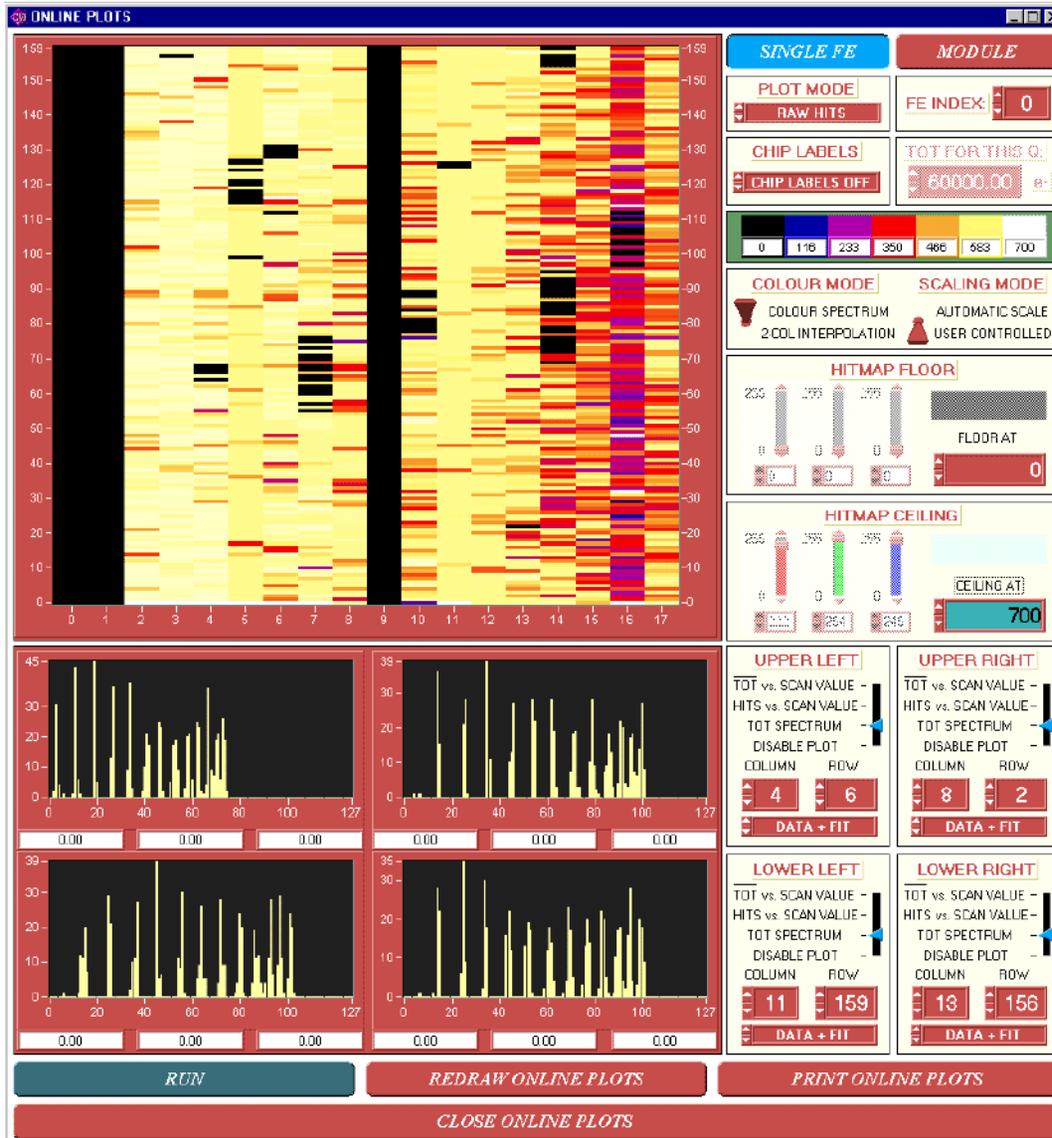
- After tuning, the dispersion is reduced to about 135e.
- The noise is about the same, but this particular chip shows fluctuations in the noise behavior, and is often much noisier.

- Do a TOT scan as well to look at dispersion (required increasing IF from 20 to 35 to avoid losing hits with large charge). Used FE-D #1:

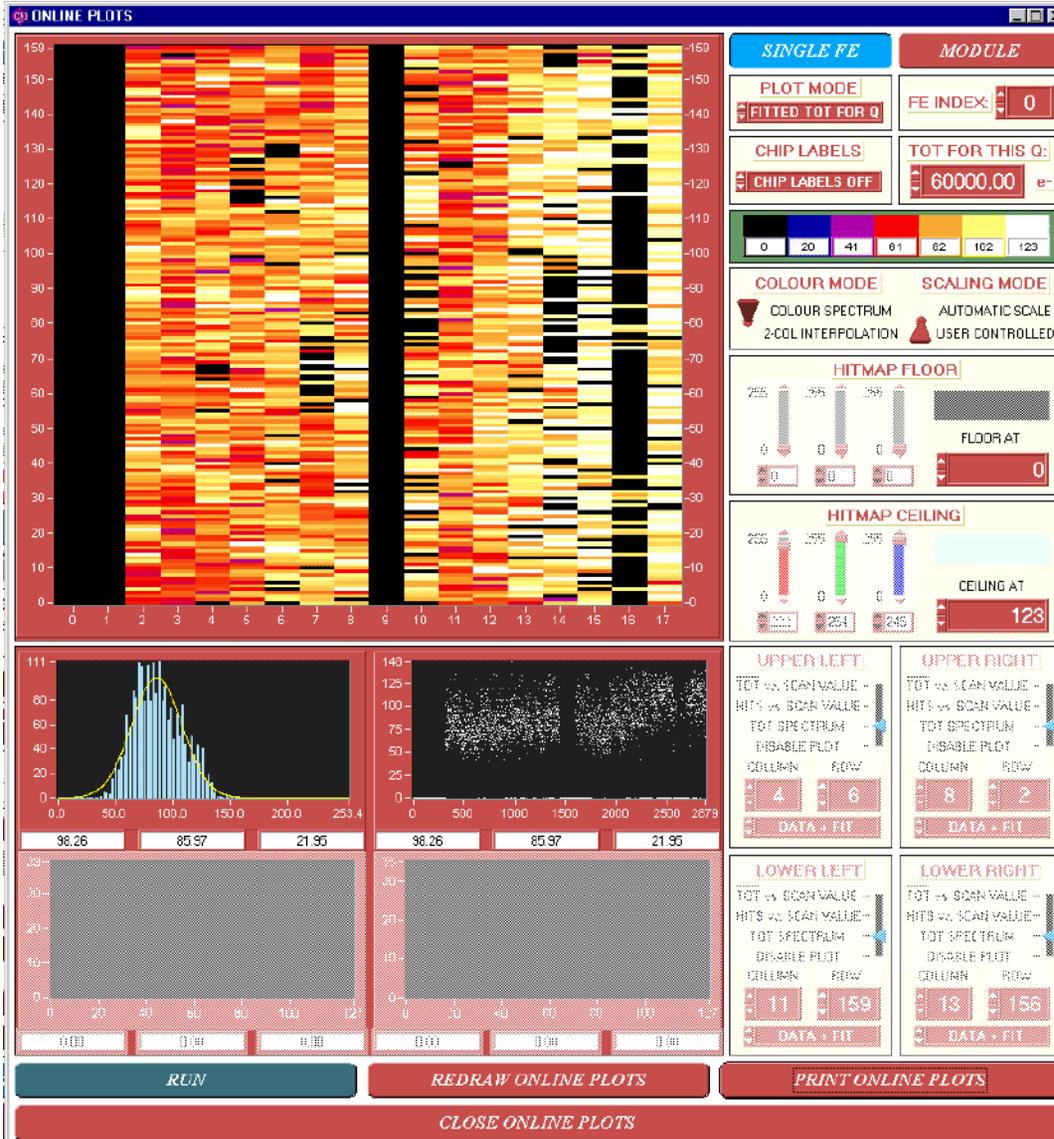


- TOT response curve is quite nice at high VCCD.
- Units are DAC counts for internal chopper DAC.

- Spectra for individual channels show a good charge measurement:

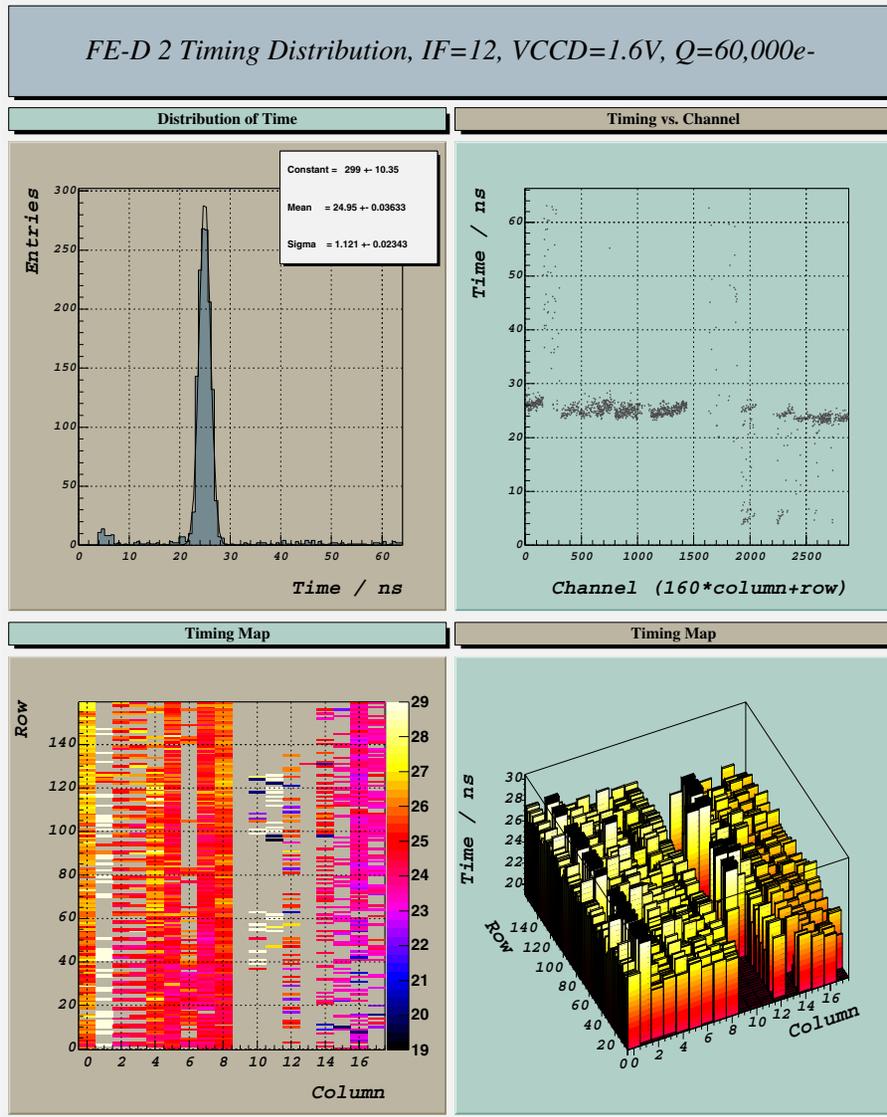


- TOT dispersion over the whole chip is also reasonable:



- Mean TOT for 60Ke (extracted from extrapolation of fit) is 86 counts.
- The dispersion on this value is 22 counts over the working parts of the chip.
- This value does not show any particular structure over the chip.

- Have also performed timing studies by injecting a large charge (60Ke) and scanning the delay to find when the hit moves from one crossing to the next:



- Scan was done for FE-D #2
- Perhaps some small indications of systematic effects, but chip had many bad/dead channels, so it is hard to tell.
- Taking an RMS over the channels gives 1.1ns, which is similar to the results obtained from FE-B in the past.

Summary and Next Steps

Overall comments:

- FE-D requires very high VDD voltage to operate properly (far beyond anything which is acceptable). Limiting factor seems to be data corruption, possibly related to XCK of serializer, or relative timing of serializer and output MUX (speculation). Difficult question is to what extent this is a result of problem with XCK distribution, and to what extent it is a separate problem.
- There seems to be a very significant yield problem. In the first wafer, only 19% of the die pass minimal digital tests. None of the die examined so far are anywhere close to passing the simple tests used to evaluate FE-B (better than 90% yield). Again, it is difficult to decide whether this is a real fabrication problem (single defects in processing), a marginal design aggravated by poor process parameters (but we tried to use the “advice DRC” layout rules to increase the yield in most places), or a side-effect of known errors like the XCK distribution problem. We should study the advice DRC errors in circuit blocks that appear to have low yield and see whether there is any pattern.
- The yield problem also appears as a large number of local fabrication defects in each die. Of the chips examined in detail, all have many ten’s of individual bad channels, as well as bad column pairs, noisy column pairs, etc. None are close to a chip we could use in an ATLAS module.

Analog Performance:

- Well-known layout error in poly capacitors in VTH amplifier. Problem can be dealt with on individual die by surgery and use of external VTH source.
- Many aspects of the analog performance look more or less as expected. The previous problem (FE-C, MAREBO) with transit time variations is solved. This is very encouraging. Timewalk performance is still to be studied.
- Some surprises: poor threshold dispersion for all but the highest VCCD settings. Recall also that dispersion is usually somewhat worse with detectors attached. Also very sensitive threshold control when using large VCCD values (100mV change in VCCD changes the threshold by more than 2Ke) which is a poor match for large step size of voltage-mode DACs used for control in FE-D.
- When VCCD is “nominal”, there appears to be large TOT dispersion as well as large threshold dispersion. A significant part of this seems to come from odd-even variations in row and column number (basic mirroring in the pixel cells). This needs further confirmation and study, but would seem to point to poor matching in the long threshold control transistors which also affect shaping.
- There appears to be some systematic problem with a threshold variation versus column number that could be related to distribution of the VCCD and VTH horizontally. Given the sensitivity of the threshold to these voltages, shifts of 10's of mV can be significant, so resistances of 10's of ohms are important.

Digital Performance:

- Beyond the VDD problem and the low yield, the next major issue is the XCK distribution problem. Clearly, the quality of the internal XCK signal is not great. However, it would be surprising if, even with the poor risetime observed on the probe pad, either the VDD problem or low yield could be explained by this.
- The “row 0” problem seems to involve strange interactions between bad pixels and the CEU. Nothing like it was ever observed in simulations. It appears to occur mainly when there is a “bad” pixel involved, so it may not be a fault in the present design, but a result of a common single-point failure in fabrication. This will require further study of different chips, and further simulations.
- Significant sensitivity to the sense amplifier bias has been observed in the data. This is not expected from simulations of pre-rad performance. Again, needs more simulations and measurements.
- There are some significant drive strength problems in the command decoder (internal Write_Mask, Write_Bit0, Write_Bit1, Write_Bit2).
- There is a minor bug in the column mask logic. The Buffer Overflow OR which propagates across the column pairs also needs to be masked, otherwise disabled column pairs can force constant buffer overflow conditions.

Next Steps:

- We need to agree on a formal response to TEMIC about this run. In order to make technical progress, we need at least several of the wafers from this run. Perhaps this means formally rejecting the run, and then negotiating a reduced price for the wafers. It is already awkward to do this when we have the wafers already in our possession, but we have to reach an agreement soon!
- We should survey more of the existing wafers to see whether the same basic problems exist on all of them. A quick look at Wafer #2 and #3 indicates similar behavior to that of Wafer #7. We should continue to improve our wafer probing tests until we decide on what a good die will be for this run of FE-D.
- We should then send the two best wafers to Alenia and IZM for bumping and assembly into single chip devices. I believe there are too many problems (and too few good chips) to make full modules.
- With these assemblies, we can investigate some of the open analog questions (timewalk and cross-talk for example). We can also compare the performance of assemblies with Alenia and IZM bumps to see whether the noise problems seen with FE-B and Alenia are reduced in the FE-D design.
- It is not yet clear to me whether there is any useful irradiation program that can be defined with these die. A full understanding of the high VDD and XCK problems may allow us to do some irradiation work with single die. Perhaps we can at least irradiate the analog test chip to study front-end performance versus dose.

Re-submission of FE-D:

- Based on the present FE-D performance, we cannot reach any conclusions about TEMIC as a vendor for pixels, and we almost certainly cannot make the irradiated system tests which are vital to validating our modules.
- We already have too much investment in DMILL to stop now, so we will have to re-engineer and re-submit this chip as soon as possible. The minimum time to prepare this work (we really MUST be successful the second time!) is probably several months (e.g. re-submit in Mar. 00). We have to organize this effort and define priorities and tasks during this meeting. I would like to keep significant momentum in our FE-H effort as well, but this may prove to be impossible.
- It is essential that we learn as much as possible from the existing chips, to eliminate as many problems as we can in the next iteration. This requires completing some of the work we didn't do before. In particular: simulations of critical circuits from netlists with all parasitics from layout, and systematic checking of all drive strength issues. It also requires lots of careful lab measurements.