

## Pixel Electronics Status

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### **Status of FE-D testing:**

- First results from wafer probing and lab testing
- Next steps
- Organization for re-submission

### **Status of other chips on FE-D run:**

- First results on MCC-D0 test chip
- First results on DORICp
- Other devices (analog test chip, LVDS buffer chip, PM bar)

### **Status of FE-H design:**

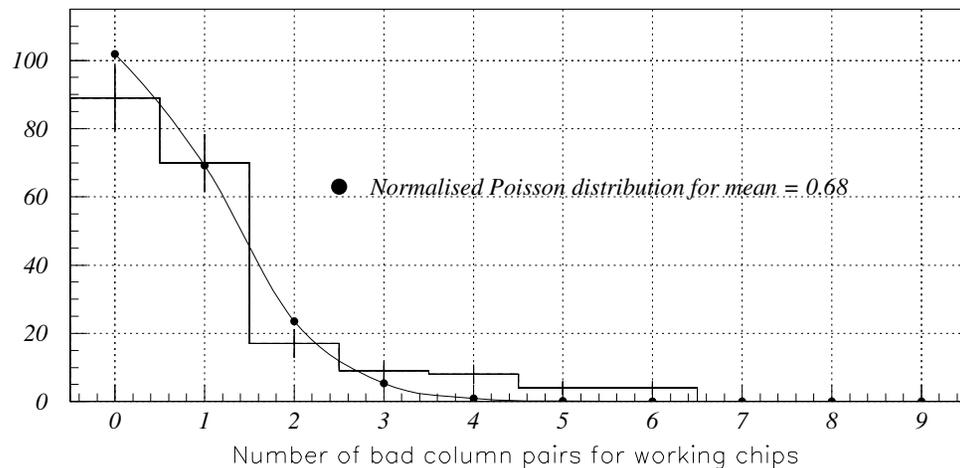
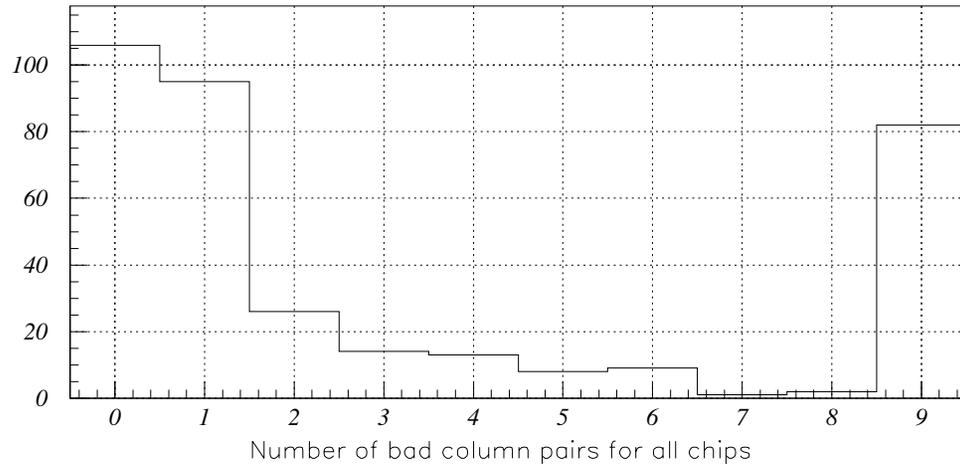
- Organization
- Status

## Wafer Probing

- Several basic problems uncovered. These include VTH amplifier short (our layout error, not caught by TEMIC LVS/DRC), buffering in command decoder (software work-arounds), and XCK distribution problem (impact not yet known).
- Additional strange behavior observed, seems to be related to defective channels (“Row 0” problem).
- However, basic chip functionality is OK (noise, analog control, TOT behavior, timing uniformity, operation of readout circuitry). Still some concerns about threshold dispersion and timewalk, plus some systematic effects.
- Have now probed three wafers in LBL, using simple selection criteria. These are basically tests of control logic (small fraction of chip), and include working Global Register and Pixel Register, plus operation under digital injection with return of EOE words. Yields are 19% (wafer #7), 31% (wafer #2), and 27% (wafer #3).

- Have analyzed the Pixel Register problem in more detail, using column-masking to divide register into 9 column-pairs, and studying bad column pair rate:

*FE-D wafers 02, 03 and 07*



Look at distribution of number of bad column pairs in register per die.

Remove chips that are already bad for other reasons.

Find well-described by Poisson, with mean of 0.6.

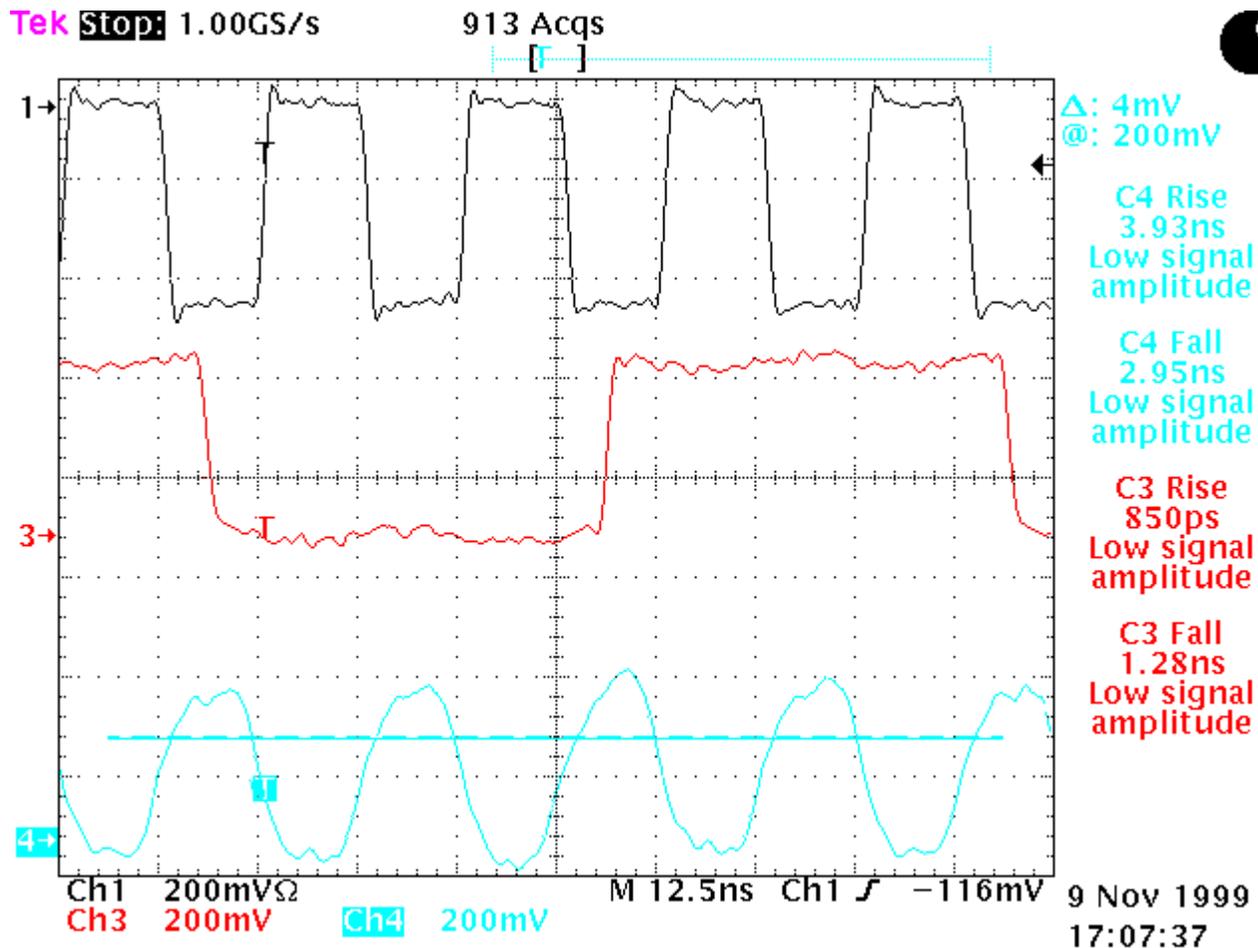
This confirms notion of single-point defects, but with a very high defect density (shift register area about  $4\text{mm}^2$ ).

Suspect yield arises from high off-current in NMOS used in dynamic FF. This requires about 1 out of 500 NMOS to fail in this way, but static logic should not be affected.

- For all of these wafers, correct operation required setting VDD to a very large value (above 4.5V), whereas our pre-rad simulations indicated 3V would work. It is possible that much of this problem is a side-effect of the XCK distribution problem, but we will have to prove this by careful measurement/simulation comparisons.
- The yield on the chips themselves for channels, column-pairs, etc. is very poor (essentially no good chips). This is the single most serious problem with this run.
- Already have significant concern about TEMIC/DMILL given that the yield for a smaller and simpler chip (ABCD, 55mm<sup>2</sup> and about 300K transistors) is about 20%, consistently over two engineering runs. This would optimistically scale to a yield of about 15% for pixels. Note Gil's yield table suggests that a fab yield of 38% requires us to purchase 1150 wafers for the complete pixel system, which already stretches our financial resources.

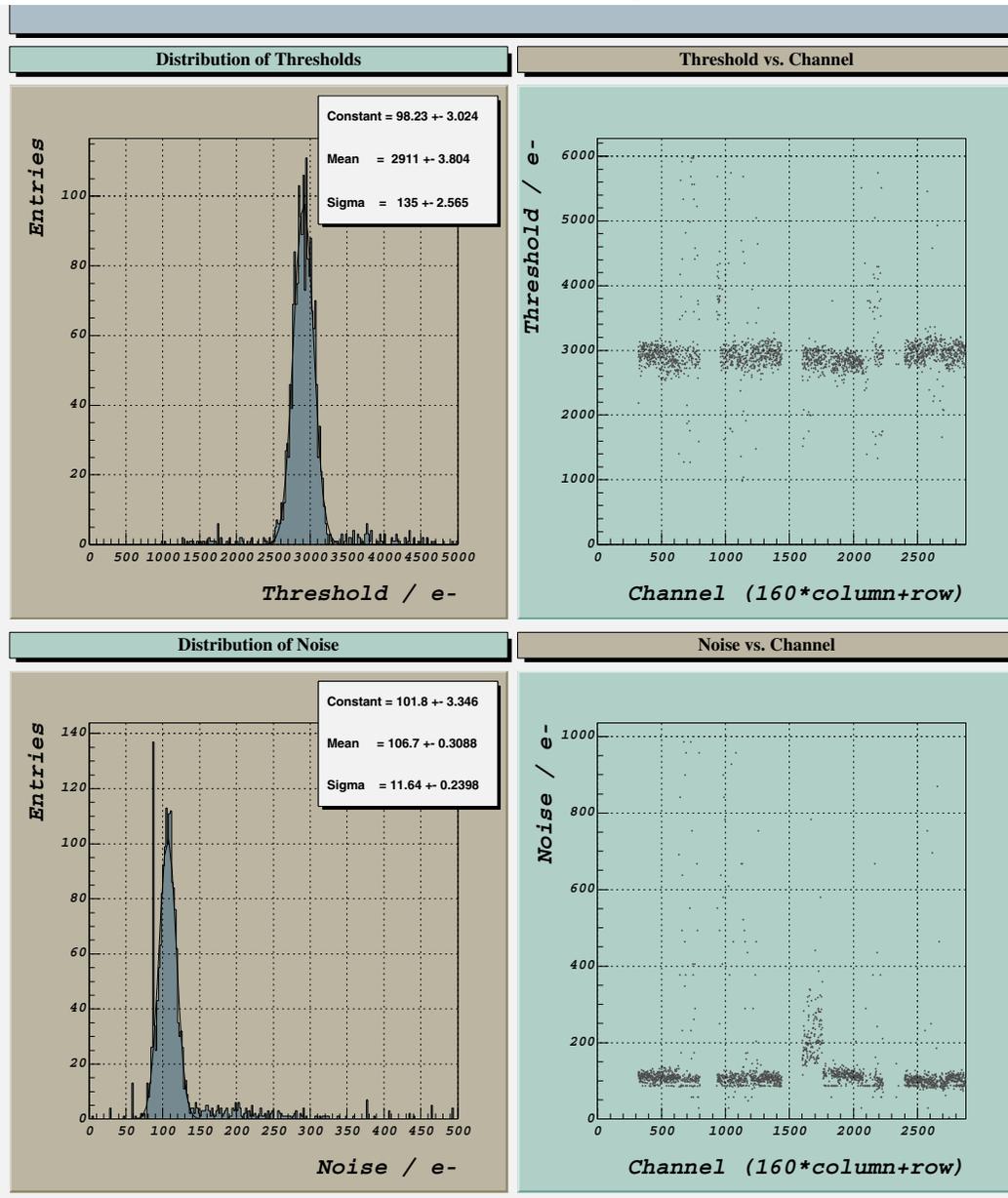
## XCK Distribution Problem

- Realized that there is a serious problem with XCK distribution inside FE-D, with relatively small transistors in LVDS receiver driving a fanout to 72 FF over a large, minimum width, set of busses (perhaps 13mm of busses 1.6 $\mu$  wide, giving 8K squares of sheet resistance, or about 300 ohms).



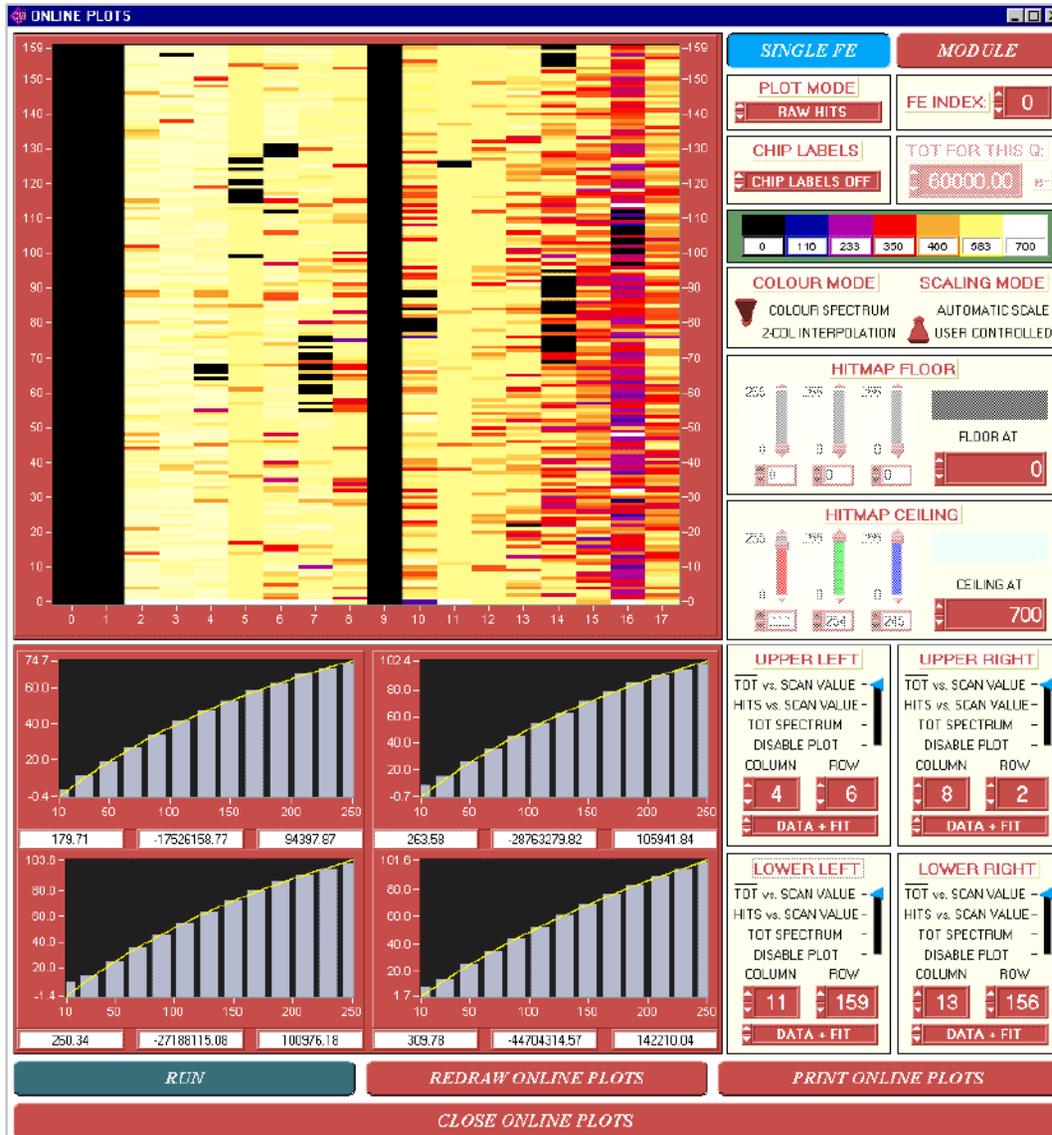
- Observe very poor risetime on internal XCK of about 5ns (10-90%). Duty cycle at VDD/2 is still 50%.
- For reference, TSC0 is also shown. It has a risetime of about 1ns, as expected for the combined Picoprobe and scope bandwidth (500 MHz).

• Example of threshold tuning scan:



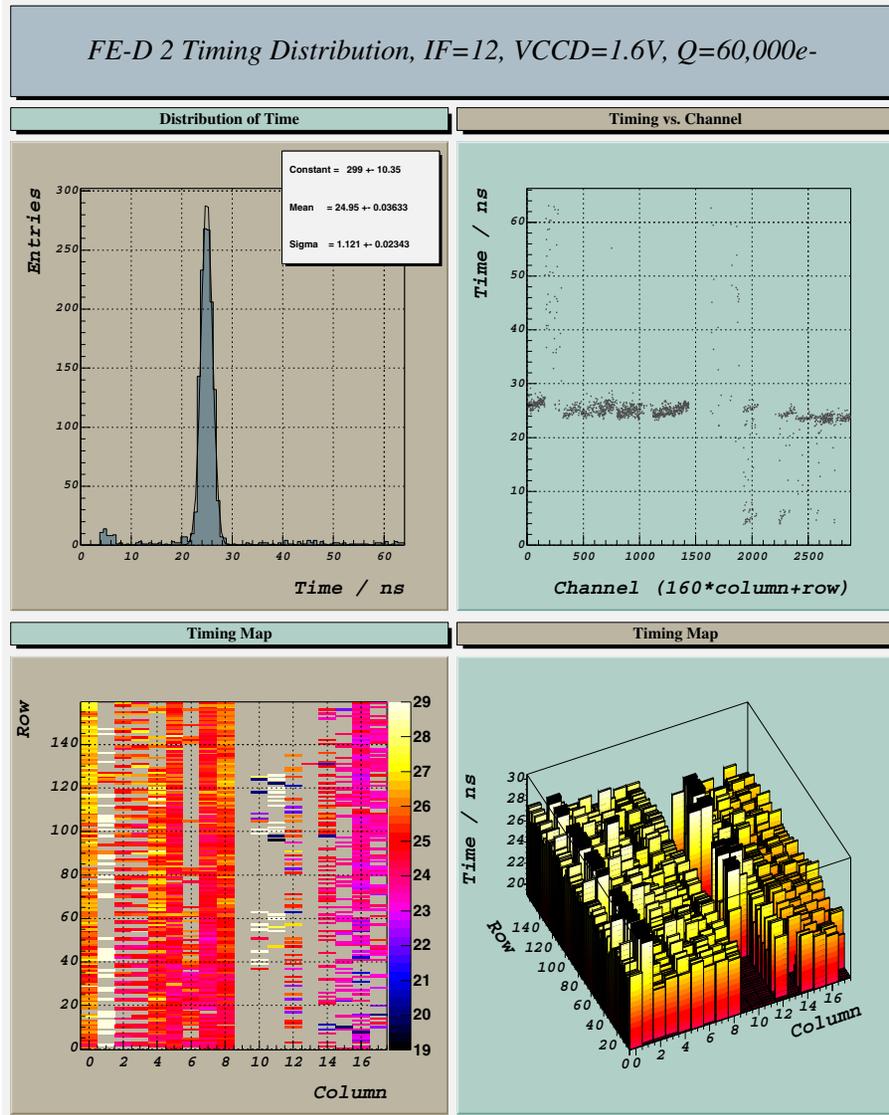
- Indicates the ability to achieve a good threshold dispersion (135e) and decent noise (105e).

- Example of a TOT scan to look at dispersion, using FE-D #1 mounted chip:



- TOT response curve is quite nice at high VCCD.
- Many dead single channels and bad column pairs.

- Have also performed timing studies by injecting a large charge (60Ke) and scanning the delay to find when the hit moves from one crossing to the next:



- Scan was done for FE-D #2
- Perhaps some small indications of systematic effects, but chip had many bad/dead channels, so it is hard to tell.
- Taking an RMS over the channels gives 1.1ns, which is similar to the results obtained from FE-B in the past.

## Next Steps:

- We need to agree on a formal response to TEMIC about this run. In order to make technical progress, we need at least several of the wafers from this run. Perhaps this means formally rejecting the run, and then negotiating a reduced price for the wafers. It is already awkward to do this when we have the wafers already in our possession, but we have to reach an agreement soon!
- We should survey more of the existing wafers to see whether the same basic problems exist on all of them. We should continue to improve our wafer probing tests until we decide on what a good die will be for this run of FE-D.
- We should then send the two best wafers to Alenia and IZM for bumping and assembly into single chip devices. I believe there are too many problems (and too few good chips) to make full modules.
- With these assemblies, we can investigate some of the open analog questions (timewalk and cross-talk for example). We can also compare the performance of assemblies with Alenia and IZM bumps to see whether the noise problems seen with FE-B and Alenia are reduced in the FE-D design.
- It is not yet clear to me whether there is any useful irradiation program that can be defined with these die. A full understanding of the high VDD and XCK problems may allow us to do some irradiation work with single die. We should irradiate the analog test chip and PM bars to study front-end performance versus dose.

## Re-submission of FE-D:

- Based on the present FE-D performance, we cannot reach any conclusions about TEMIC as a vendor for pixels, and we almost certainly cannot make the irradiated system tests which are vital to validating our modules.
- We already have too much investment in DMILL to stop now, so we will have to re-engineer and re-submit this chip as soon as possible. The minimum time to prepare this work (we really MUST be successful the second time!) is probably several months (e.g. re-submit in Mar. 00). It is important to keep significant momentum in our FE-H effort as well, or we will fail to evaluate a second vendor.
- It is essential that we learn as much as possible from the existing chips, to eliminate as many problems as we can in the next iteration. This requires completing some of the work we didn't do before. In particular: simulations of critical circuits from netlists with all parasitics from layout, and systematic checking of all drive strength issues. It also requires lots of careful lab measurements. We should draw the line at getting deeply involved in DMILL process issues, and concentrate on fixing our design as best we can.
- Once we have a more complete picture of the problems with this run, we should make a trip to Nantes to discuss in detail with TEMIC experts. This should happen fairly soon (mid-January ?), and could also be the final step in the negotiation of pricing for this run.

## Other Results from FE-D Run

- MCC-D0 tested by Genova, and appears to be working. The command decoder and the prototype FIFO are OK, but the FIFO is not testable at full speed. Note that this is completely incompatible with the defect density observed in FE-D if we assume the defects are “generic” and affect all types of circuitry in the same way.
- DORICp tested by OSU. Appears to work properly at 5V (it decodes command data and 40MHz clock), but not at 4V (locks to 20MHz). Internal nodes are available for debugging with probes. Testing getting started in Siegen and OSU.
- Analog test chip extensively studied in Bonn, and many nice results on FE-D front-end have been measured.
- Will extract device parameters from PM bar at LBL. Some indications that the preamp risetime is worse than expected (as well as timewalk), so want to confirm PMOS  $g_m$  in particular.
- Propose that analog test chips are irradiated, along with PM bars containing analog devices used in front-end.
- LVDS buffer will be tested next week at LBL using new rad-hard FE-D testboard. This is our vehicle for irradiating FE-D chips while they are operating.

## Status of FE-H Design

- TAA agreements now essentially in place with Bonn and CPPM.
- We are still working on finalization of Layout Rules covered under the TAA agreement with Honeywell. Next version promised for Dec. 7, and we hope it will be final enough to begin serious layout work.
- Laurent spent time this week already learning about HSOI and getting first copies of documentation from Gerrit. Expect he should gradually come up to speed over the next few weeks.
- Gerrit is working on Cadence files (now proposing to move to Cadence 4.4.2), standard cell library, and re-drawing digital schematics for limited synthesis using Synopsys.
- Emanuele is working on pixel/CEU design, including a new pixel RAM cell, improved hit logic, and CMOS sense amplifier. Expect to have design ready for layout in about another month or so.
- Next step would be to get Bonn started on two major tasks. The first is transfer of miscellaneous analog blocks (DACs, chopper, VCCD/VTH amplifiers, current reference, LVDS I/O), the second is EOC layout. Sharing of this work between LBL and Bonn will depend on FE-D re-submission needs.
- Critical paths for the submission are likely to be the front-end design, plus the EOC and BOC region where lots of hand-crafted layout work is required.

## Comments

- If we look at Gil's yield table to derive wafer counts, we see we need about 1150 wafers for pixel FE chips at 38.5% fab yield (TEMIC "optimal" yield). Present contract proposes a target yield of 70% of optimal yield as a trigger for wafer acceptance discussions.
- If we run this backwards and say our financial resources are fixed at something like 10MCHF for FE wafers alone, then using the present frame contract numbers, the minimum yield for TEMIC would be about 28%, and the minimum yield for Honeywell would be about 48%, in order to meet our budget target.
- Believe there is significant risk that we could fail to meet these target yields with one or both of these vendors. Certainly indications from TEMIC/DMILL are strongly in this direction.
- Backup is to use IBM CMOS6 process. Naively, assume same yield (but would expect yield closer to FE-B chip fabed with HP), and factor two for number of die per wafer using 200mm wafers. Then, need 575 wafers, at a total cost of less than 2MCHF.

## **This may be the only way we can afford to build the pixels...**

- Propose that, in parallel with our work with DMILL and HSOI, we begin work with IBM process (get NDAs in place and work on test chips for June 00). This will almost certainly require additional manpower (help from CERN and RAL ?).