

Preparations for FE-I Testing

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Focus on testing of FE-I chips and modules:

- Present status of boards
- New support cards
- Plan for FE-I Testing

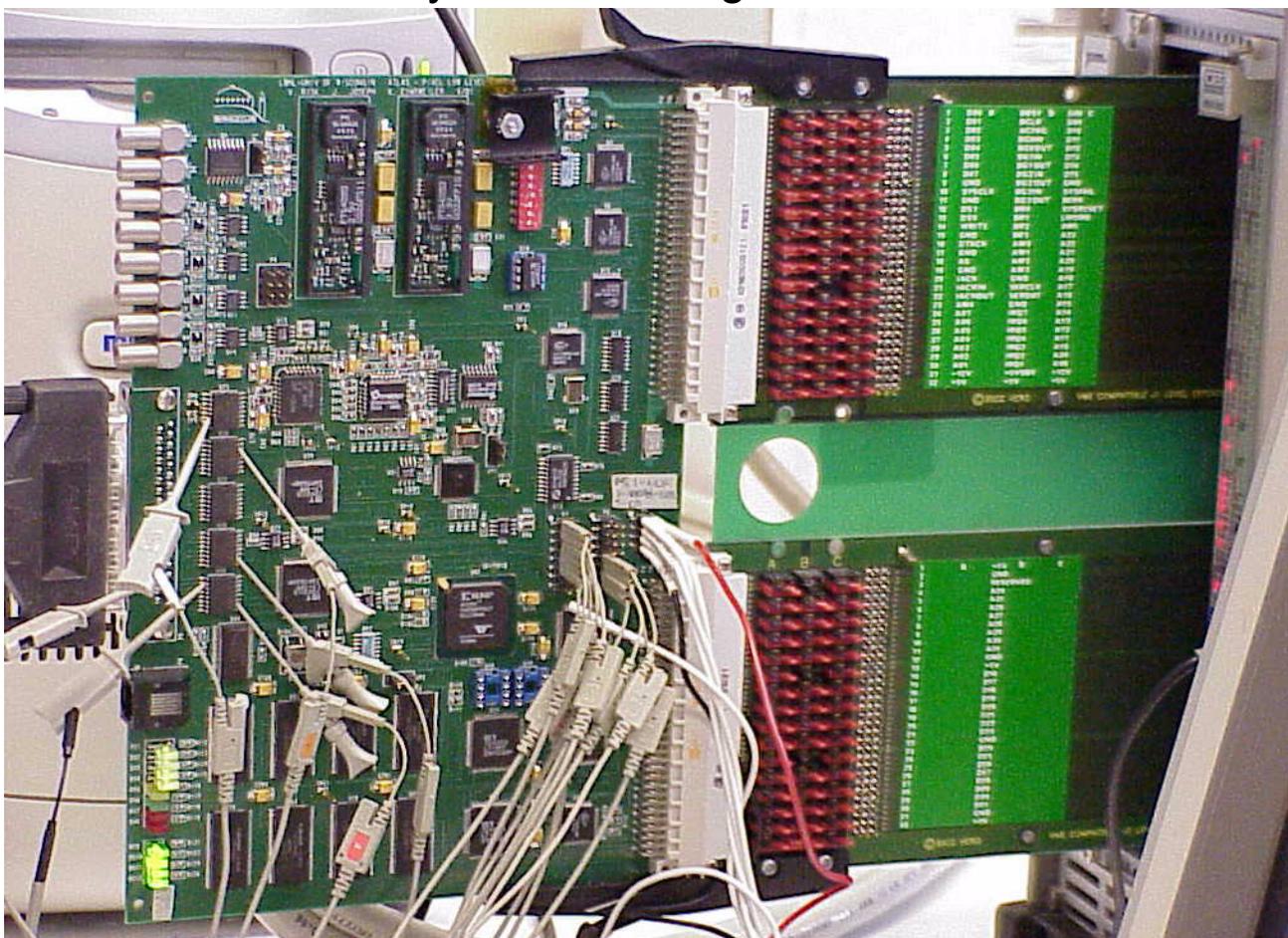
Important Comment:

- Presently do not plan to upgrade old PLL and PixelDAQ to support FE-I and MCC-I.
- Proposed path is to use new hardware (TPLL, PICT/TPCC) and new software (TurboDAQ) for this purpose.

Status of Components

TPLL Status:

- Have components for 10 boards. Fabricated and loaded 3 PC boards.
- First board working in the lab with single chips, including commands, scans, and histogramming. Operations using MCC are now working, and we will proceed to do first module scans very soon. Making I/O FIFOs work was not so simple.



- Will need further VHDL upgrades to support PICT and MCC-I. Both should be fairly straightforward.
- Layout errors found include negative regulator pinout, and 37-pin D connector mirrored (temporary solution is to mount it on the back of the board).
- Major omission was the circuitry required to decode the new 80Mbit data streams from the MCC. This requires just two FF and an inverted XCKR, but the present wiring brings the data directly into a FIFO, so trailing edge information is lost.
- Also intend to provide 32-bit bus between FPGA and VME (now only 16-bits wide).
- Present plan is to fully debug 3 cards that we have now, distribute one to Bonn, then revise the present artwork, and fabricate final boards in December.
- The first 3 boards would get us through the wafer probing of FE-I, and give time needed to produce “production” TPLLs before FE-I modules are back from bump-bonders (end March ?)

Software:

- New version of PixelDAQ called TurboDAQ. This already has all changes necessary for TPLL except for a user friendly interface for varying XCK frequency.
- Next major items are FE-I interface (more complex option-set in Global Register) and PICT interface (much more complex set of operations and scans). This work is beginning now.
- Debugging PICT software difficult before hardware arrives...

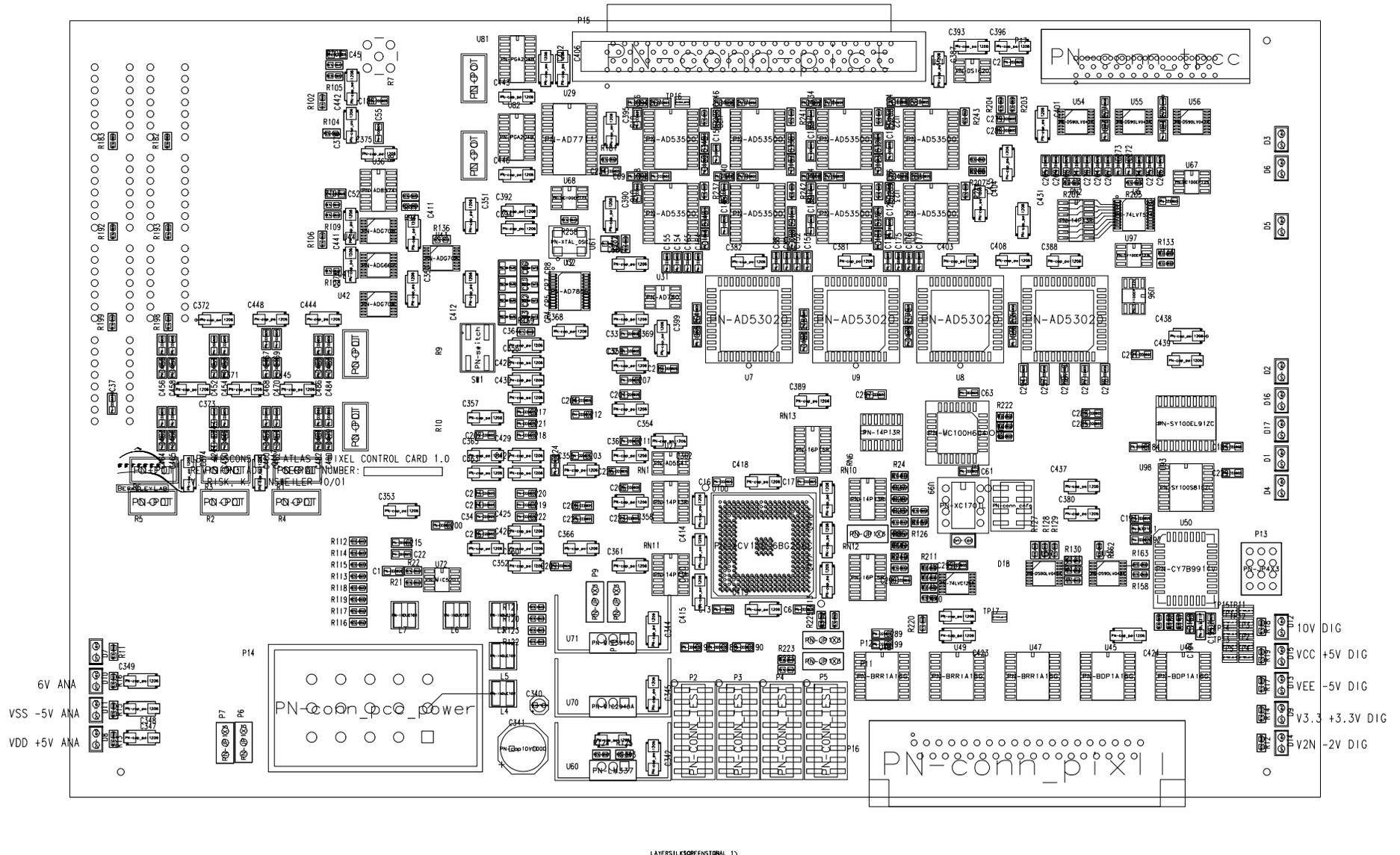
Compatibility with existing hardware:

- Supports additional DTO2 line by removing PCC_RESET. Otherwise, interface to PCC is identical. Therefore, it will work with the old PCC. We plan to retain the old PCC support code.
- We have defined an improved protocol for communication with the new TPCC and PICT, because there are many more, and more complex, commands for the PICT. The old protocol (adapted to the 68K controller chip on the Siegen PCC) is VERY slow (about 100 Kbits/sec) and limited.
- We are not planning to remove the support for FE-B/FE-D/MCC-AMS which already exists in the hardware and software. In fact, this is how we are testing the system now. Old single chips and modules will still be testable with the new hardware. The one option that has been dropped is the MCC-AMS transparent mode. This has been rarely used after the initial module debugging.

PICT Status:

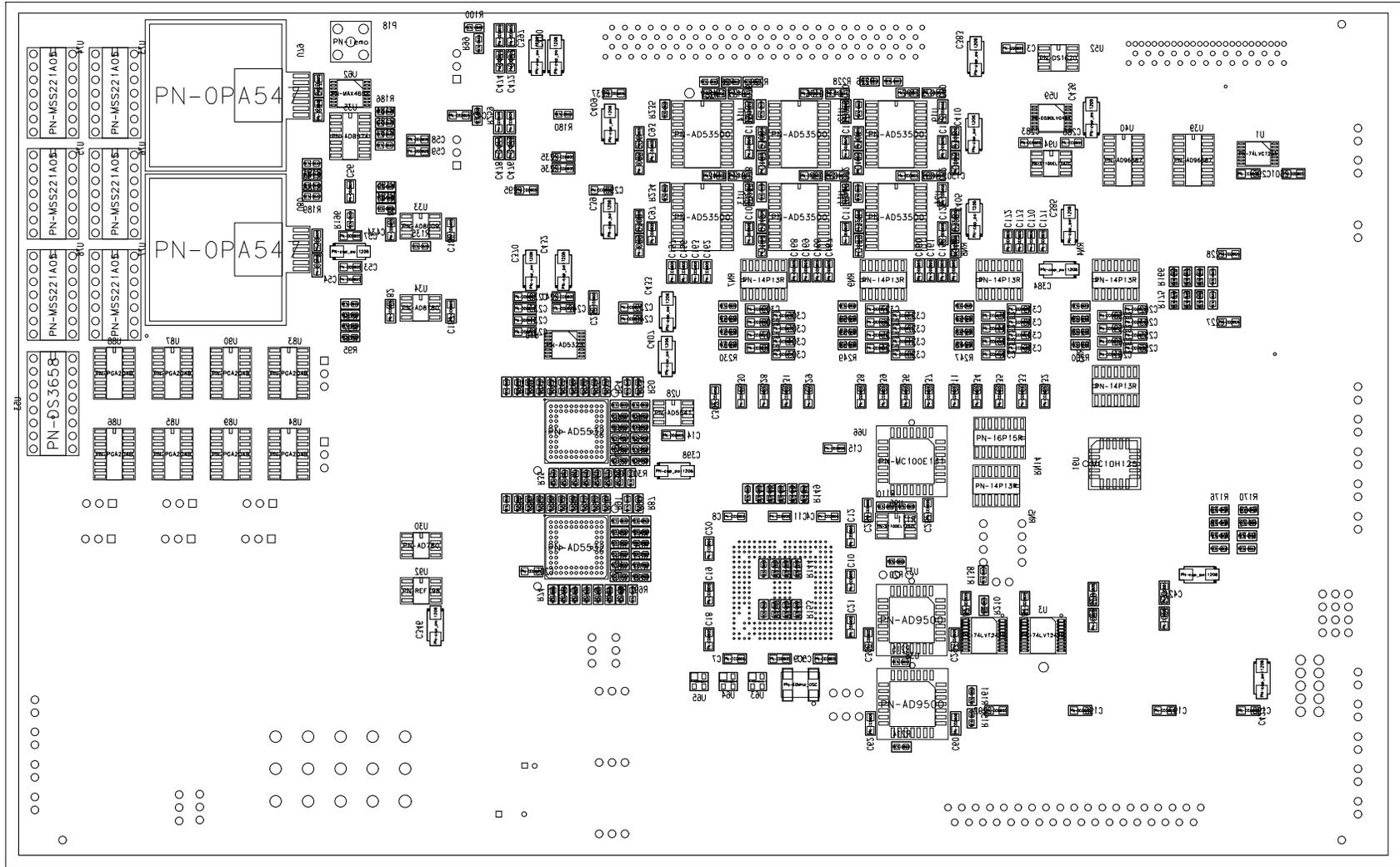
- Component orders for 5 boards completed, and all parts received, including parts for cables and support cards to be connected to PICT.
- Schematics frozen for several weeks, but one fix implemented last week for proper Strobe control in external inject mode (FE-I is not protected against using Str and ExtInj pins at the same time).
- Board has 12 layers (8 power/ground, 2 controlled impedance, 2 signal), and components on both sides. Achieves good separation of analog and high-speed digital functions, with hot parts on top. Input connectors are on bottom and output connectors on top.
- Power supplies will be +/-5V at about 4A and +10V at 1.5A, provided by GPIB lab supplies to allow monitoring of currents, and shutdown for overtemperature conditions. This should provide reliable unattended operation during wafer probing.
- TurboDAQ program is being extended to support PICT. New LBL postdoc Aldo Saavedra, and grad student John Freeman, will work closely with John Richardson on PC software for PICT and wafer probing, as well as production database and more sophisticated off-line analysis based on ROOT.
- Delivering fully supported systems to Bonn and LBL for FE-I probing before arrival of IBM wafers is highest priority, but given present schedule, may not be achieved.
- Backup solution is to start initial probing with TPLL and old PCC-based probe card. We will implement this as well (little additional effort required).

Component placement:



- View of top side of PICT. PICT connector is top center, PCC connector is top right.

Component placement:



FILE:PCB\BOARD\BOARD.BOT210W1.PCB

- View of bottom side of PICT

Schedule:

- Schedule has continued to slip due to resource conflicts and technical problems.
- All components are placed on board, and beginning to connect all parts to power planes.
- Next step will be to auto-route board, then deal with poorly routed controlled impedance and analog lines by hand. Expect that this should be fairly straightforward, as component placement carefully follows signal flow.
- Estimate that board should be ready to fabricate by Dec 14. This would give first loaded board by about Jan 11, due to holiday effects. This could slip further still...
- Depending on when wafers appear, it may be necessary to do initial wafer probing using TPCC, then proceed to dice half-wafer and study parts in more detail on support cards.
- Strong desire to do probing of all wafers which get bump-bonded using new PICT system, in order to create a comprehensive set of measurements.
- Suggest (given small number of wafers), we will benefit again from double-probing: probe all wafers in both Bonn and LBL. Then we can cross-check measurements and their consistency. Delay should not be large, but there is increased risk of damage in shipping or handling.
- At risk of duplicating work, it is probably necessary for Bonn to update the probing system they used for FE-D2 for use with FE-I, as this will provide basic analog characterization to supplement what old PCC-based system can provide.

PICT Command Protocol:

- Includes many commands to address individual chips on PICT/TPCC, and interface to them in a simple way. Present working definition, based on 32-bit words is:

PICT commands

	Write7711Ctrl	Read7711Ctrl	Read7711Data	Write7856Ctrl	Read7856Reg	Start7856	ADC_BusyInquire	Write5323	Write5532	Read5532	Write5541	Set9500Delay	Therm_BusyInquire	WriteTherm	ReadTherm	SetupReg	ReadSetupReg	ControlReg	ReadControlReg	FPGAalive	0x	
Bit 31 (MSB)							0						1		1		1		1		1	1
Bit 30							ADC = 0						0		0		0		1		1	1
Bit 29:							0	5323 = 0				5541/5532 = 1			1		1		1		0	1
Bit 28: Device			7711 = 0				7856 = 1	X	AOV_NIDOV			5532 = 0		5541 = 1	CHIP1		0		1		1	X
Bit 27	0	0	1	0	0	1	X	GAIN	CHIP	CHIP	CHIP	CHIP	0		0		1		0		1	X
Bit 26	0	1	1	0	1	1	X	0	0	1	DATA 15	DATA7	X	CHIP1	CHIP		X	CAPTEST	X	CAPTEST_EN	X	X
Bit 25	MODE 2	X	X	MUX 3	X	X	X	0	1	1	DATA 14	DATA6	X	CHIP0	THERMRD7		X	REFRESET	X	REFRESET_EN	X	X
Bit 24	MODE 1	X	X	MUX 2	X	X	X	DATA 11	0	0	DATA 13	DATA5	X	THERMWR7	THERMRD6		X	GA3	X	GA3_EN	X	X
Bit 23	MODE 0	X	X	MUX 1	X	X	X	DATA 10	0	0	DATA 12	DATA4	X	THERMWR6	THERMRD5		X	GA2	X	GA2_EN	X	X
Bit 22	GAIN 2	X	X	MUX 0	X	X	X	DATA 9	0	0	DATA 11	DATA3	X	THERMWR5	THERMRD4		X	GA1	X	GA1_EN	X	X
Bit 21	GAIN 1	X	X	RSEL 2	X	X	X	DATA 8	CHANNEL 4	CHANNEL 4	DATA 10	DATA2	X	THERMWR4	THERMRD3		X	GA0	X	GA0_EN	X	X
Bit 20	GAIN 0	X	X	RSEL 1	X	X	X	DATA 7	CHANNEL 3	CHANNEL 3	DATA 9	DATA1	X	THERMWR3	THERMRD2		X	SW_VCAL	X	RELAY_LO_HI	X	X
Bit 19	0	X	X	RSEL 0	X	X	X	DATA 6	CHANNEL 2	CHANNEL 2	DATA 8	DATA 0	X	THERMWR2	THERMRD1		X	CKR_FS1	X	RELAY_EN	X	X
Bit 18	0	X	X	1	X	X	X	DATA 5	CHANNEL 1	CHANNEL 1	DATA 7	X	X	THERMWR1	THERMRD0		X	CKR_FS0	X	AOVER_EN	X	X
Bit 17	1	X	X	1	X	X	X	DATA 4	CHANNEL 0	CHANNEL 0	DATA 6	X	X	THERMWR0	X		X	CLK_MODE	X	DOVER_EN	X	X
Bit 16	0	X	X	1	X	X	X	DATA 3	DATA 13	X	DATA 5	X	X	DATA8	X		X	DRIVER_MODE	X	IVDD_GAIN1	X	X
Bit 15	0	X	X	CHANNEL 2	X	X	X	DATA 2	DATA 12	X	DATA 4	X	X	DATA7	X		X	PICT_DO -/+	X	IVDD_GAIN0	X	X
Bit 14	1	X	X	CHANNEL 1	X	X	X	DATA 1	DATA 11	X	DATA 3	X	X	DATA6	X		X	X	X	IVDDA_GAIN1	X	X
Bit 13	FILTER 11	X	X	CHANNEL 0	X	X	X	DATA 0	DATA 10	X	DATA 2	X	X	DATA5	X		X	X	X	IVDDA_GAIN0	X	X
Bit 12	FILTER 10	X	X	0	X	X	X	X	DATA 9	X	DATA 1	X	X	DATA4	X		X	X	X	IVCCA_GAIN1	X	X
Bit 11	FILTER 9	X	X	1	X	X	X	X	DATA 8	X	DATA 0	X	X	DATA3	X		X	X	X	IVCCA_GAIN0	X	X
Bit 10	FILTER 8	X	X	REGISTER 1	X	X	X	X	DATA 7	X	X	X	X	DATA2	X		X	X	X	LEAK_GAIN1	X	X
Bit 9	FILTER 7	X	X	REGISTER 0	X	X	X	X	DATA 6	X	X	X	X	DATA1	X		X	X	X	LEAK_GAIN0	X	X
Bit 8	FILTER 6	X	X	0	X	X	X	X	DATA 5	X	X	X	X	DATA 0	X		X	X	X	CAPM_GAIN1	X	X
Bit 7	FILTER 5	X	X	CONVST	X	X	X	X	DATA 4	X	X	X	X	X	X		X	X	X	CAPM_GAIN0	X	X
Bit 6	FILTER 4	X	X	0	X	X	X	X	DATA 3	X	X	X	X	X	X		X	X	X	AOVER_GAIN1	X	X
Bit 5	FILTER 3	X	X	CAL SELECT 1	X	X	X	X	DATA 2	X	X	X	X	X	X		X	X	X	AOVER_GAIN0	X	X
Bit 4	FILTER 2	X	X	CAL SELECT 0	X	X	X	X	DATA 1	X	X	X	X	X	X		X	X	X	DOVER_GAIN1	X	X
Bit 3	FILTER 1	X	X	START CAL	X	X	X	X	DATA 0	X	X	X	X	X	X		X	X	X	DOVER_GAIN0	X	X
Bit 2	FILTER 0	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X
Bit 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X
Bit 0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X

ACMJ 9/01

used only by vhdI
device command
padding to end of command word

- This allows configuring one of 5 DACs (total of 68 channels), 2 ADCs (total of 23 channels), two thermometers, two delay chips, and many individual control bits.
- Two general purpose internal registers (SetUp and Control) contain most bits.
- Protocol operates at 1MHz clock rate to avoid any timing problems with TPLL/PICT and local chips.

•Where possible, information is readback as well, using the same 32-bit format:

PICT Return Data																					
	Write7711Ctrl	Read7711Ctrl	Read7711Data	Write7856Ctrl	Read7856Reg		Start7856	ADC_BusyInquire	Write5323	Write5532	Write5541	Read5532	Set9500Delay	Therm_BusyInquire	WriteTherm	ReadTherm	SetupReg	ReadSetupReg	ControlReg	ReadControlReg	FPGAalive
	(none)			(none)	Data Register	Status Register			(none)	(none)		(none)		X	(none)		(none)		(none)		
Bit 31		X	X		X	X	X	X	X			X		X		X		X		X	X
Bit 30		X	X		X	X	X	X	X			X		X		X		X		X	X
Bit 29		X	X		X	X	X	X	X			X		X		X		X		X	X
Bit 28		X	X		X	X	X	X	X			X		X		X		X		X	X
Bit 27		X	X		X	X	X	X	X			X		X		X		X		X	X
Bit 26		X	X		X	X	X	X	X			X		X		X		X		X	X
Bit 25		X	X		X	X	X	X	X			X		X		X		X		X	X
Bit 24		X	X		X	X	X	X	X			X		X		X		X		CAPTEST_EN	X
Bit 23		X	DATA 23		X	X	X	X	X			X		X		X		X		REFRESET_EN	X
Bit 22		X	DATA 22		X	X	X	X	X			X		X		X		X		GA3_EN	X
Bit 21		MODE 2	DATA 21		X	X	X	X	X			X		X		X		X		GA2_EN	X
Bit 20		MODE 1	DATA 20		X	X	X	X	X			X		X		X		X		GA1_EN	X
Bit 19		MODE 0	DATA 19		X	X	X	X	X			X		X		X		X		GA0_EN	X
Bit 18		GAIN 2	DATA 18		X	X	X	X	X			X		X		X		X		RELAY_LO	X
Bit 17		GAIN 1	DATA 17		X	X	X	X	X			X		X		X		X		RELAY_HI	X
Bit 16		GAIN 0	DATA 16		X	X	X	X	X			X		X		X		X		RELAY_EN	X
Bit 15		0	DATA 15		DATA 15	0	DATA 15	X	X			X		X		X		X		AOVER_EN	1
Bit 14		0	DATA 14		DATA 14	BUSY	DATA 14	X	X			X		X		X		X		DOVER_EN	1
Bit 13		1	DATA 13		DATA 13	1	DATA 13	X	X			DATA 13		X		X		X		IVDD_GAIN1	0
Bit 12		0	DATA 12		DATA 12	CHANNEL 2	DATA 12	X	X			DATA 12		X		DATA 8		PCC/PICT		IVDD_GAIN0	1
Bit 11		0	DATA 11		DATA 11	CHANNEL 1	DATA 11	X	DATA 11			DATA 11		X		DATA 7		CAPTEST		IVDDA_GAIN1	1
Bit 10		1	DATA 10		DATA 10	CHANNEL 0	DATA 10	X	DATA 10			DATA 10		X		DATA 6		REFRESET		IVDDA_GAIN0	1
Bit 9		FILTER 11	DATA 9		DATA 9	0	DATA 9	X	DATA 9			DATA 9		X		DATA 5		GA3		IVCCA_GAIN1	0
Bit 8		FILTER 10	DATA 8		DATA 8	1	DATA 8	X	DATA 8			DATA 8		X		DATA 4		GA2		IVCCA_GAIN0	1
Bit 7		FILTER 9	DATA 7		DATA 7	REGISTER 1	DATA 7	X	DATA 7			DATA 7		X		DATA 3		GA1		LEAK_GAIN1	1
Bit 6		FILTER 8	DATA 6		DATA 6	REGISTER 0	DATA 6	X	DATA 6			DATA 6		X		DATA 2		GA0		LEAK_GAIN0	0
Bit 5		FILTER 7	DATA 5		DATA 5	0	DATA 5	X	DATA 5			DATA 5		X		DATA 1		SW_VCAL		CAPM_GAIN1	1
Bit 4		FILTER 6	DATA 4		DATA 4	X	DATA 4	X	DATA 4			DATA 4		X		DATA 0		CKR_FS1		CAPM_GAIN0	0
Bit 3		FILTER 5	DATA 3		DATA 3	0	DATA 3	X	DATA 3			DATA 3		X		X		CKR_FS0		AOVER_GAIN1	1
Bit 2		FILTER 4	DATA 2		DATA 2	CAL SELECT 1	DATA 2	X	DATA 2			DATA 2		X		X		CLK_MODE		AOVER_GAIN0	1
Bit 1		FILTER 3	DATA 1		DATA 1	CAL SELECT 0	DATA 1	BUSY 1: 7711	DATA 1			DATA 1		X		X		DRIVER_MODE		DOVER_GAIN1	0
Bit 0		FILTER 2	DATA 0		DATA 0	START CAL	DATA 0	BUSY 0: 7856	DATA 0			DATA 0		Therm_Busy		X		PICT_DO +/-		DOVER_GAIN0	1
Bit 31		FILTER 1																			
Bit 30		FILTER 0																			

- First pass at VHDL is complete. Note it is fairly simple because the PICT operates as a pure slave to TPLL, with no autonomous clock.
- Header/trailer bits are added by TPLL, and checked by PICT and TPLL. Command format above is mapped in simple way into the individual serial command streams needed for individual chips on PICT.

TPCC Status:

- After PICT is finished, will extract subset of schematic and make new TPCC. The new TPCC should support most lab/testbeam module testing.
- Included features from the PICT are improved Strobe delay, new dual 16-bit VCal chopper, ADC for module temperature measurement, but no I/V monitoring of chip power supplies (should use GPIB controlled lab supplies to provide this).
- Intend to include limited multi-module support. This would include four 50-pin output connectors, and four independent power supply connections (including support for second analog supply ?).
- Power supplies would be treated as on the LBL PCC, not as on the Siegen PCC. There would be an input connector for a cable to be connected to lab supplies, but there would be no power management circuitry (regulators, etc.) on the TPCC itself. This gives us more flexibility and simplifies development, particularly for multi-modules where we want independent floating supplies for each module, features best provided by commercial linear low-noise lab supplies.
- The board would provide control (via mask registers) of which of the four output connectors would receive XCK, which would receive output signals like DCI, STR, SYNC RSI and LVL1, and which would be allowed to send DTO and DTO2, as well as temperature data, back to the TPLL.
- Work on this card would start as soon as the PICT is under control. Would hope to deliver some boards already on March timescale.

New Support Cards for FE-I

- With the change in operating voltages and pinout, all presently existing support cards must be updated.
- Described cards in detail in Oct pixel week, and this information is attached here for reference.
- Presently working on two basic single chip support cards (50-pin card for use with PCC/TPCC and 100-pin card for use with PICT). We will fabricate these cards in December, and will be able to supply them for single chip testing.
- John is working on the lay out of a simple rectangular passive probe card. This will define the card-edge connector pin-out needed for adapter cards.
- Then will proceed to modify 50-pin and 100-pin single chip cards to connect to probe card instead. This will support either PCC/TPCC-based probing or full PICT probing, depending on which card is used.
- This probe adapter-card approach was used for all probing so far, and has worked fairly well. For production probing, intend to develop integrated probe card in collaboration with Bonn. This will be strongly influenced by tooling adopted for single-die probing and bare-module probing.

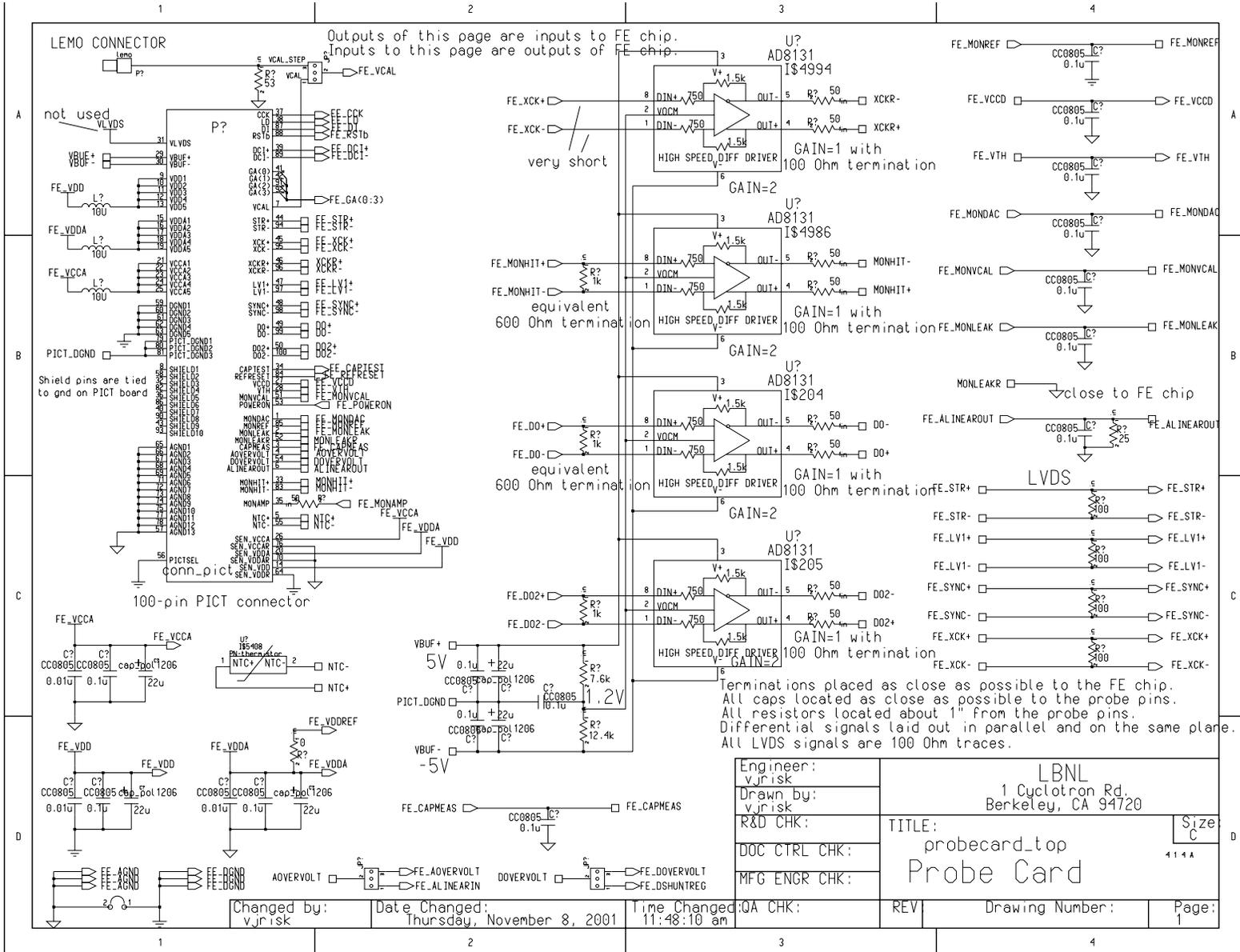
Single Chip Card (50-pin TPCC connector):

- Only active component would be the LVDS Buffer chip. It would convert the incoming LVDS signals for RSTb, LD, DI, and CCK to CMOS, and serve as a repeater for the DO, MonHit, and XCKR signals.
- Provide test header connections for new signals in FE-I for lab evaluation.
- Complete list of test signals on FE-I includes: RefReset, PowerOn, CapTest, DOvervoltage, DShuntReg, AOvervoltage, ALinearRegIn, ALinearRegOut, MonDAC, MonLeak, MonRef, MonVCal, MonAmp, and CapMeasure.
- If the user did not want to test or operate the special blocks, then only the central 30 pins would need to be wire-bonded. There will be an indication on the board which pads are part of this required bonding pattern.

Probe Adapter Card (100-pin PICT connector):

- Use AD8131 differential video buffer for high-performance buffering of LVDS outputs. This makes the testing dependent only on the speed of a commercial 400MHz part, and allows us to measure the true performance of the chips and modules we want to test.
- The buffered outputs include: DTO, DTO2, MonHit, and XCKR.
- No other active components are required, because PICT generates correct signal levels for all inputs directly. The PICT connector provides the +/-5V power necessary to operate the high-speed buffers.

- For the wafer probe card, initially plan a simple adapter card to carry the needed circuitry for the interface to the PICT. This would be combined with a standard rectangular probe card with card-edge interface. Schematic is now "frozen":



Single Chip Support Card for PICT (100-pin PICT connector):

- This card would be based on the same schematic as the probe adapter card, using the AD8131 buffers instead of the LVDS Buffer chip.
- It would allow testing of single chips with the full power of the PICT to characterize amplitude and timing margins, as well as performing measurements on the additional specialized blocks in the FE-I chip. This would be essential for careful studies of the design, and could be very useful for detailed irradiation studies.

Flex Support Adapter Card (50-pin TPCC connector):

- For Flex3 and Flex4, this is intended to be a very simple card which uses a card-edge connector to mate with the Flex Support Card being designed by Bonn.
- It would also use the 50-pin TPCC connector interface.
- It would use the LVDS buffer chip to convert RS1b signal from differential to CMOS for the MCC-I and would act as an LVDS repeater for returning XCKR signal.
- This very simple card would be finalized once the exact pin definition and geometry of the card-edge connection to the Flex Support Card is finalized.
- A PICT version could also be built if we want to have the ability to fully characterize the MCC LVDS I/O performance (XCK and DCI inputs, DTO and DTO2 outputs). This capability is supported by the PICT, and would just require an adapter card based on the same schematic as the Probe Adapter Card, with a slightly different card-edge connector.