

# Status of ROD Crate Hardware

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## **ROD and BOC status:**

- Pre-production RODs
- Simple BOC for lab testing without opto-links
- Pre-production BOCs (BOC1)

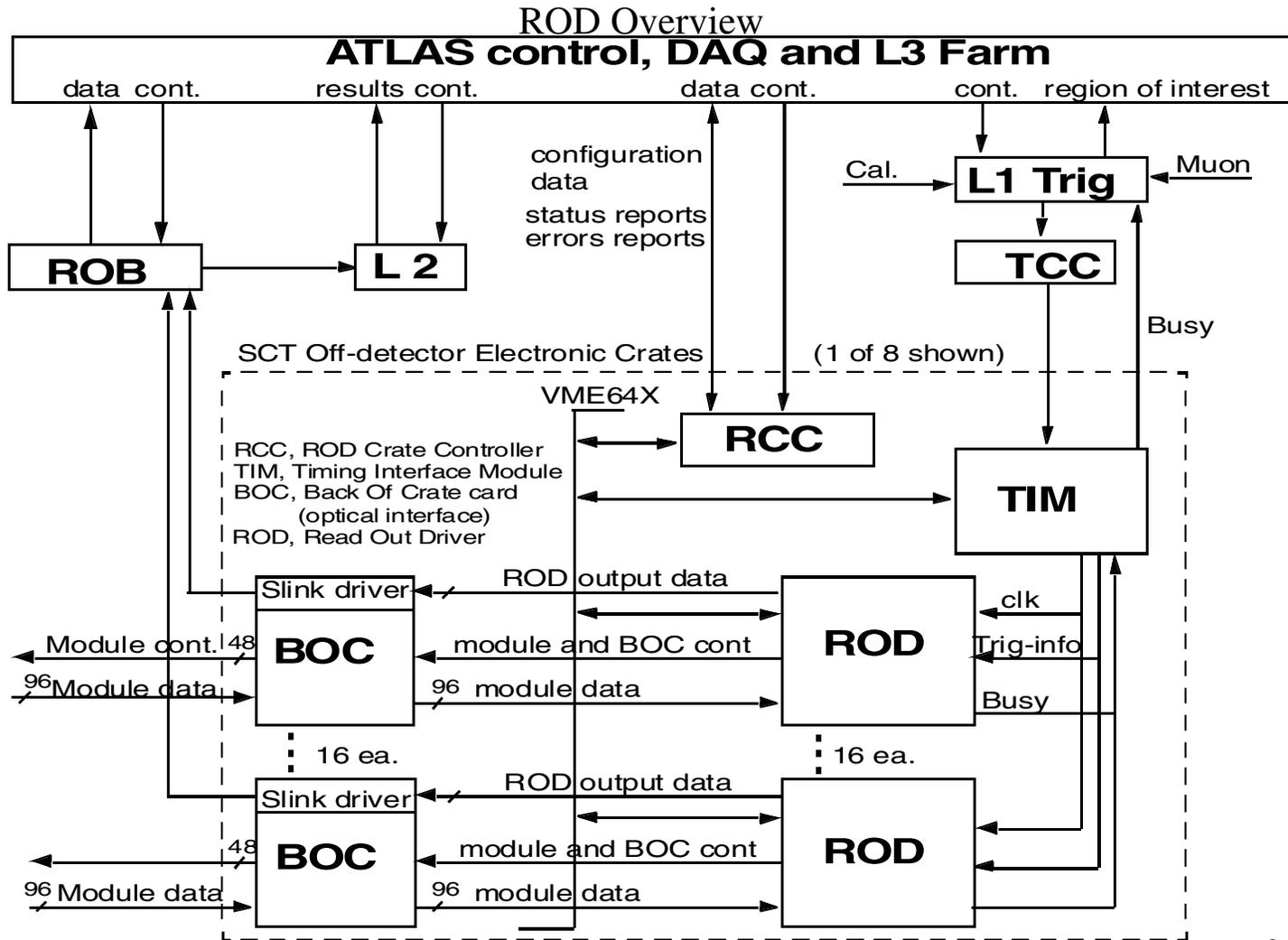
## **Related issues:**

- Assignment of modules to RODs and RODs to crates in USA15
- TTC partitioning in USA15

# System Block Diagram

## Reminder of what the blocks are:

- ROD Crate includes 16 (ROD+BOC) cards (two groups of 8, with TIM in center), one TIM, and one RCC, sitting in a 9U VME64x crate with a custom backplane.



## Status of ROD Prototype

### First ROD prototypes:

- Three boards fabricated. Two boards fully loaded and debugged.
- First system test took place in Cambridge in June. Operation of a TIM driving the special backplane, with a ROD and a BOC, was demonstrated.
- Development and testing has continued with one of these boards at LBL. About 60 million simulated events have been run through the data paths, with no errors found in data captured by back-end DSPs.
- Numerous fixes, incorporating everything learned over 5 month debugging period, were made to schematics during July through Sept. Almost all of the corresponding VHDL upgrades are now complete, with the exception of the Controller FPGA (still about 25% of changes to implement).
- Board changes included upgrading of controller FPGA from Virtex to Virtex-E 600 part, upgrade of router FPGA from Virtex-E 200 to 300 part, and upgrade of program manager FPGA to Virtex-E part (no Virtex used on ROD anymore). Also, DSP SDRAM was upgraded from 16MB to 32MB.
- Fifteen new PC boards now fabricated. Four boards are out for loading and expected back Dec. 4. Expect to deliver these 4 boards (one is for pixels) during January 02. Additional boards will be loaded later in 2002.
- These boards will be the pre-production version of the ROD.

## Plans for pre-production RODs:

- The first pixel pre-production ROD will reside at LBL for initial hardware and software development.
- The first goal will be to focus on evaluating the hardware by using it to operate modules in the lab in a “calibration” mode. Scans of various types would be implemented (threshold, TOT, timewalk).
- This would be an evaluation of the ROD hardware/firmware, and also the beginnings of a system test.
- After evaluation of these first 4 boards by SCT and pixels, additional 8-10 boards will be loaded and delivered. Pixels expects to receive 2-3 additional boards by Summer 02. These boards will allow pixels to carry out system testing in 2-3 sites, and develop opto-link support in another site.
- The number and timing for these additional boards could be somewhat flexible, depending on pixel needs. There will be the need for continuing hardware evaluation of the ROD (LBL + Genova ?), for system tests (LBL + Bonn + Genova ?), for BOC and opto-link hardware evaluation and software development (OSU + ?), and for testbeam and DAQ-1 software development (LBL + Genova + ?). Note also that Iowa is involved generally (SCT+pixel) as a member of the ROD development team.
- The user evaluation period for these boards would extend until Fall 02.

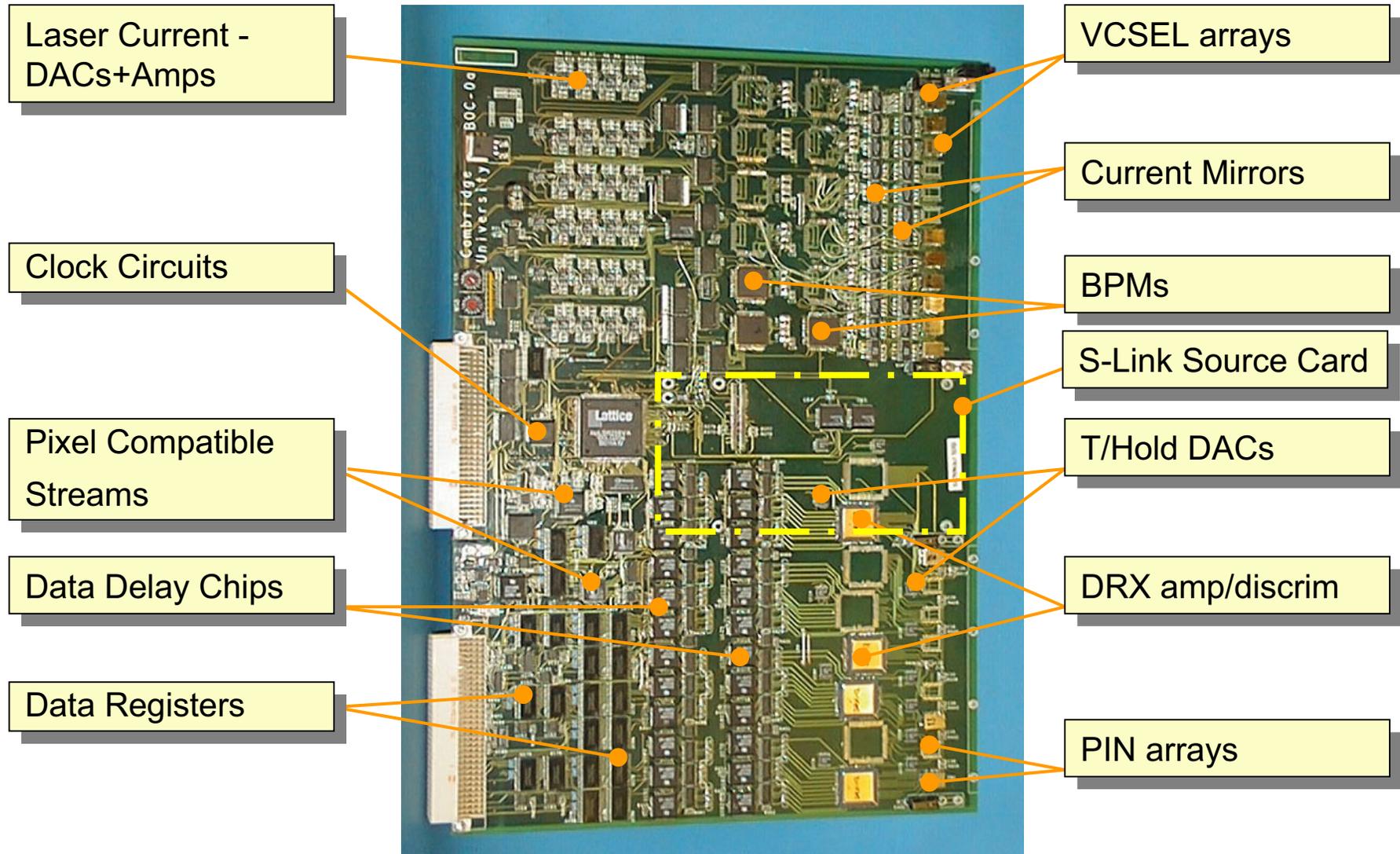
## Simple BOC proposal:

- Support two 6/7 module groups, including operation at 80 Mbits.
- Generate 40MHz clock locally on BOC to eliminate the need for a TIM module in this simple single ROD system.
- Transmit groups of signals to 6/7 modules. Each module group would contain a single XCK and seven DCI links down to daughter card using LVDS drivers.
- Use local LVDS repeaters and clock fanout chip on daughter card to regenerate high-quality signals and drive individual Type 0 cables from PP0.
- Daughter card would use LVDS repeaters to regenerate XCKR, DTO, and DTO2, and send them back to the simple BOC.
- Use individual clock recovery chips (RoboClock used in all PLL modules) to recover clock, and provide local jumper-based phase adjustment. Use of XCKR simplifies timing, and makes it largely independent of cable length.
- Correctly resynchronize the data with the 40MHz BOC clock, and feed the data into the ROD.
- Simple BOC would have no control registers, and a total of about 25-30 simple chips running at 3.3V on it. Replacement for opto-daughter card would have about 28 tiny LVDS repeater chips and a clock fanout chip, all running on a single 3.3V supply. A 25 pair data transmission cable would be used, and would support operation of the system with a cable length of at least 10 meters.

## Status of BOC Prototypes

- BOC for both SCT and pixels is a development carried out at Cambridge and led by Maurice Goodrick. Pixels will get the BOC design for free, but will pay materials cost for board fabrication and parts loading.
- Initial BOC prototype, referred to as BOC0, was fabricated using 4-channel opto-chips. This board included the full link count required for SCT (48 TTC links, 96 data links), as well as some circuitry for 80 Mbit pixel links.
- It served as a test-bed for many issues in BOC design. A second test module was developed to interface to BOC Setup Bus from VME, to interface to SCT test modules, and to create simulated datastreams (including 80Mbit pixel data).
- The performance of BOC0 has been almost completely evaluated, including clock jitter, bit error rates, and operation with real SCT modules (S-link tests still waiting for missing hardware). Basic design, which relies on fast PLDs, was shown to meet timing requirements.
- Recently held a review of BOC work on Nov 15 (LBL participated by phone for several hours), in which BOC0 results plus BOC1 design and schematics were covered in detail. Minor updates needed, but overall design looked good.
- Pre-production version is referred to as BOC1. It is based on production concept for all optical components (12-way transmit and receive modules). Fabrication of 10 boards will start during December. Pixels will receive 3 boards.

## BOC0 Prototype:



- BOC0 was very full, in part because of 4-channel pre-production links.

## Summary of adjustments implemented in BOC:

### Threshold adjustments:

- OptoRX containing DRX-12 has threshold adjustment for each channel, in range of 0-255 $\mu$ A. Scan with known bit pattern and measure BER to set safe threshold.

### Timing adjustments:

- BPM-12 has two types of adjustable delays for each output channel. One is in units of 25ns (range 0-31 beam crossings), and one is in units of 0.5ns (range 0-31ns). These delays are intended for adjustment of module timing in the experiment.
- Output of OptoRX modules pass through individual channels of PHOS4 delays chips (0-25ns delay in 1ns units using DLL locked to LHC 40MHz) to allow adjustment of return data timing.
- Global timing adjustments for internal clocks used for data recovery (LXA-clock, LXB-clock, LXV-clock) are made using PHOS4 chips. Similarly, global timing for internal clock used for data transmission (PX clock) is also made using PHOS4 chip.

## Description of BOC1 and Pixel Specifics

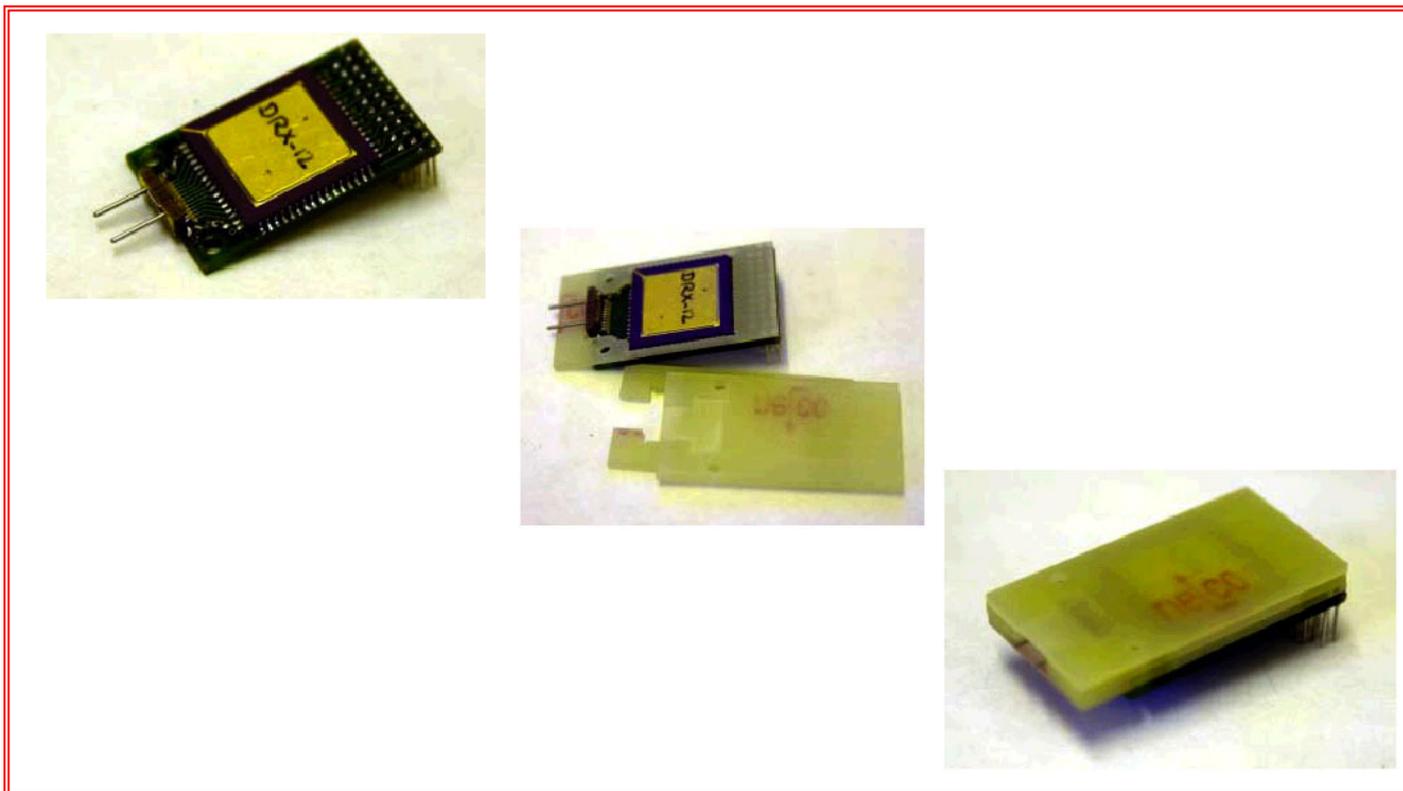
### Changes since BOC0:

- Finalized PC board geometry to fit in production 9U crates.
- Improved clocking circuitry, with redundant clock generation using on-board crystal, increased delay range adjustment, reduced jitter, and improved duty cycle (“mark-space ratio” in SCT jargon).
- Improved implementation of laser safety interlock.
- Major change is use of 12-channel production opto-modules.
- Implementation of 80Mbit decoding on multiple channels.

### Comments on pixel and SCT multiplicities:

- SCT system is built around 12-way opto-links and uses MT-12 connectors. Pixel system is built around 8-way opto-links and uses MT-8 connectors (of which only 6 or 7 links are active !)
- MT-12 and MT-8 connectors are compatible, with MT-8 links mapping to central 8 links of MT-12. BOC and ROD programming and partial loading are explicitly designed to cope with this.

## Production opto-modules:



- In-kind contribution from Taiwan for both SCT and pixels. Based on 12-way VCSEL and PIN arrays. First prototypes shown here.
- Small modules of about 20x30mm. OptoRX includes DRX-12 + multi-channel DACs + PIN array. OptoTX includes BPM-12 + multi-channel DACs + VCSEL array.
- Pixels connects to modules with MT-8, and uses 6 or 7 links among central 8.

## Pixel 80Mbit decoding:

- Implemented one channel of decoding on BOC0 and tested it with simulated data streams:

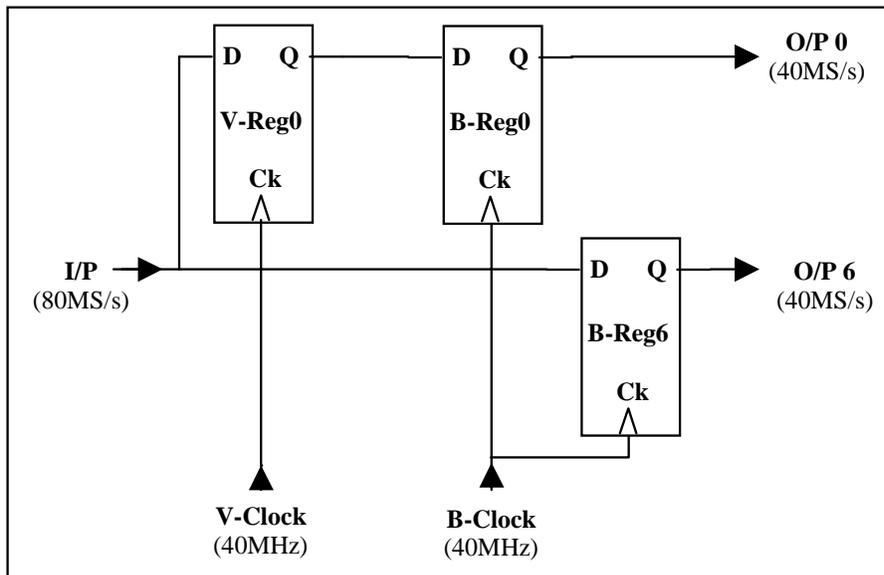


Figure 1: CPLD Configuration for De-Multiplexing

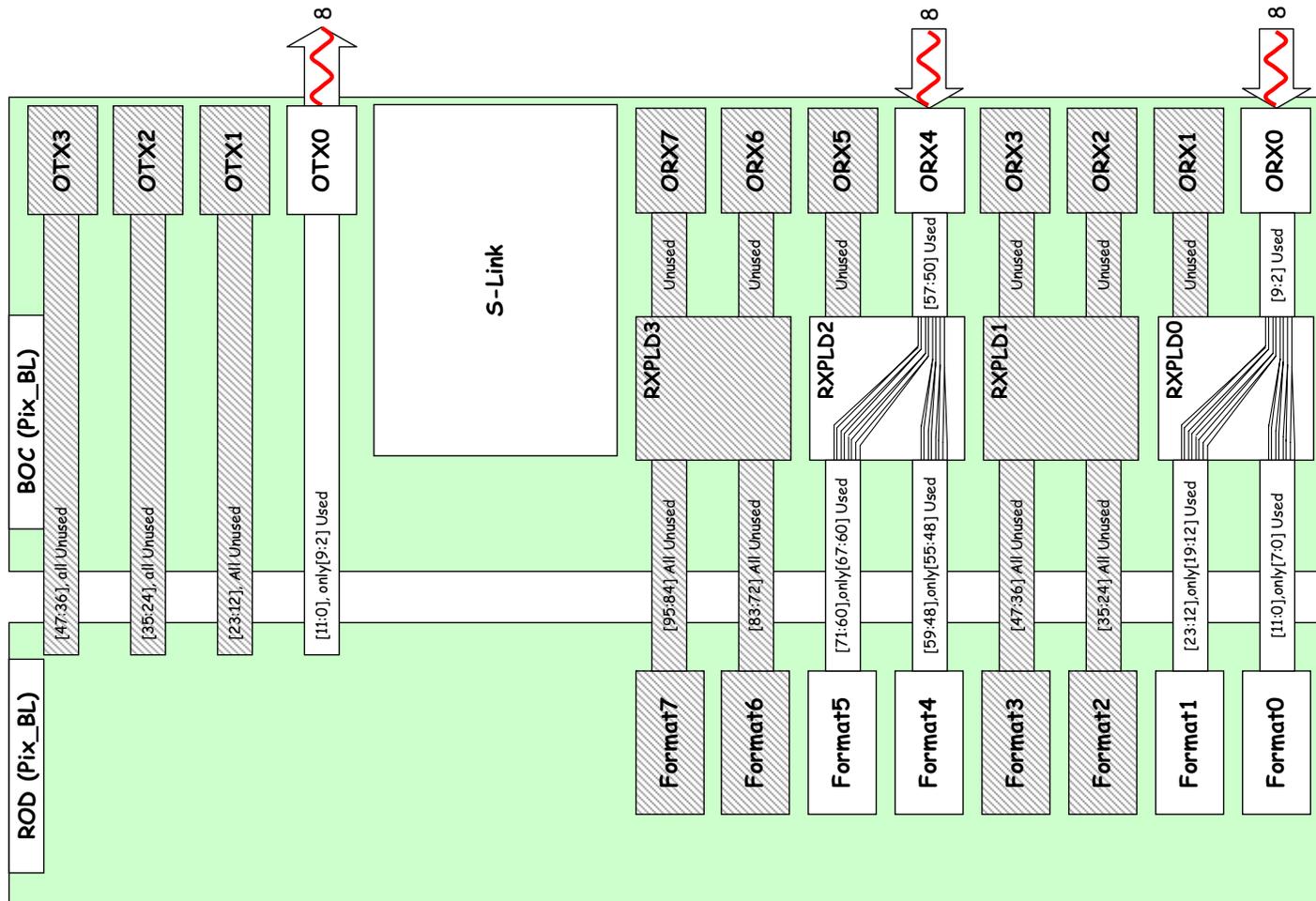
- Use two clocks for decoding. Timing of both V and B clocks is adjustable on BOC, and for this test, they were shifted by half period.

- Sample data streams were generated, and phase of data stream was adjusted using PHOS4 delay chip which is standard for return data in BOC.
- Found a working range of 10ns within which the data was correctly decoded.
- Concluded that this simple design works well for decoding 80Mbit streams.

## Configuration of BOC for Pixel Readout

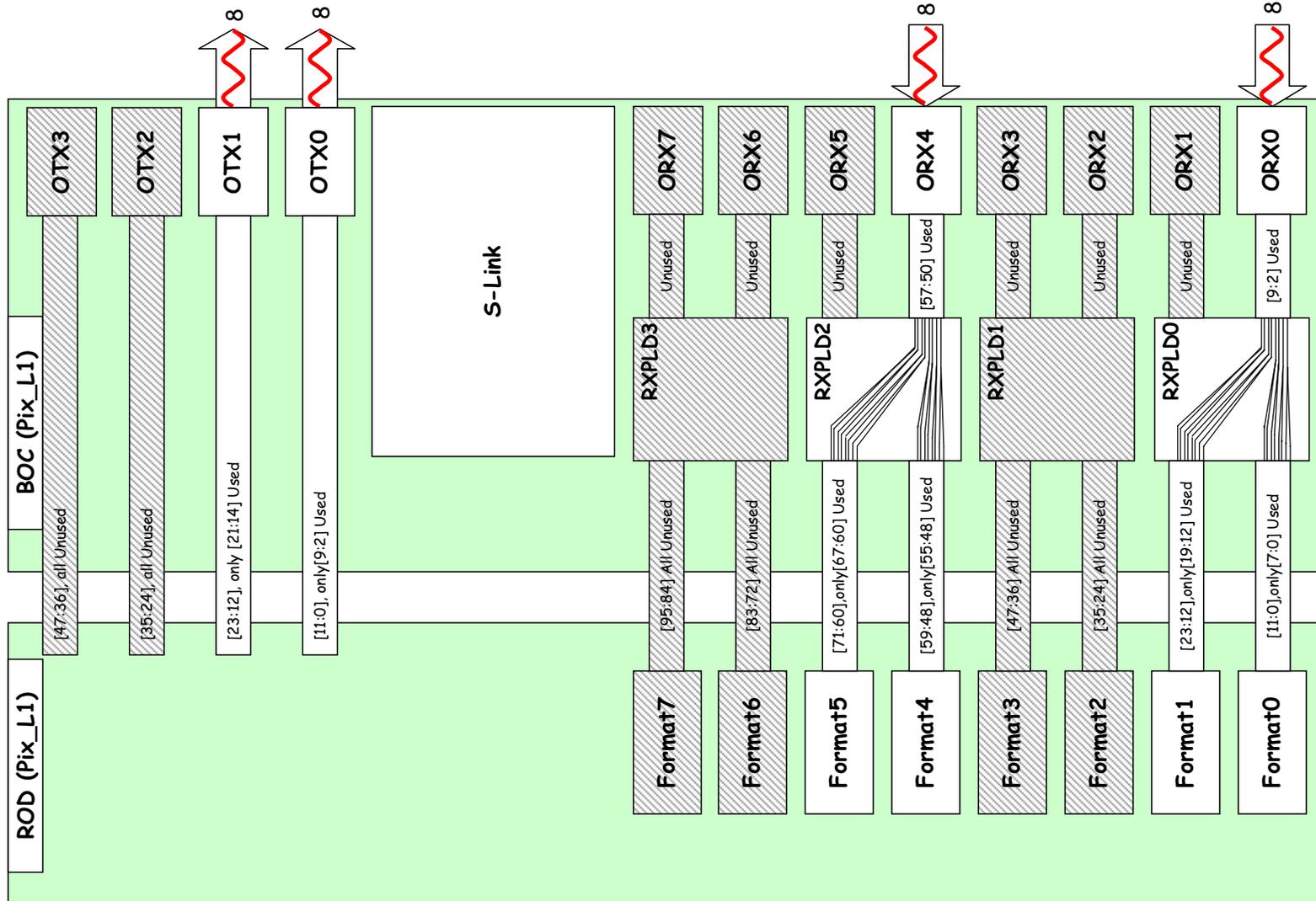
**Pixel system uses several different readout schemes:**

- B-Layer has two 80Mbit data links per module, and 6-7 modules per ROD:



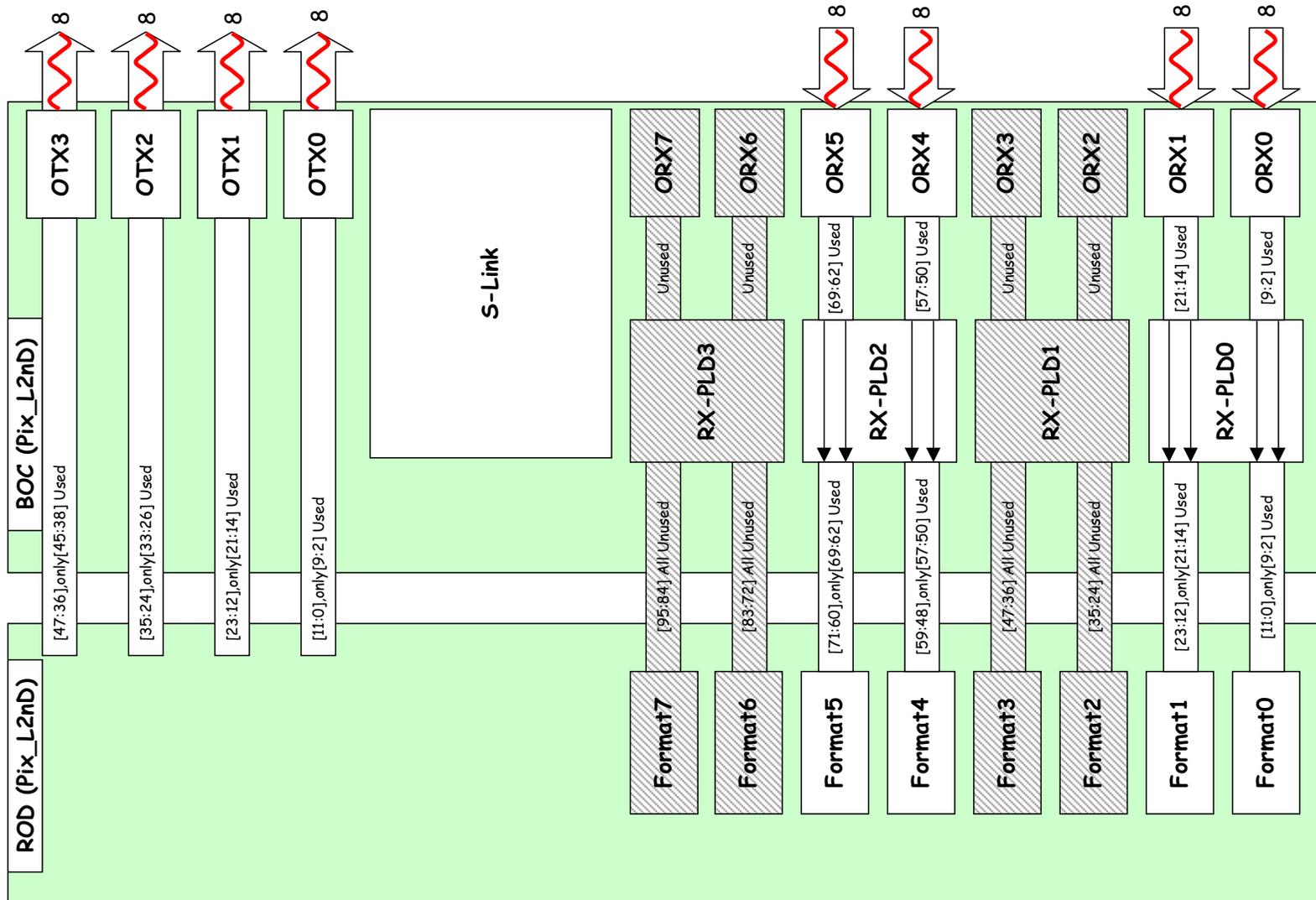
- Convention will be updated to use [2:9] of [0:11] everywhere (TTC and Data links)

- Layer 1 has 1 80Mbit link per module, and one stave of 13 modules per ROD:



- Convention will be updated to use [2:9] of [0:11] everywhere (TTC and Data links)

- Layer 2 + Disks have 1 40Mbit link per module, and 4 disk sectors (24) or 2 barrel staves (26) modules per ROD:



- Convention will be updated to use [2:9] of [0:11] everywhere (TTC and Data links)

## ROD Production Planning

### ROD Production:

- After the user evaluation period, large-scale procurements for production of SCT (and possibly pixel) RODs would begin.
- SCT wants significant number of RODs in macro-assembly sites by end of 2002.
- Exact timing of pixel ROD production will depend on results from user evaluation period.
- Present plan is to produce pixel RODs which are identical to SCT RODs (but loading only 50% of the formatter FPGAs).
- The pixel parts procurement would be done together with that for SCT in late 02.
- The SCT and pixel ROD production would be done sequentially. This would lead to production of all RODs by early 2004, and is intended to minimize/control engineering costs.
- Pixels would be able to get some additional RODs, beyond the 3-4 pre-production boards delivered in 2002, in the first half of 2003 if necessary.

## Pixel ROD Configuration

### Module mapping already defined (for full 3-hit system):

- B-layer has half-stave per ROD, for a total of 44 RODs
- Layer 1 has one stave per ROD, for a total of 38 RODs
- Layer 2 has two staves per ROD, for a total of 26 RODs
- Disks have four sectors per ROD, for a total of 12 RODs

### Rod Rack layout (4 racks allocated in USA15):

- Assume only two ROD crates per rack because of complex service issues involved in bringing large numbers of opto-links in and out of BOC.
- Assume there is an additional 6U VME crate placed in the middle of the rack. This would contain the TTC electronics and any additional test/diagnostic electronics.

### TTC Partition proposal:

- Propose that B-layer is one partition of 3 ROD crates.
- Propose disks are a second partition of 1 ROD crate.
- Propose that Layer 1 and 2 are third partition of 4 ROD crates.
- Separating Layer 1 and Layer 2 into different TTC partitions would require two extra ROD crates, because there are only 16 slots per crate available for RODs.