

# Electronics Issues

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## **Status of front-end electronics**

- IBM engineering run status
- Testing preparations
- Organization of testing (production DB, probing of die and bare modules)

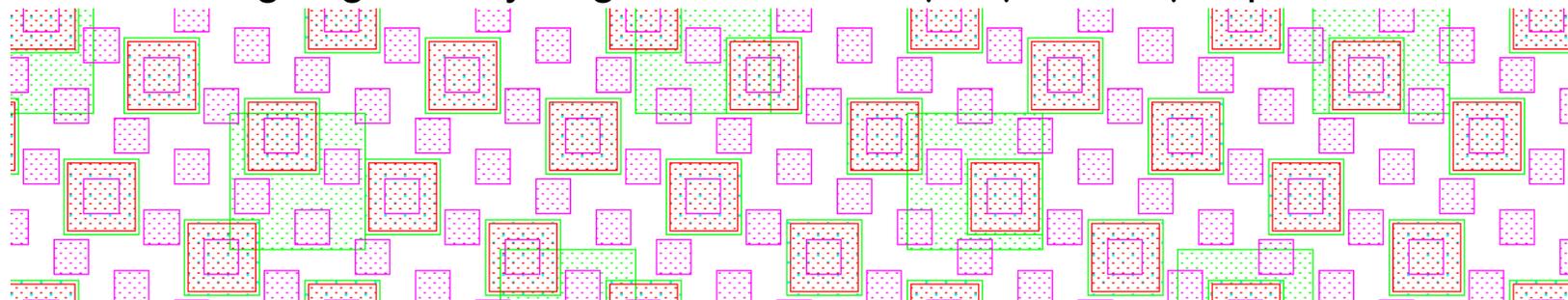
## **Additional electronics issues**

- Opto-electronics and opto-link issues
- Power supply and regulator prototype status
- Preparations for system tests: infrastructure (power supplies, monitoring)
- ROD Hardware and Software issues

## Status of FE-I Engineering Run

### Reticle and DRC Waivers accepted by IBM:

- Only one DRC error that we were required to fix (IBM did not accept our waiver request). This was in Analog Test chip, and was a violation of TV opening spacing rules in a capacitor array. The openings were removed, causing one day of delay.
- We received back the filled IBM GDS file (118 MB), and it looks correct. Fill was excluded over complete FE-I chips, DORIC preamp, CapTest chip, and Alignment Marks. Filling is generally large numbers of  $1\mu$ ,  $2\mu$ , and  $4\mu$  squares:



- CERN discovered IBM error in wafer map layout on Nov 27. Had switched the locations of “thin” and “fat” test structures, making dicing of FE-I to correct size very difficult. They are now re-done this, but it has caused some delay in wafer delivery.
- PO for additional 6 wafers now complete. Expect delivery of additional wafers within several weeks of initial run (or possibly even at the same time).
- No firm delivery date, but last half of January seems most likely. Should get more detailed information next week, after CERN-scheduled meeting with IBM. CERN has agreed to divide shipment in half, and forward wafers to Bonn and LBL.

## Reticle for FE-I Run

**All designs use same pads, and have logo for identification.**

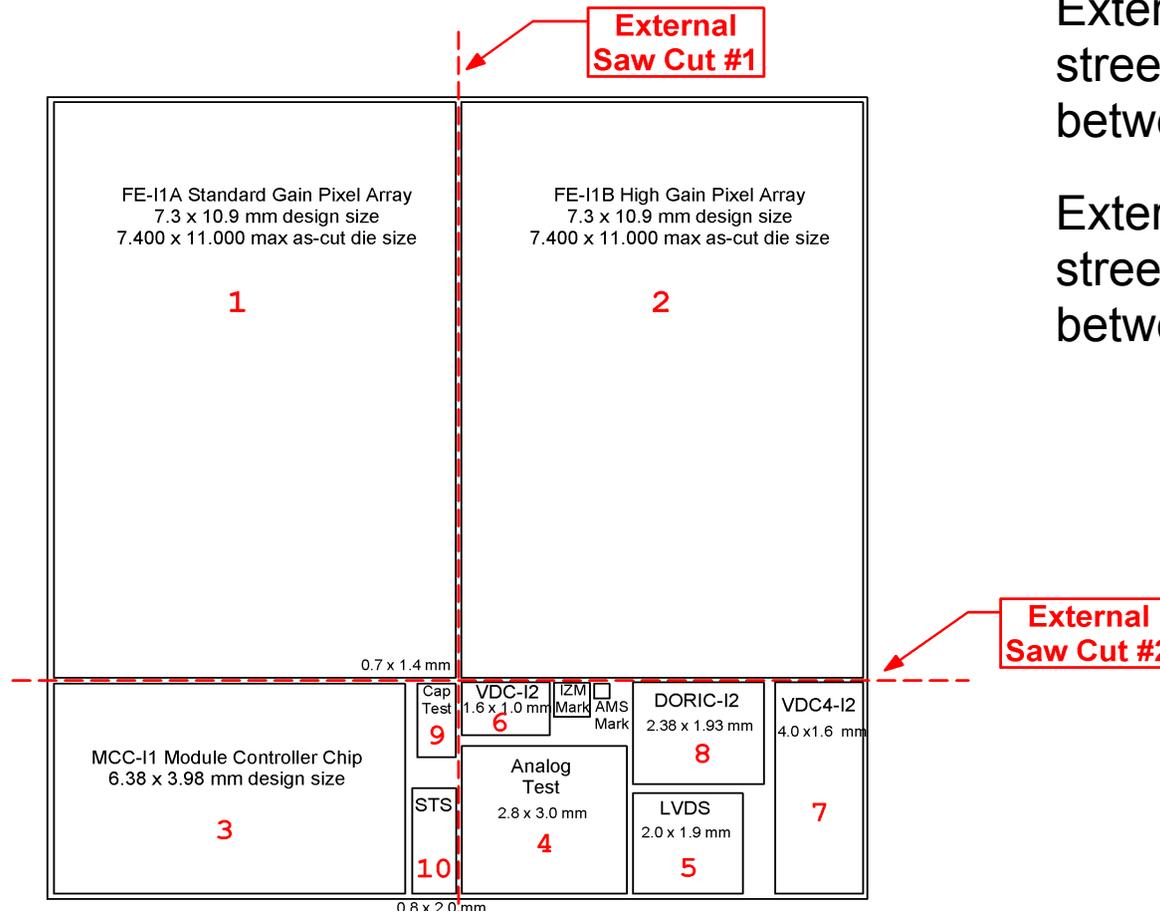
- **Two FE-I chips:** the left one is FE-I1A (10fF) and the right one is FE-I1B (5fF).
- **MCC-I chip:** this is the complete new MCC with U-pinout to satisfy module constraints.
- **DORIC-I and VDC-I chips:** they are improved versions of the designs submitted in the Feb MPW run, including 4-channel VDC. These are the “I2” generation.
- **Analog Test Chip:** this is very similar to the test chips fabricated in Feb/Mar with IBM and TSMC, but contains the final design and layout of all analog blocks, and 56 pixels instead of 20 (28 of each of the two types from FE-I)
- **LVDS Buffer Chip:** this is a convenient way to include the interface between a single chip and our test system into a rad-hard chip. It contains 4 LVDS->CMOS converters, 3 LVDS->LVDS repeaters (3.5mA outputs).
- **CapTest Chip:** this uses the CapMeasure circuit to provide characterization of all M1, M2, and M3 parasitics using a total of 64 test structures.
- **PM bar:** may be useful for checking details of device characteristics, although the very good parameter stability seen so far suggests it may no longer be needed. We have taken the CERN test structure and converted it to a 5-metal layout.
- **Alignment marks:** we have included the structure requested by Alenia and the one requested by IZM. These are for alignment of the wafer-scale bump masks.

# Final reticle layout:

Reticle size is: 14.700 (W) x 15.000 (L) mm.

IBM adds 138 $\mu$  in one direction and 378 $\mu$  in the other direction.  
 We choose to have the 138 $\mu$  added to the left/right of the reticle shown here,  
 and to have the 378 $\mu$  added above/below the reticle shown here. This allows us to meet  
 critical die dimension requirements on Die #1 and #2 with simple dicing procedure.

Reticle stepping increments with these rules are: 14.838 (W) x 15.378 (L) mm.



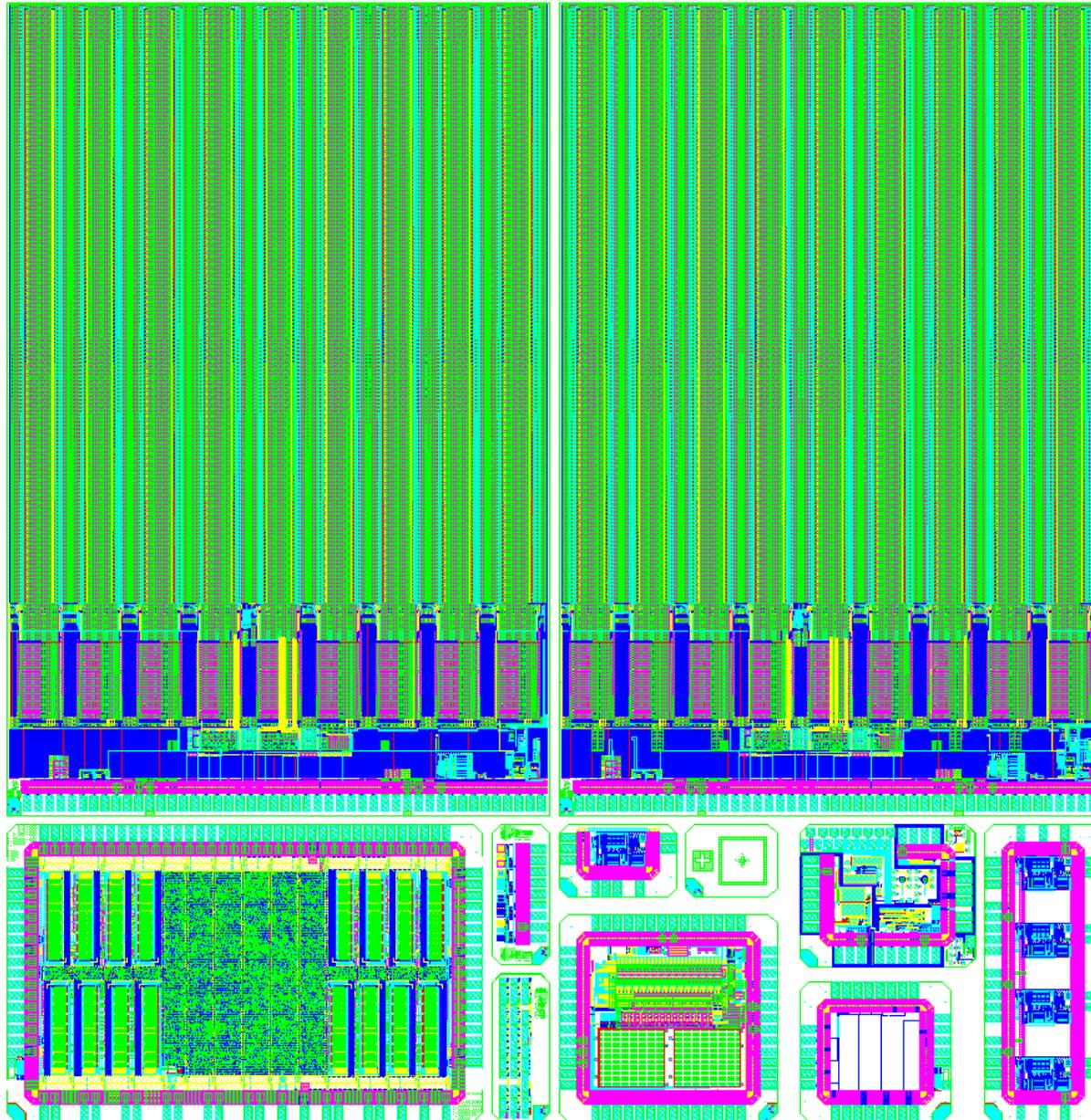
Internal streets are 120 $\mu$  between ChipGuards

External vertical streets are 160 $\mu$  between ChipGuards

External horizontal streets are 400 $\mu$  between ChipGuards

- FE chips can be diced directly without destroying other die. Other die will all require a second dicing pass to remove (even MCC, due to space constraints on Flex V4).

## GDS of Reticle:



Dicing will depend on wafer thickness, but typically will remove 60-100 $\mu$  of material. Assume minimum of 60 $\mu$

This will give diced size for FE-I of 7.36mm x 11.96mm.

After one pass, MCC would then be 7.36mm x 4.28mm.

Removing structures on the end of MCC would give a die size of 6.44mm x 4.28mm, compared to nominal design size of 6.38mm x 3.98mm.

Should assume size of 6.5mm x 4.3mm for Flex !



## Preparations for testing of 0.25 $\mu$ chips

### **For FE-I wafers, single chips, and modules with MCC-I:**

- New TPLL and PICT are planned route for FE-I wafer probing. They will allow very complete characterization of the FE-I chip and its many new features.
- Expect to deliver TPLL systems to LBL and Bonn for probing in early Jan 02. However, PICT delivery still not certain, and unlikely to be ready in time for initial probing.
- For this reason, Bonn will upgrade their FE-D probing system to make sure we can get a reasonable set of analog measurements. All wafers will be probed in both sites to compare test results (new larger bond pads reduce the risk !). Hope to have PICT available for “experimental” probing in LBL. If not, we will rely on Bonn analog measurements.
- Expect to deliver final TPLL and TPCC to the rest of the collaboration starting in about March 02. This is later than initially planned, but should be just in time for the arrival of bump-bonded FE-I parts.
- New single chip support cards and module adapter card will be fabricated during next two months. New FE-I pinout and new Flex Support Card from Bonn for Flex4 seem well-defined enough for LBL to go ahead with board layout immediately.

## For MCC-I:

- As soon as the first FE-I wafer is diced, Genova will receive MCC-I die for packaging. This will allow first testing of MCC-I with the full MCCEX system.
- Once tested die are available, some will be sent to LBL to complete testing of the TPLL VHDL code for the MCC-I. This will complete preparation of new test system.
- Genova intends to deliver a single wafer to a commercial IC testing firm in order to have them run a series of test vectors on it and characterize good chips. This wafer will be diced to provide large number of known good MCC-I die for Flex V4 loading.

## For opto-chips:

- After dicing of first FE-I wafer in LBL, die will be delivered to OSU for further packaging and distribution, as was done in the past for FE-D opto-parts.

## For LVDS Buffer Chip:

- Will do simple wafer probe and package directly into SOIC28 plastic packages and distribute. Defective parts can also be easily replaced when support board is tested.

## For Analog Test Chip

- Will update existing single-board test system used up to now at LBL. Plan to continue packaging parts in PLCC-68 package. Bonn will also work on this testing. Will send proposed bonding diagram around next week.

## Organization of testing for 0.25 $\mu$ chips

### Engineering run:

- Processed by IBM as two back-to-back runs of 6 wafers each, where the second run does not include any NRE costs. IBM will process both groups at the same time. Delivery of second group of wafers should occur at same time, but may be delayed by a few weeks if second PO not in to IBM on time.

### Wafer probing:

- CERN will divide wafer shipment into two, repackage in carriers, and ship to LBL and Bonn directly. IBM now provides notice of shipment, so paperwork can be prepared in advance.
- Proposal for first 6 wafers is to divide them into 2 groups of 3, and probe half in Bonn and half in LBL. The wafers would then be exchanged, and re-probed to complete testing of FE chips.
- One of the LBL wafers would then be completely diced as soon as possible, and would provide large numbers of die of each design type. These die would not be thinned. This wafer would probably be diced without double-probing, in order to expedite testing of other designs.

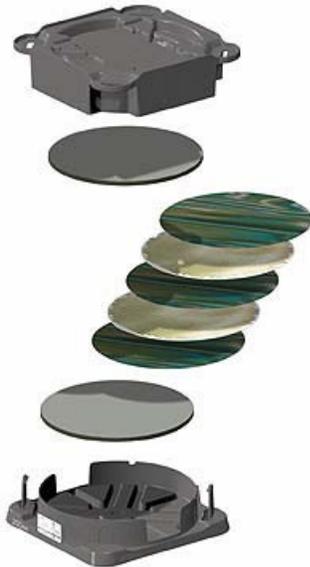
- One of the Bonn wafers would be given to Genova for commercial MCC-I testing at selected firm (Delta in Denmark). These MCC would be for Flex V4 module construction. This wafer should be thinned to  $300\mu$ , and then diced after testing. This could be handled by Genova or by LBL if Genova prefers.
- Remaining two sets of 2 wafers would be sent to IZM and AMS respectively.
- Opto-die harvested from fully diced wafer would be sent to OSU/Siegen/Wuppertal for testing. LVDS Buffers would be packaged by LBL for use with support cards.
- Second group of 6 wafers would be probed after the first set was sent off to bumping vendors. Would then probably be kept in reserve until first bumping results from first wafers are analyzed.

# Comment on shipping:

- It is quite clear that the IBM wafers will be shipped frequently to undergo the various processing steps. These wafers are expensive, and cannot be replaced.
- Recommend very careful shipping procedures, using proper wafer shipping containers. Example used by IBM:



## Horizontal Wafer Shippers



The Entegris Horizontal Wafer Shipper provides secure protection for processing, storage and shipping of 200mm or 150mm finished wafers. The system protects full thickness or thinned wafers from physical and electrostatic discharge and has low contamination characteristics, significantly reducing particulation, outgassing and ionics. The following order policies apply:

- Minimum order quantity 4 pieces: thereafter in quantities of 1 piece.
- **Accessories** sold separately: Inner Cushions / Carbon Leaf Inserts / Secondary Packaging
- **Check out our on-line stack calculator** to ensure the proper use of cushions and inserts!

System based on cushion and carbon leaf inserts. Simple web page for calculating inserts required to ship given wafer quantity.

Can be ordered directly from Entegris website.

Recommend that Bonn and LBL acquire minimum stock of parts, and make sure that all vendors and institutes shipping wafers use them.

Part Number	Description	Inventory	MOQ	Unit Price	Order Quantity	
HWS200-101A-61C02	Horizontal Wafer Shipper - 200 mm (8") wafers	--	4	--	<input type="text" value="4"/>	<a href="#">ADD TO CART</a>
HWS150-101-61C02	Horizontal Wafer Shipper - 150 mm (6") wafers	--	4	--	<input type="text" value="4"/>	<a href="#">ADD TO CART</a>

## Thinning, Dicing, and Die probing:

- Wafers are ordered “unthinned” with native 700 $\mu$  thickness. Expect that if dummy module program validates thinning vendor(s), and dummy modules made with thinned die have good yields, then all bumped wafers will be thinned prior to dicing.
- Should “fast track” one wafer each from IZM and AMS to bypass thinning to allow lab, testbeam, and irradiation work to proceed on modules as soon as possible.
- Bumped FE-I die should be re-probed after thinning and dicing, and flip-chip should use “known good bumped die”. Expect Bonn to handle IZM, LBL to handle AMS.
- If all goes well, initial 2+2 wafers (roughly 200 FE-I per wafer) could produce as many as 15+15 modules. We should be prepared for this possibility, although real numbers may be much smaller.

## Bare module probing:

- All bare modules returned from bumping vendors should be tested prior to being assembled into flex modules with Flex 4 hybrids.
- Many groups are working on performing bare module probing (Bonn, CPPM, LBL, Milano). Assuming we get many modules back, many groups should test modules.

## Production database preparation:

- As part of preparation of probing software for FE-I, LBL group intends to invest in creating a first version of the electronics database. Expect Genova should do something similar for MCC-I.

## Opto-link and opto-electronics developments

### Reached preliminary decisions on all outstanding issues.

- Agreed to base DORIC design on single-ended preamplifier to avoid problems with large VPIN and  $0.25\mu$  process limits. Since DORIC input is BPM-encoded clock, it is DC-balanced, and the DORIC can be AC-coupled. A first version of such a DORIC design (DORIC-I3) was included on IBM MPW6 run, submitted at end Nov.
- The present VDC uses the VDC power supply to also provide the bias for the VCSEL. Updated information from Taiwan suggests that we can select Truelight VCSELS to satisfy a 2.3V maximum post-rad forward voltage specification for 20mA current (this higher current is needed for annealing purposes after irradiation) by making sure that the pre-rad forward voltage is less than about 2.1V. DORIC and VDC would then be operated at 2.5V nominal supply voltage, leaving adequate margin for operation of VDC current source.
- Because this situation is somewhat marginal, propose to also assign opto-board connector pins to allow a separate VVCSEL to be brought to the opto-board. Prototype tests should be carried out to explore operation of opto-links with independent control of the VDC/DORIC supply voltage and the VCSEL bias voltage and make sure there are no major technical problems.
- Have begun task of re-evaluating the total light budgets in the opto-links. Present system has margin of only about 4db (factor of about 2.5). Propose to tighten DORIC spec to require low BER for input signal amplitudes of only  $20\mu$ A.

- At the strong request of Taiwan, we have agreed to modify the VDC design to support common-cathode VCSELs instead of common-anode VCSELs. This will allow use of VDCs to operate the present baseline opto-packages which use individual VCSEL and PIN die, as well as the proposed alternate connectorized package based on common-cathode VCSEL and PIN arrays.

## Propose to simplify opto-link services:

- The present opto-board interface will remain the same, with the exception of a minor change to remove the present VVDC\_Sense lines to PP0, and assign those pins to VVCSEL.
- There would be only a single VVDC supply connection per opto-card supported in the services from PP0 outwards. The VVDC\_Sense would be treated as it is now for the VDD and VDDA supplies on the module. A regulator would be assigned to VVDC at PP2, and would operate in remote sense mode.
- For now, VVCSEL would only be supported on opto-board connector, and would not be included in the rest of the services design. This could be revised in the near future, pending further test results. However, the probability of this seems low enough to continue as proposed here for now.

## Next steps:

- Need to finalize these preliminary decisions and propagate the results into the Services, Power Supply, and DORIC/VDC specification documents, as well as into the next-generation PP0 and opto-board prototypes.

## Power Supply status:

### Power Supply specifications:

- Specifications are clearly not yet final. However, we now have a new proposal for opto-link modularity, which would suggest two types of supply modules.
- One module would support an opto-board (VVDC, VPIN, VASET), and one would support a pixel module (VDDA, VDD, VDET). There are far fewer opto-link supply channels, and in principle, a pixel module channel could be used (dangerous for VPIN to be supplied from VDET channel of 700V).
- We have also not yet finalized the module multiplicity (how many modules per complex channel). Opto-board modularity is clearly one. Should we spec all pixel module supplies for modularity two ? Should we seriously request cost information for both modularity one and two ?
- We have also not finalized the voltage drops allowed for Type 4 cables. New services document proposes using 12V output supplies for critical voltages (VDD and VDDA), with 6V drop allowed in Type 4. This will reflect badly on power supply spec, and does not save much money in services. Need to optimize the total system of services+supplies, but suspect that 8V supply output is closer to the correct value.
- We (Kevin, Mauro, Susanne) need to make strong effort to create updated specification for Feb pixel week consistent with proposed new services design. This also meshes with timing of ATLAS-wide rack review during Feb pixel week.

## Prototype status:

- We have initiated prototyping efforts for three different solutions:
- **CAEN**: LV/HV complex channel system with a very intelligent mainframe
- **DPS**: LV/HV complex channel system with a less complex mainframe
- **ISEG/Wiener**: separate LV and HV channels with a “simple” mainframe
- All prototypes ordered have been delivered, and now have to be evaluated. DPS prototype has significant problems still, which are under discussion with the vendor. No prototype was ordered from Wiener.
- We need to define this evaluation process more clearly, and define its schedule. It must involve tests with FE-I modules, but there are only a few channels of each prototype available, so tests will be limited. First thoughts suggest it will take roughly until the end of 2002 to conclude the evaluation period.
- Until we have defined a vendor and a system, and finalized the requirements, we cannot begin to acquire any significant number of channels of each system (e.g. mainframes and many channels for system test purposes).
- Mainframes in particular present a large overhead (CAEN SY1527 is about 15KCHF) for getting systems running in several labs.
- Susanne and Mauro should work on defining how to complete the evaluation process and proceed to a vendor selection by late 2002/early 2003.

## Regulator status:

- Fourth generation of L4913 regulator appears to be a success. Delivering prototypes in small quantities now (Milano should have gotten 5 yesterday). These will be evaluated soon, particularly in remote sense configuration.
- Recent interactions with ST have suggested alternative configurations for use in remote sense operation (using ADJ pin instead of SENSE pin). This will also be explored in Milano.
- Design for PP2 at Milano is evolving to the level where one can begin prototyping something in the first half of 2002, depending on prototype regulator tests above.
- Presently discussing “remote sense” modification to L4913. The present design has a quiescent current of about 2% of the load current (measured to be 23mA at 1A output current). In a remote sense configuration, this current will flow in the sense return line, causing regulation problems, and requiring a large sense return wire.
- Proposal from ST is a modification in which the maximum quiescent current is about 10mA (hopefully less !) and is independent of the load current. This design change has apparently been implemented in the prototype run for the L7913 (negative regulator), and so we will know in March whether it works. If so, it will be implemented in the L4913, and a new prototype run will be made. Jarron is organizing the financing for this run, but ATLAS pixels could be responsible for contributing at the level of 10-20KCHF.

## Preparation for system tests in 2002

- We expect to get a significant number of functional modules from the FE-I runs. One of the most critical steps, once the modules are shown to work individually, is to proceed with multi-module testing, and a complete prototype of as many aspects of the final system as possible. Refer to this as “system test”.
- Proposal is that this test will use a ROD-based system for module readout, and will use realistic services (initially PP0 and Type 0 cables, later to be extended to include PP1 and Type 1 cables, then PP2 and Type 2/3/4 cables).
- Should also incorporate realistic power supplies, use of DCS for power supply control and temperature monitoring, and use of I-box for temperature interlock, as soon as these options become possible.
- The first version of this system should be ready by Summer 02, leading to a more complete version by early 2003. The first version will be too early for many system components to be ready.
- Propose a phased approach, with initial configuration based on: ROD with SimpleBOC using copper links with no TIM and no S-Link, GPIB-based lab power supplies, and perhaps limited DCS. Already at this time, would like 2-3 systems in collaboration (later needed for assembly sites), with support for 20-30 modules.
- Second phase would start to bring in real power supply prototypes, DCS with ELMB and CANbus, DAQ-1 environment, real opto-links, and should generally approach a full-scale prototype of the final system quite closely.

- Need to develop short-term solution for power supplies for system testing.
- Short-term solution should cover basic needs, including computer control (most likely GPIB, but other possibilities could be discussed), remote interlock, and remote sensing for LV supplies.
- For LV supplies, an example of an inexpensive lab supply is Agilent E3646A (dual channel 8V/3A, capable of operating two modules, roughly \$800 each) or Agilent E3648A (dual channel 8V/5A, barely capable of operating 4 modules, roughly \$1100 each). A mixture of these could allow us to evaluate multiplicity 1/2/4 for module powering in system test environment.
- For HV supplies, choices are more difficult. Susanne recommends ordering more of the ISEG 8-channel HV supplies. In principle, we are entitled to three 8-channel boards for evaluation under our prototype contract. This looks like the best solution for now.
- At least one setup should include prototype complex-channel power supplies delivered so far (CAEN, DPS). However, these require mainframe for operation.

## ROD hardware and software:

- Delivery of first pre-production ROD is only about one month away. other RODs will follow toward the middle of 2002. First realistic BOC1 would also likely be toward the middle of 2002.
- Need to begin planning and acquiring infrastructure for use of RODs. Expect there will initially be 3-4 setups in pixel collaboration. Present understanding is that these would be LBL (ROD hardware evaluation, software development, system test), Genova (ROD hardware evaluation, software development, system test), and Wuppertal (BOC hardware and software development, system test). Possible fourth site could be OSU (BOC hardware and software development).
- Groups who intend to participate in this effort need to acquire 9U VME crate (possibilities include purchase from Wiener or long-term loan from CERN pool). Depending on activities, will need a National Instruments MX-VXI setup, or a Concurrent Technologies SBC setup, or both.
- LBL will take responsibility to develop and provide SimpleBOC for copper-link based testing of modules in lab and testbeam. Do not expect realistic opto-link support before end of 2002.
- ROD Software group is starting to function. It is a joint SCT/pixel activity, and overlaps with DAQ-1 activity as well. Genova, Udine, LBL, and Iowa are involved on the pixel side. There are regular VRVS meetings (mainly audio).