

Electrical Services Issues for New Layout

K. Einsweiler, LBNL

Overview of non-optical services:

- Describe components, their interconnections, and power requirements

Decoupling/passives plan for modules and patchpanels:

- Where do passive components go ? What are issues for 0.25 μ chips ?

Concepts for power cables:

- Definition of different cable types and voltage drop goals

Grounding issues:

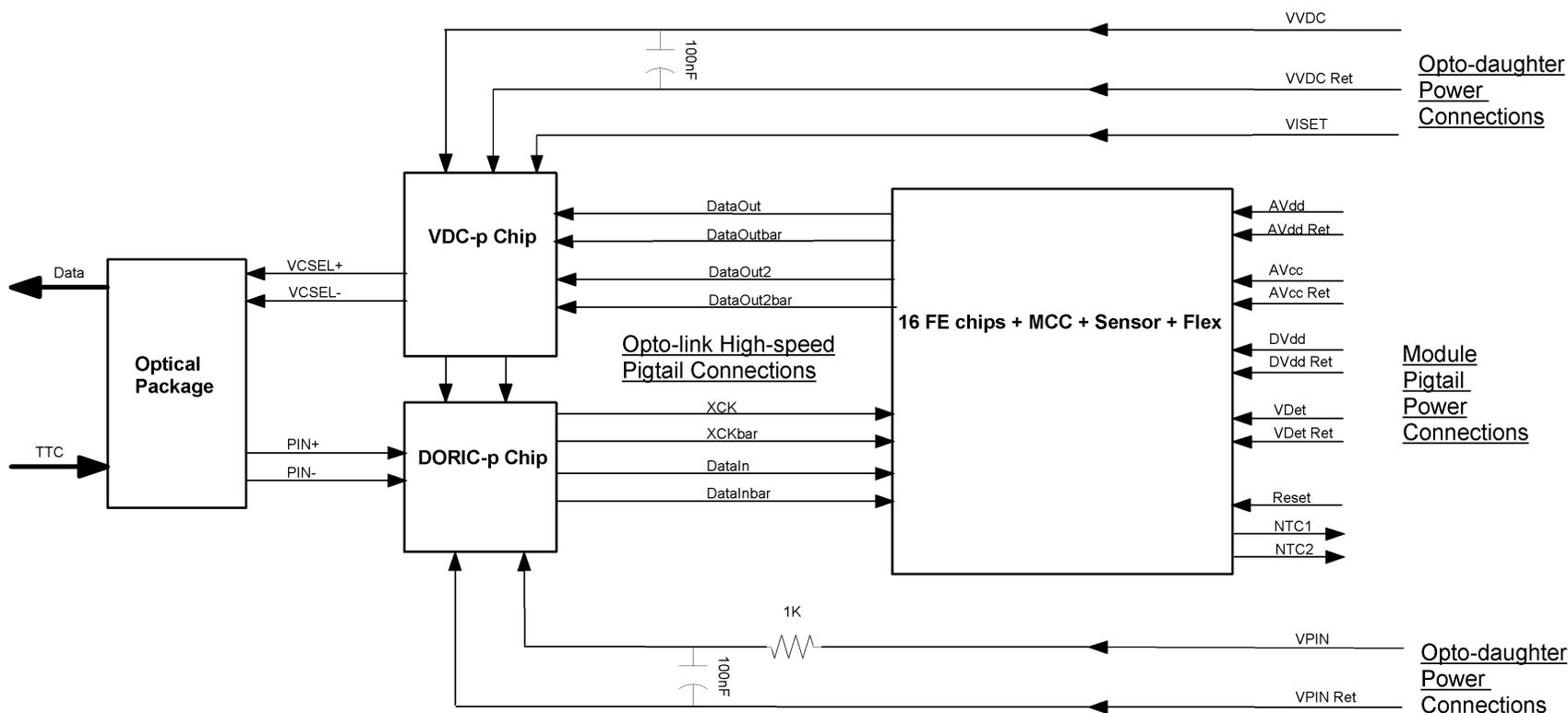
- Where/how are different grounds connected

Shielding issues:

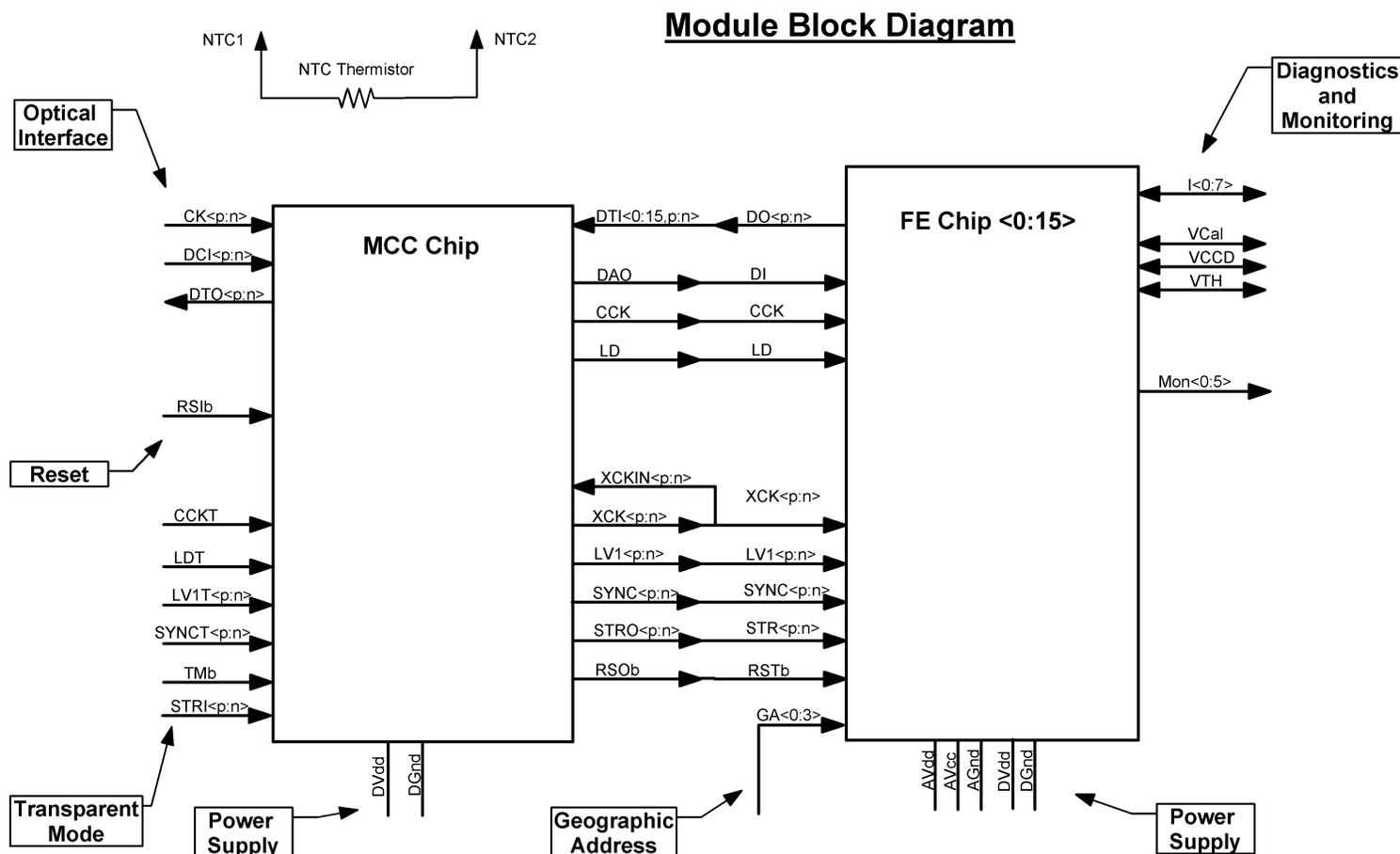
- How are cables shielded, the need for a commoning shield integrated with the pixel Global Support, and what is the shielding role of the beampipe.

Electronics components of pixel module:

- **Front-end chip:** Sixteen 7.4x11.0mm die per module, each containing 2880 pixels of size $50\mu \times 400\mu$, plus control of internal biasing and readout circuitry.
- **Module Controller chip:** assembles data from 16 FE chips into single event, and provides module level control functions and interface to opto-electronics.
- **Opto-electronics:** Driver for VCSELs used to transmit data stream to USA15 (VDC-p) and decoder for clock and command stream from USA15 (DORIC-p).
- **Power Distribution:** Six supplies and one control voltage provided from USA15.



Connections inside of Bare Module (MCC+FE+Sensor only):



- Interface to outside uses serial in, serial out, and 40 MHz clock.
- Only slow control uses CMOS signals. All critical connections use LVDS protocol.
- No analog signals are required between chips. FE chips have internal reference and 8-bit DACs to adjust front-end bias currents and calibration charge.

Power Supply and Miscellaneous Connections

Supplies required at module level (supplied by pigtail):

- One HV supply to bias sensor.
- Two Analog LV supplies for FE chips.
- One Digital LV supply for FE chips and MCC chip.

Supplies required at half-stave/sector level (opto-board):

- One Digital LV supply for VDC and DORIC.
- One Analog LV supply for PIN diode bias. Very low current.
- One digital control voltage (V_{ISET}) to adjust the VCSEL bias.

Additional DC signals in module interface:

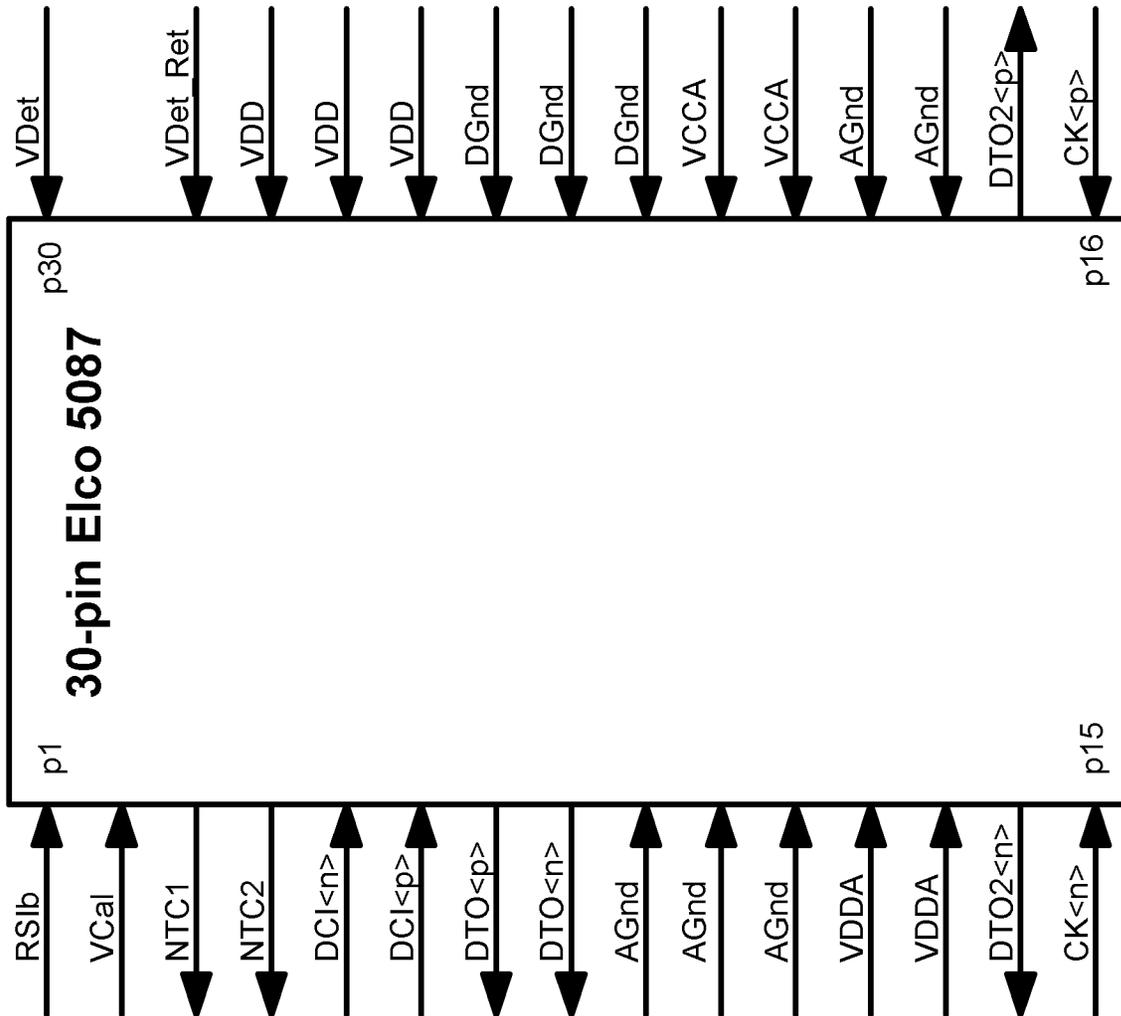
- **Reset** is an (optional ?) slow interface to RSI pin on MCC, to allow performing system reset from off-detector if necessary. Propose to implement this at half-stave/sector level for now, as it is a “safety net”. It is active-low DGND-referenced CMOS signal, and should be filtered to avoid any noise causing spurious resets.
- **NTC1** and **NTC2** are connected to a precision (1%) 10K Ω NTC thermistor used to monitor the module temperature (0603 part attached to Flex near module center). These signals are sent out at the module level, and are sampled by the I-box and digitized by the DCS system, both on-detector.

Sense Wires for High-Current Supplies:

- For power supply lines which carry current, there will be significant voltage drops, typically about 2-3V round-trip in our proposed cable plant.
- Ideally, we would like to know/regulate the absolute voltage on a given module to something like +/- 100mV during long-term operation. This particular specification requires further study, and is related to the detailed design, operation, and calibration of the FE electronics.
- For the proposed current-sensing supply control, this requires knowing the cable resistance to about +/-5%. The temperature coefficient for Copper resistance is 0.42%/C. Assuming no other uncertainties, this requires knowing the cable temperature to about +/-10 degrees, particularly in the high-resistance regions of the power cables.
- In addition, we have typically five connectors in the power conductors (one at each patch-panel), whose contact resistance should be negligible, but can evolve with time or fault conditions.
- Preferred solution would be to run individual sense wires to commoning point on module (basically, the pigtail connection). One side of NTC sensor could be connected to this same point, and hence could serve as a ground reference (assuming NTC signals routed to USA15). This scheme requires the addition of one wire per supply voltage. This wire can be small, imposing very little burden in the outer cables, e.g., 30 AWG (250 μ , 35 Ω /100m) or 32 AWG (200 μ , 55 Ω /100m).

Conductor Count and Pinout for Flex/Pigtail Connector:

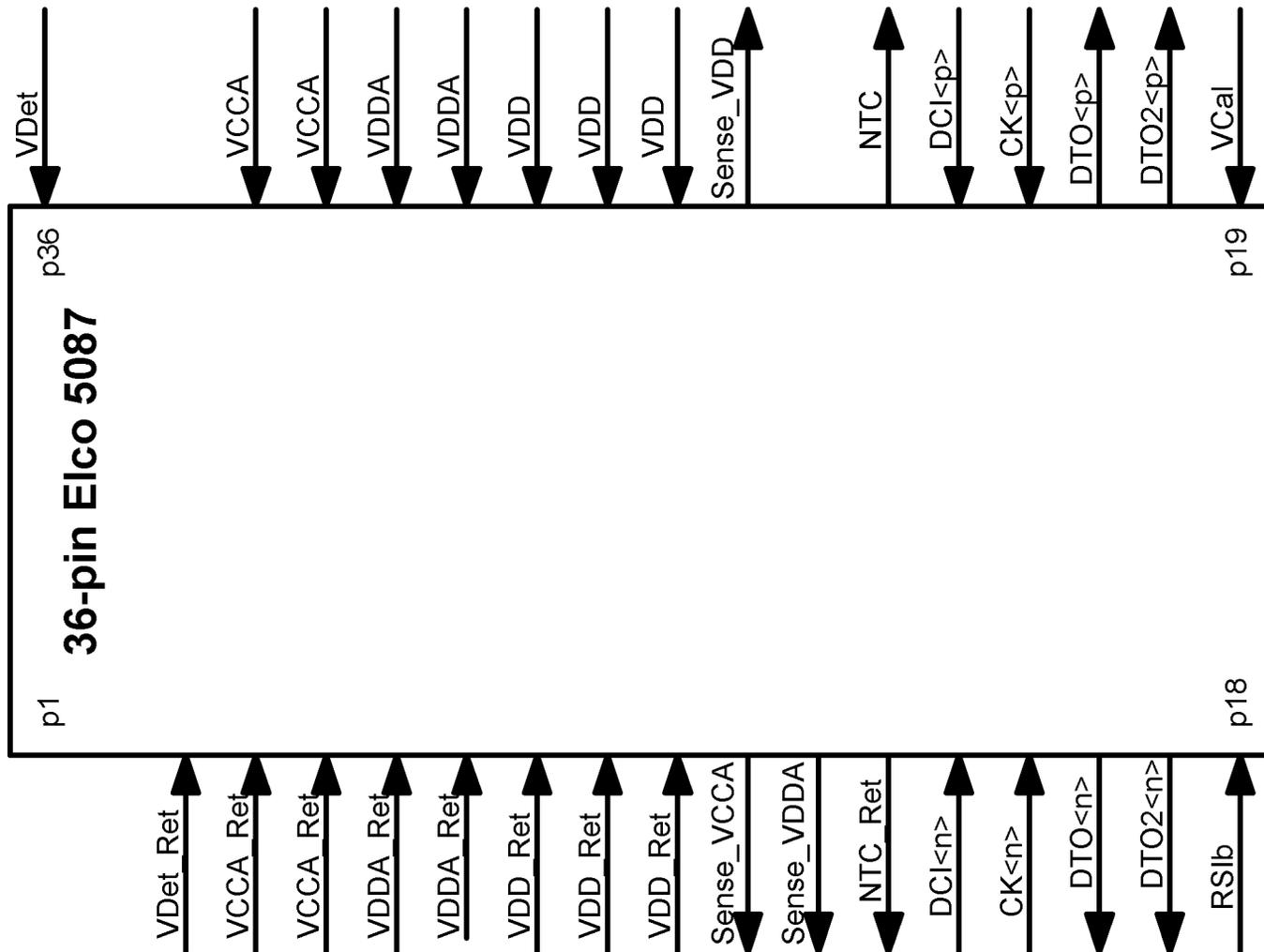
- This covers both the Pigtail and the Test Connector (common pinout)
- Present Flex 2.x design is a first pass, based on 30-pin Elco 5087 connector:



- These pin assignments grew out of the layout of the Flex2 hybrid.
- There is not much room around the VDet connection for 700V stand-off.
- These assignments mix high speed signals and power supplies, making the pigtail layout awkward.

Improved design (Flex 3.x ?) would look like the following:

- Organize conductors to provide optimal layout of Pigtail, separating AC and DC connections, and pairing connections on opposite sides of double-sided cable. Also leaves more space around the VDet connection.
- Include sense connections for high current supplies (VDD, VDDA, VCCA):



Current and Voltage Requirements for DMILL Chips

Analog Supplies:

- Assume a nominal operating voltage of 1.5/3.0V for VCCA and VDDA, with a worst case operating voltage of 1.75/3.5V. Assume for analog supplies that bias current is kept fixed, so increase of voltage causes linear power increase.
- **VCCA supply:** provides bias current for input transistor of preamp. Presently, FE-B uses about 5.5 μ A, and FE-C uses 10 μ A per pixel. Assume a worst case value of 15 μ A per pixel. Below, provide numbers for both 400 μ (and 300 μ) pixels, assuming 2880 and 3840 pixels per chip.
 - Total: 10 μ A/pixel at 1.5V, gives 29mA (38mA) or 43mW (58mW) typical.
 - Total: 15 μ A/pixel at 1.75V, gives 43mA (58mA) or 75mW (101mW) worst case.
- **VDDA supply:** provides bias current for preamp (load and source follower) and discriminator. Also supplies other circuitry, but assume this is negligible here. Presently, FE-B and FE-C use about 1.5 μ A, 1.5 μ A, and 5 μ A respectively for these purposes, for a total of 8 μ A per pixel. The worst case is assumed to be 12 μ A per pixel.
 - Total: 8 μ A/pixel at 3.0V, gives 23mA (31mA) or 69mW (92mW) typical.
 - Total: 12 μ A/pixel at 3.5V, gives 35mA (46mA) or 121mW (161mW) worst case.

Digital Supplies:

- Assume a nominal operating voltage of 3.0V for VDD, with a worst case operating voltage of 4.0V. For digital currents in CMOS chips, the scaling with supply voltage is more complex. Charging parasitic capacitances gives a quadratic dependence, whereas pull-up/pull-down resistors and overlap currents give a linear dependence. For FE-B and MCC, the current increase from 3V to 4V VDD is roughly a factor 1.6 (quadratic would give 1.8). An increase from 3V to 3.5V increases the current by about 1.25.
- **VDD supply:** Current for FE-B is about 18 mA at 3.0V. Add some additional current for sense amps in FE-D, plus some contingency to arrive at 25mA (35mA). Below, provide numbers for both 400 μ (and 300 μ) pixels, assuming 2880 and 3840 pixels per chip. Assume that the total digital current scales with the number of pixels on the FE chip. Present MCC is about 75mA at 3V, so add some contingency for new circuitry and arrive at 100mA.
- Total FE: 25mA (35mA) at 3.0V, gives 75mW (105mW) typical.
- Total FE: 40mA (55mA) at 4.0V, gives 160mW (220mW) worst case.
- Total MCC: 100mA at 3.0V, gives 300mW typical.
- Total MCC: 160mA at 4.0V, gives 640mW worst case.

Detector Bias Supplies:

- Assume the highest operating voltage will be 600V for the sensor bias. Our first sensors irradiated to 10^{15} fluences drew $60\mu\text{A}$ for a single chip at -7C and 600V, corresponding to 1mA per module. Long-term annealing should reduce this value in the experiment, however we assume this is nominal. We take a factor 2 worse for the worst case.
- **VDET supply:**
- Total : 1mA at 600V, gives 600mW typical.
- Total : 2mA at 600V, gives 1200mW worst case.

Optolink Supplies:

- There are two chips needed to support the optolink. Both use VVDC as a power supply. For the DORIC, we reduce the values determined from the SCT prototype chips since we will not use two outputs and we will reduce the current drive of the outputs since our loads are much smaller. Based on discussions with Dave White, 25mA seems a good estimate for the DORIC current in this case. For the VDC, the current consumption is dominated by the VCSEL drive current, which is nominally 10mA, and is 20mA worst case. For the B-layer, we assume we always operate both VCSELs. For the supply voltage, we assume the link will always operate at the “worst case” voltage of 4.0V.
- There is a separate bias supply for the epitaxial PIN diode used to receive the clock and control information. Irradiation studies suggest that bias voltages of up to 10 volts are required to get fast signals and good sensitivity after irradiation to full pixel fluences.
- **VVDC supply:**
 - Total : 25mA (DORIC) + 15mA (25mA B-layer) (VDC) at 4.0V, or 200mW typical.
 - Total : 40mA (DORIC) + 30mA (50mA B-layer) (VDC) at 4.0V, or 360mW worst case.
- **VPIN supply:**
 - Total : 10 μ A at 10V worst case.

Optolink Control Voltages:

- This control voltage determines the bias current for the VCSEL. It is provided by an additional low-current power supply channel. In the existing VDC chip, a given voltage determines the current value, and the load corresponds to a 1K resistor, or 5mA for the largest control voltage of 5V. This can be driven by a commercial DAC.
- We have tentatively agreed that even for the case of a B-layer link, where two VCSELs would be used for greater bandwidth, both would be controlled by a common VASET supply.
- **VASET supply:**
- Total : 5mA at 4.0V per VDC, gives 40mW worst case.

Summary of module current and power budget:

Voltage	Nominal Current	Nominal Voltage	Nominal Power	Worst Current	Worst Voltage	Worst Power	Supply Voltage	Supply Current
VCCA	460mA	1.5V	690mW	690mA	1.75V	1210mW	5V	1A
VCCA (B-layer)	610mA	1.5V	920mW	920mA	1.75V	1610mW	5V	1A
VDDA	370mA	3.0V	1110mW	550mA	3.5V	1940mW	7V	1A
VDDA (B-layer)	490mA	3.0V	1470mW	740mA	3.5V	2580mW	7V	1A
VDD	500mA	3.0V	1500mW	800mA	4.0V	3200mW	7V	1A
VDD (B-layer)	660mA	3.0V	1980mW	1040mA	4.0V	4160mW	7V	1A
VDET	1mA	600V	600mW	2mA	600V	1200mW	700V	2mA
Total			3900mW			7550mW		
Total (B-layer)			4970mW			9550mW		

Summary of opto-board budget (assuming 6 links):

Voltage	Nominal Current	Nominal Voltage	Nominal Power	Worst Current	Worst Voltage	Worst Power	Supply Voltage	Supply Current
VVDC	240mA	3.0V	720mW	420mA	4.0V	1680mW	7V	0.1A
VVDC (B-layer)	300mA	3.0V	900mW	540mA	4.0V	2160mW	7V	0.1A
VPIN		5V		10 μ A	10V		12V	5mA
VISET		1V		10mA	4V	40mW	7V	10mA

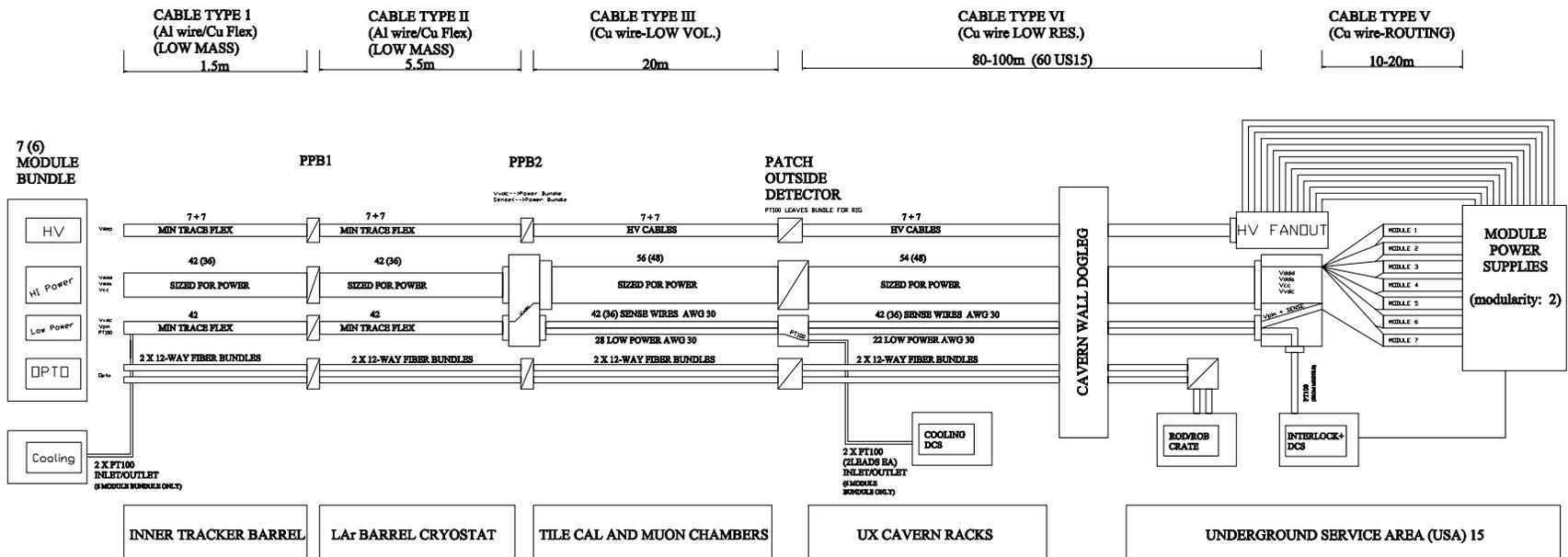
- Note these totals do not include power dissipation in the voltage drops along the power cables. The new allocation is 50mV for the Flex, up to 400mV for the pigtail along the stave, and an additional 150mV to reach PP0, or a total drop of 600mV for the Flex plus pigtail. In this case, the module power consumption increases by about 1.2W (1.6W) for the worst cases.
- The maximum DC power to be provided by the supplies for a single module is about 18W. The maximum voltage from the supply has been defined to allow up to 2V of drop on the cable system (1.0V supply and 1.0V return).

Comments on Requirements for 0.25 μ Designs

- Front-end design is still evolving, so not much understanding of what the front-end currents will need to be. However, it appears quite likely there will be only a single analog supply (VCCA will be dropped).
- Goal is to keep within the present current budget. This would imply about half the power for the modules (2V instead of 3.5V or 4V), but the same power dissipation and sizing for the services. For the digital parts of the designs, this should be a conservative assumption, since digital consumption is driven by parasitic capacitances, which are generally reduced in a smaller feature size design. For the analog parts, it is still too early to tell, but previous worst-case assumption was already fairly conservative, so no surprises would be expected.
- Optimistically, can hope for reductions in worst-case currents, but this cannot be proven until we have a working FE-I chip...
- Could end up with a mixed-technology system. This might mean DMILL for the DORIC and VDC (no problems with power distribution, since VVDC is already separate). It could even mean a DMILL MCC, in which case the dropped VCCA wires could be used for VDD_MCC. None of these options should present significant technical problems.
- At this time, we should avoid making any design decisions which would rule out any combination of DMILL and 0.25 μ implementations for any of the ICs. Once we have really proven the 0.25 μ solution, this could be relaxed.

Original Cable Layout and Voltage Drops:

- Initial design assumed maximum $\Delta V = 2.0V$ (round-trip).
- There are five types of cables, plus a local pigtail onto the module from the end of stave or sector, plus the Flex hybrid itself.
- The Flex hybrid budget was $\Delta V = 0.05V$, and the pigtail budget was $\Delta V = 0.20V$.
- The type I and II regions (out to PP2) are proposed to be round cables for the large currents, and flat cables for the others.
- The remaining two types of cables go through PP3 and on to USA15, with a nominal drop on each of about $\Delta V = 0.4V$. A multiplicity of 2 modules/channel is assumed at the power supply end:



Updated Cable Components and Voltage Drops

Pigtail (length up to 40cm for disk, 120cm for barrel):

- Attaches to the Flex hybrid using wirebonds (barrel concept) or solder pads (disk concept). With new services concept, the pigtail goes from the Flex Hybrid to PP0, where PP0 is mounted on the Services Support at either end of the Global Support for the pixel detector. This makes the length of the pigtail in the barrel (worst case is B-layer) up to about 1.2 meter long.
- Present Flex 2 design makes optimal layout difficult. Ideally, would use broad-side coupled transmission lines for all LVDS signal pairs and supply/return pairs. This cable must be designed for minimum EMI, since it contains substantial 40MHz clocking. Low mass design within budget of $\Delta V=600\text{mV}$ (50mV for Flex, 400mV in stave region and 150mV from stave to PP0) for LV supplies will be challenging.

PP0 (located at R of about 10cm):

- Simple patch-panel to map half-stave or sector cable bundle into 6-7 pigtail connectors (presently 30-pin Elco 5087). Also includes opto-daughter card to transform optical versions of clock/control and data into LVDS versions. Concept is that this card supports 6-7 complete module opto-links (most likely to be transformed into a single wider opto-link).
- Do not plan to place any passive components (decoupling or transient protection) on this panel at this time, but needs further analysis.

Type 1 cable (length now about 3m, at R of about 10cm):

- Contains low mass Flex connections for signals (Reset, NTC, VISET) and low current supplies (VPIN, VDET). Ideally, this cable would be directly integrated (using rigid-flex technology) with PP0 and PP1 terminations.
- Contains AI round cable connections for power supplies with real current (VCCA, VDDA, VDD, VVDC). Assume this is unshielded twisted pair, but needs further analysis (twisting roughly doubles cable cross-section). Termination of these cables remains a technical issue. If crimped to pins, there are lifetime issues, if soldered, there are metallurgy issues. ΔV budget is 500mV to minimize material.
- Note in new concept with opto-daughter card serving a half-stave or sector, the Reset, VISET, VPIN, and VVDC traces are only present once per cable, with corresponding loss of redundancy for opto-links (can lose 6-7 modules).

PP1 (located at R of about 15cm):

- Basically exists to allow services disconnect at end of ID, and to increase conductor sizes for run out to PP2.
- In previous design, this could have contained additional filtering/decoupling capacitors and transient protection (not clear that space for this existed). New location could have fewer space and material constraints, but has more severe radiation dose constraints.
- Filtering could be additional 1206-size ceramic filters on all LV power lines.

- Transient protection is more complex issue. Largest concern is case where, due to changes in module operation, there is a significant change in current consumption on one or more of the supplies for the module (e.g. loss of XCK will dramatically change digital supply current). This can induce an appreciable transient before the power supplies can compensate.
- For DMILL electronics (supplies in range of 3V to 4V with snapback voltages of 8V), there exist commercial solutions. Chose AVX Transguard (ZnO varistor with operating voltage of 3.3V) as baseline part. In an 0805 package, it is rated for energy absorption of 0.3J. Some of these parts were irradiated at the PS to 50MRad in May, and they survived.
- For 0.25 μ electronics (supply voltage in range of 2V with worst case snapback voltage of 4V), protection is more difficult. Conventional transient protection devices (varistors, zeners, avalanche diodes) do not provide good clamping below 4V. There is a production from Semtech (“enhanced punch-through diode”) which has good I/V characteristics. This is a semiconductor device with novel geometry (although it is based largely on lightly or heavily doped p regions, so it may be radiation hard), as opposed to a ceramic device like the previous baseline. Parts are on order for evaluation.

Type 2 cable (length now about 3.5m, R from 20cm out):

- Very similar to Type 1 cable, with low mass Flex where possible and twisted pair Al cable where currents are large. ΔV budget is 150mV since mass is not critical.

PP2 (R about 2.5m):

- This is the transition to more conventional connectors and cables.
- If placing of passive components discussed above at PP1 is too difficult, they would move out here.

Type 3 cable (length of about 25m):

- These are conventional cables, assumed to be unshielded and twisted pair. Present budget is $\Delta V=500\text{mV}$ to allow small sizing to pass through finger region.

PP3 (R about 3m):

- First relatively large region, located in racks just outside of muon system.
- One concept proposed by SCT is to use common-mode chokes on all power supplies. This has virtue of significantly reducing constraints on conventional cable design, and blocking most noise on supplies induced from outside of detector. Because of residual B field, chokes (parts from Pulse Engineering) need to be inside iron tubes. Second option is to use radiation-tolerant linear regulators, but they require remote voltage adjust and dissipate significant power.

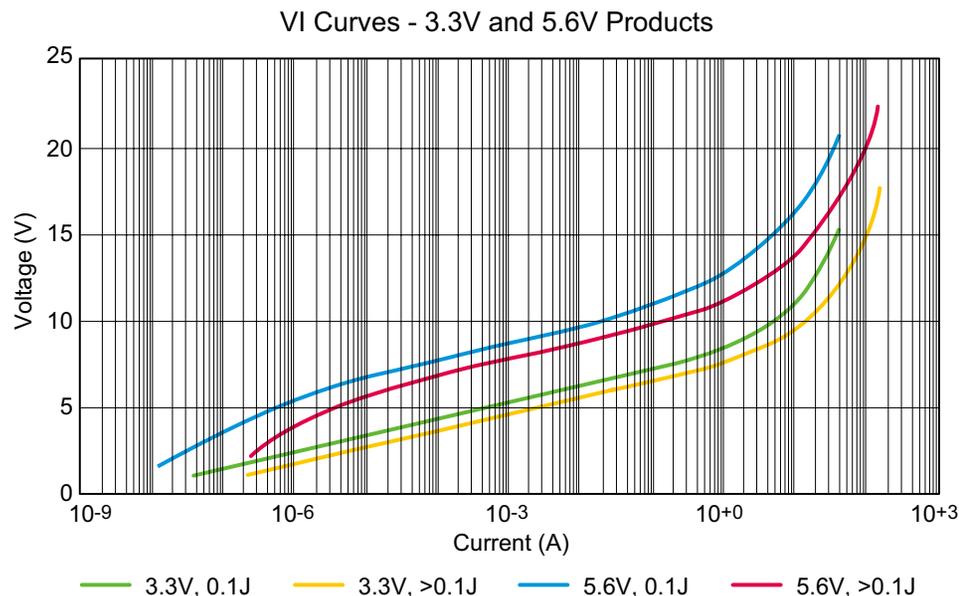
Type 4 (length to 100m) and Type 5 (length to 20m) cable:

- This is the long conventional cable run, where Copper costs play a large role. It is not clear at what level this is shielded (if at all), or whether it is twisted. It could be much shorter if supplies are divided between US15 and USA15.

More on Transient Protection

AVX Varistor transient protection:

- Devices of choice seem to be TransGuard product from AVX. These are varistors, ceramic semiconductors based on ZnO. They operate like a pair of back-back Zener diodes, but have a “distributed” junction to provide much better current and energy absorption than Zeners.
- They will switch on in less than 1 ns, but do not have a terribly steep I/V curve. The lowest voltage part is 3.3V. It has a “breakdown” voltage of 4-6V (voltage at which $I = 1\text{mA}$), and an equivalent R less than 1Ω at about 8V:

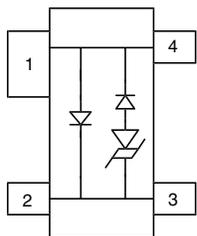


- Part of interest is 3.3V 0.3J 0805 component.

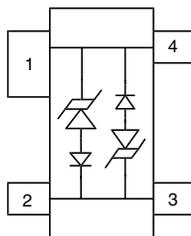
SemTech TVS Diode:

- Semiconductor part, based on “enhanced punch-through” diode. It uses a complex pnp structure in which avalanche behavior under reverse bias is suppressed and punch-through conduction is enhanced above threshold voltage.

Circuit Diagrams

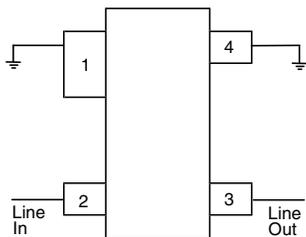


SLVG2.8



SLVE2.8

Connection Diagrams



Common Mode Protection
(SLVE2.8 or SLVG2.8)

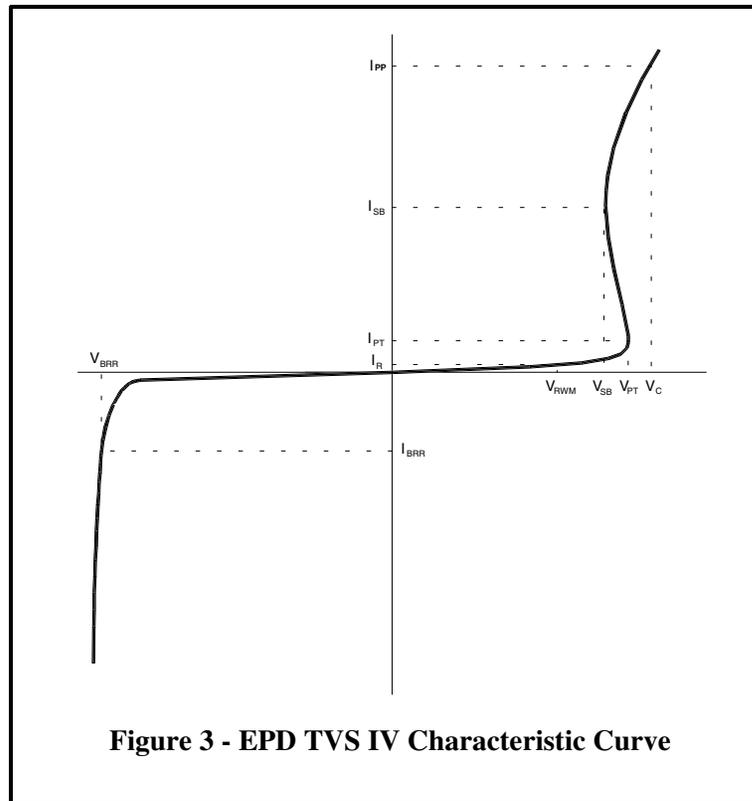


Figure 3 - EPD TVS IV Characteristic Curve

VStandOff
(VRWM) = 2.8V

Vpunchthrough
(VPT) = 3.0V

Vsnapback
(VSB) = 2.8V

VClamp
(VC)= 4.1V
for 1A current pulse

- Packaged as an SOT-143 package, about the same size as a 1210 capacitor.
- Have ordered significant quantity of the SLVE2.8 for evaluation purposes.

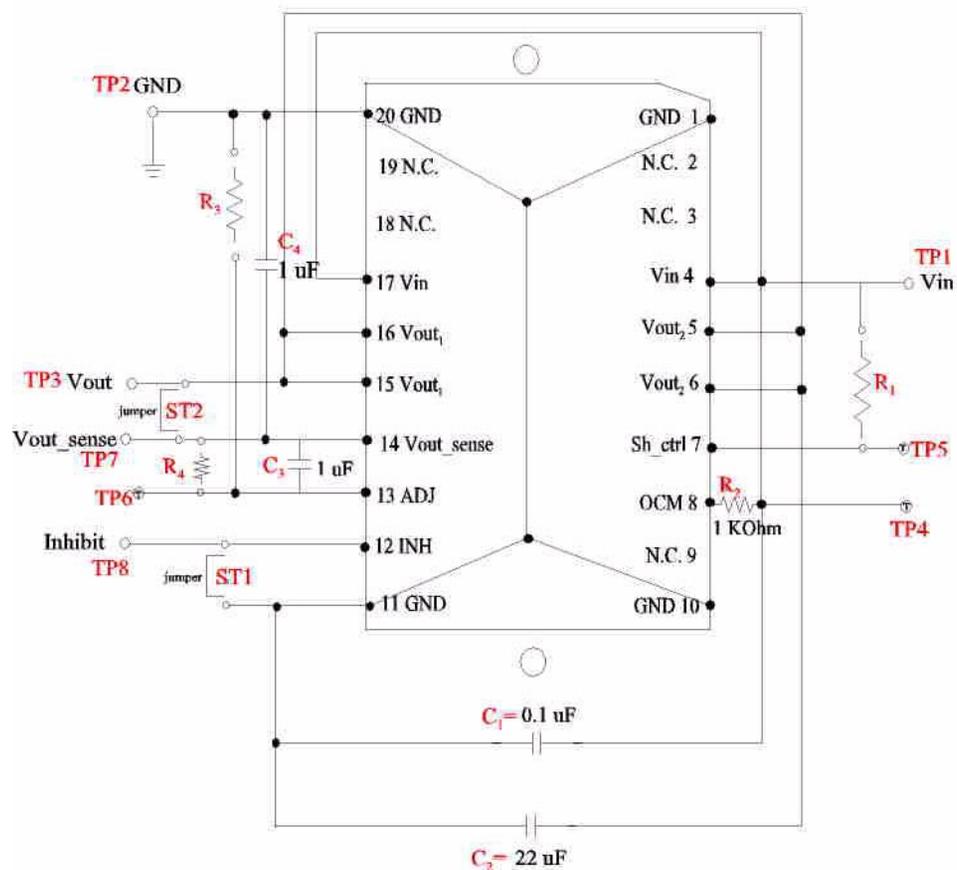
Possible use of Rad-Tol Regulators

- An improved power distribution system could be constructed if linear regulators could be used closer to the pixel modules (5-30m), instead of relying on passive components alone to filter noise and transients.
- CERN has jointly developed a Rad-Tol LDO (Low Drop Out) regulator in collaboration with ST Microelectronics (L4913).

Some of the specifications include:

- Radiation tolerance of 500KRad total dose and 2×10^{13} n/cm² neutron fluence. This is achieved by using a high-speed bipolar process from ST which is different from their standard regulator process (high-speed bipolar processes have thinner oxide layers and hence smaller low-dose rate effects).
- Low drop-out voltage of 0.5V for 1A operation (0.65V worst-case).
- Over-temperature, Over-voltage, and adjustable Over-current protection.
- Support of remote sensing (possible over 30m ?)
- Part is packaged in special PowerSO20 package.
- First evaluations show design meets specifications, with some minor design flaws which are now being fixed. Production is foreseen to begin late in 2001.
- Cost is modest (about \$25 each in quantity ?)

•Evaluation board is available:



- First irradiations show operation is OK up to 10MRad and $3 \times 10^{14} \pi/\text{cm}^2$.
- For pixels, the total current for a module is about 2A, and a 1V VDO would be needed for safety, so the three regulators/module would dissipate 2W. This makes implementation at PP2 very difficult, so PP3 is the natural location.
- Would need to implement remote voltage adjustment via DAC (?)

What is needed for a cable design:

Cables and patch-panels form complex electrical system

- Present design needs to be completed at the most detailed level. This includes pin assignments, exact part numbers for connectors and cables and inventory of all connections, prototyping of all termination concepts, evaluation of all components for reliability and radiation dose issues, etc...
- Ideally, would like to work on SPICE level simulations of cables (including Flex Hybrid), including crude model for AC current transients in operating module, local decoupling on Flex, and any additional passive components at PP0/1/2/3. Can SPICE parameters of cables be determined in lab or by calculation ?
- Will be validating some aspects of design at single module level, using prototype power cables, operating with power supply prototypes, over next few months.
- Next level of prototyping would need to involve half-stave or sector prototype with 3-6 modules operating together.
- Perhaps final level of prototyping would involve something like a complete bi-stave prototype with 26 modules operating together.
- These prototypes will come extremely late, due to lateness of electronics. There will be little (or no) time for iteration. The design must be conservative within the limited space, material, and financial envelopes...
- Major open question (and cost driver): what is maximum allowed ΔV in design ?

Grounding and Shielding Concept:

Grounding Philosophy:

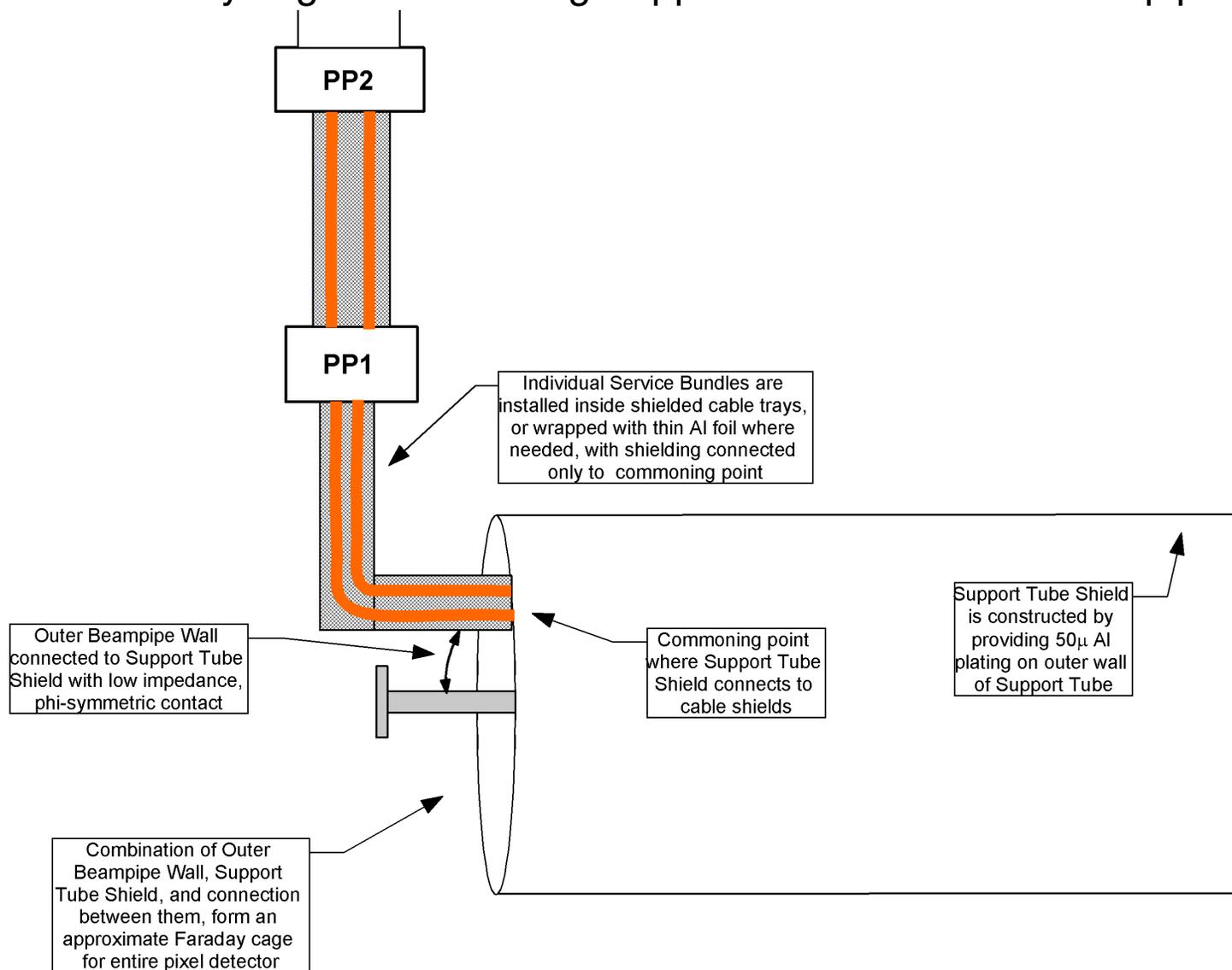
- All power supplies are assumed to have individually floating channels, where only safety (resistive) ground connections are made. All grounding/commoning takes place inside the detector volume. The connection between the pixel detector commoning point (see below) and the rest of ATLAS should be a controlled, single-point connection, not the result of many random connections.
- Initial reference point will be connection of various grounds on module. The present grounds are AGnd (VDDA return, VCCA return, and VDET return) and DGnd. Interconnections of these grounds can be individually controlled on Flex2 Hybrid. However, note that this hybrid does not have a ground plane, but only rather narrow ground traces, which do not even satisfy our ΔV requirements due to limited area available in a double-sided design.
- Second reference point would naturally be connection of relevant grounds on PP0 patch panel. Imagine that this would be connection of AGnd from all modules in a service bundle, and connection of DGnd from all modules in a service bundle. There could be the option of connecting AGnd and DGnd also at this level, although if true commoning point is PP1, this is not preferred. This raises the question of whether the pigtailed support separate grounds for each supply (as now conceived), or whether they implement only AGnd/DGnd planes, or even a single combined ground plane. Preferred solution is to keep them all separate.

- The original SCT concept is to have a shield at the outer radius which serves as the commoning point for all local grounds, and which would shunt the externally induced noise currents on these grounds around the sensitive signal paths inside the individual modules. This metal cylinder does not yet exist in the new pixel mechanical design, but is essential. Detailed calculations are needed for its thickness. It should be thick enough that there is a significant reduction in the noise current flow through the module signal paths (factor of 10 ?). This implies that relative impedance of the shunted current paths should be at least ten times lower than the impedance for noise currents to flow through the signal paths.
- Two possibilities exist for such a commoning point. One would be a conductive tube between PP0's on the two ends of the detector. This has the virtue of commoning close to the detector, and of attaching the shield directly to the Pixel Global Support. However, it is almost impossible to implement a real shield (continuous metal layer) in this region due to mechanical constraints, so only a shunt could be provided. It is also difficult to connect from the end of the Global Support down to the beampipe with the low-impedance, phi-symmetric connection needed (beampipe has large CTE compared to carbon supports).
- The alternative is to use the Support Tube used for installation of the pixel detector, and support of its services, as the shield. In this case, the outer surface would be metalized with something like 100 μ of Al. It is easier to connect down to the beam pipe because the end of the Support Tube is close to the beampipe flanges. The commoning point would then be PP1, just beyond the tube end.

- Expect that all service bundles (half-stave or sector level) are individually shielded with an overall foil wrap of maybe 50 μ of Aluminum, or enclosed in individual conductive (but isolated) Aluminum cable trays. These shields should be connected together at the commoning point, and should surround the cables as they run from PP1 outwards. The individual foil shields should not be in electrical contact as the cables find their way out from the commoning point, in order to avoid additional ground loops between the shields.
- The pigtailed, as well as the cables going inside from PP1 to PP0, should not require shielding from the point where they enter the Support Tube Shield until they connect to the individual modules, but this depends somewhat on whether a good low-EMI design is possible for the cables. Otherwise, it may be necessary to shield each cable from the noise produced by the other cables.
- The pixel volume would be further enclosed by the conductive sheet at the end of the support tube, that would be used to connect the beampipe and the Aluminum support tube shield together electrically.
- The above scheme only applies if the central portion of the outer wall of the beampipe is electrically isolated from the inner wall of the beampipe. If this is not the case, then we probably only want to connect the Support Tube Shield to one end of the beampipe to avoid creating loops for the beam image currents to flow around. In this case, the shielding from the beam-induced noise would be reduced, and we would not have a real Faraday cage.

Summary of the Overall Grounding/Shielding Scheme

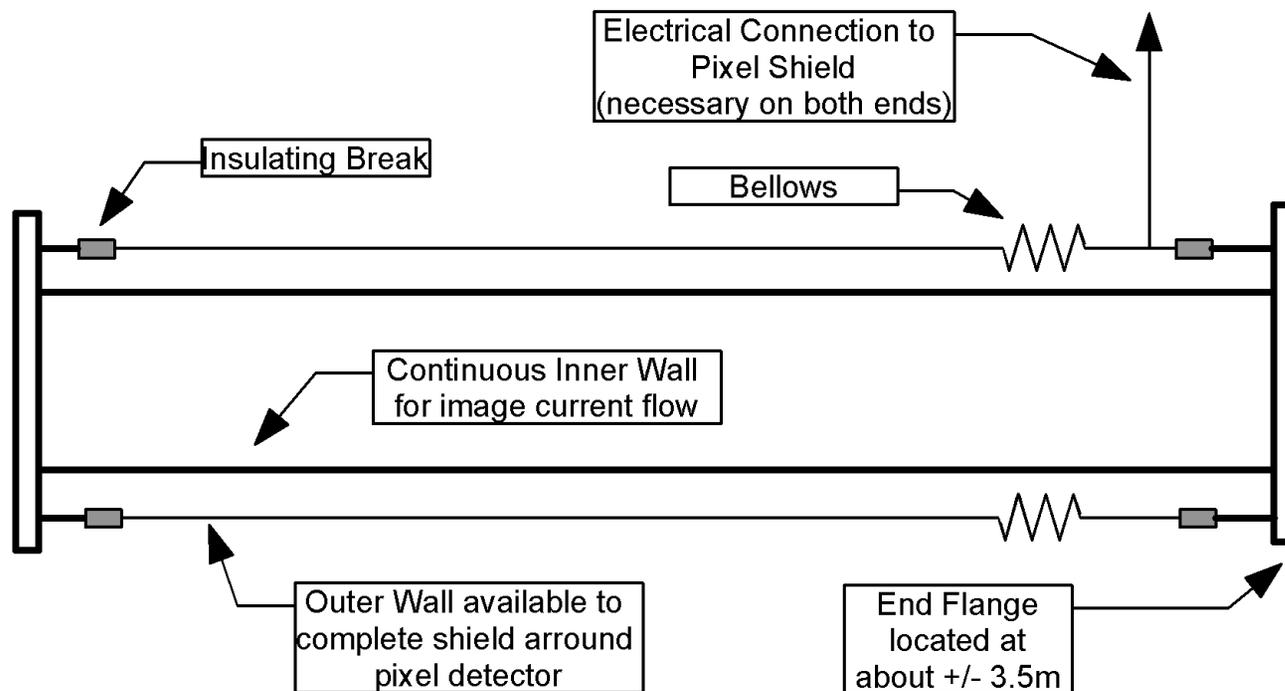
- Form Faraday cage from 7m long Support Tube and outer beampipe wall:



Beampipe Issues

Present baseline is double-wall beampipe:

- This design offers many advantages from grounding/shielding point of view. The dangerous beam image currents flow on the inner wall, and the isolated outer wall is available to play a significant role in defining a shielding cage for pixels.
- Beampipe concept, with both inner and outer walls of 800μ thick Be:

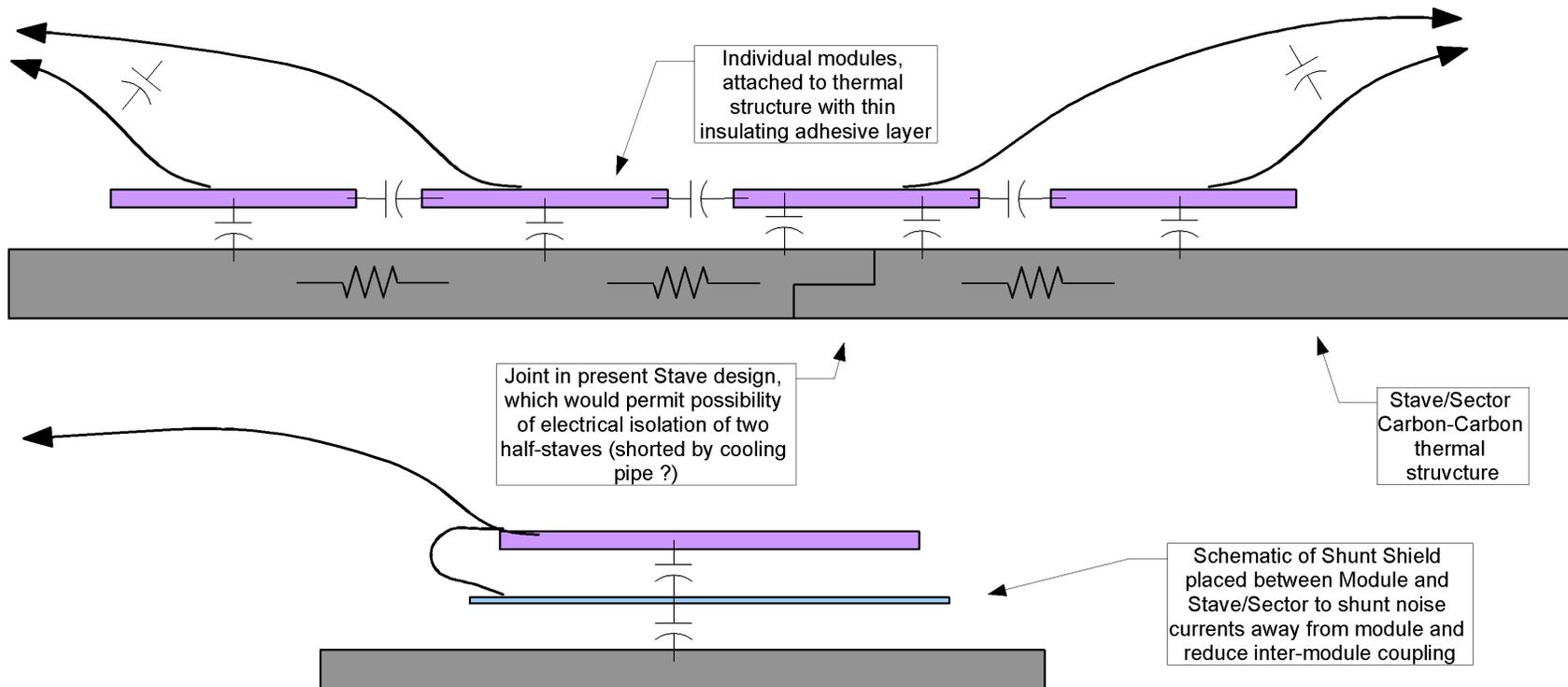


- Recent comments from beampipe experts suggest that electrical isolation of central portion of outer beampipe by insulating breaks may be technically very difficult, and must be strongly justified.

Module attachment issues/comments:

- Local mechanical supports are all electrically fairly conductive (C-C material). The modules are assumed to be electrically (DC) isolated from these structures, but they are mechanically intimately coupled to them. The exact scheme depends on whether or not a back-side AGnd connection to the module is needed. If it is not needed, then the chip back-side is coupled via about 100 μ of adhesive ($\epsilon=4$, 100 μ thick gives 35pF/cm², or 500pF/module). This will connect all module grounds together via a moderate impedance in the frequency range of greatest relevance (impedance of ideal capacitor of 500pF is 100 Ω at 3.5MHz).

Electrical Model of Module Coupling in Stave/Sector



- Shunt Shield between module and thermal structure offers the possibility of increased isolation between modules on common thermal structures. However, it certainly complicates the module attachment and degrades the thermal conductivity between module and cooling pipe.

Comments on back-side electrical contact with module:

- The substrate of an FE chip is made out of low-resistivity (highly doped) p+ material. In the case of the DMILL SOI process, there is a 1.2μ epitaxially grown layer of silicon which is on top of a buried oxide layer, and so the silicon in which the transistor wells are formed is only capacitively coupled to the wafer substrate. In the case of a deep-submicron process, there is a 2μ epitaxially grown layer on top of a very highly doped p+ substrate (resistivity $< 0.01\Omega\text{-cm}$), and there is a direct coupling to the wafer substrate.
- In either case, any digital noise currents flowing in the substrate could change the potential of the wells of analog transistors, and therefore have the potential to affect the noise performance of the FE chip. If the back of the low-resistivity substrate is instead uniformly connected to a high quality ground plane, then these noise currents will tend to follow the path of lowest impedance down through the substrate to the ground, and not couple into nearby sensitive analog circuits. Conservative practice would always connect the back-side to ground.
- This has been tested in earlier generations of FE IC's (FE-B and FE-D1b) by back-side grinding (to remove native oxides), and plating with Ni and Au. The die

were then epoxied to the standard single-chip support card, which contains a large analog ground plane under the entire FE die region. In none of these cases did we detect a significant change in noise performance for the two cases (with and without low-impedance back-side contact). For the FE-B case, this was tested on bump-bonded assemblies from both IZM and AMS, both single chips and modules. For the FE-D1b case, this was only tested with bare die.

- Nevertheless, particularly with the FE-I design, it is possible that once we arrive at final FE designs, there will be a large difference between the noise performance with and without the good back-side contact.
- It is very difficult to implement an elegant back-side contact scheme for ATLAS pixel modules. A major issue with any ground plane is that a large metal plate has a much larger CTE than the carbon structure. This means that the large metal pad for contacting the back-side must be divided into small regions. Furthermore, the present 2-sided Flex design does not contain a true ground plane, making it more imperative that the support interface could fill this need.
- For the barrel modules, there is only a modest space available on the module sides, in between the FE chips, because the production bonding pattern only allows bonding the central 30 pads. In this case, one could imagine a Flex with tabs extending outward between FE die, and then attaching those tabs to the module back-side with conductive epoxy. For the disk case, the clearances on the module sides are very minimal, forcing consideration of the module top and bottom for the interconnect between the two sides of the module.

Additional issues/comments:

- It is assumed that the local mechanical supports will in general be electrically (DC) isolated from the relevant support shells (barrel) and support rings (disks). There should be a decent quality single-point ground connection between all elements of the mechanical support structure, to provide a safety ground and keep the mechanical structure at a well-defined potential without ground loops. This does not have to be a low-impedance connection. This safety ground should be single-point connected to global common.
- For the barrel case, would prefer the connection to be on one end only to prevent individual staves shunting the outer shield. If it is possible to electrically isolate the two halves of a stave via the joint used in the stave fabrication, that would be very desirable. The mechanical implications of this are not clear. For disk case, all individual sectors are isolated from each other, and from the overall mechanical support, by a small PEEK insert.
- Present cooling concept involves a bi-stave (both cooling connections at the same end of a pair of staves) and a double sector for new 8-sector disks. The bistave case has the pair of pipes close together (few cm), but the disk case has the pipes about 90 degrees apart in ϕ . This makes commoning of the relevant pipes topologically simple, but for the disk, only one end should be commoned.
- Finally, most of the conductors in the above discussion are Aluminum, and there are many issues involved in making reliable, low-resistance connections to these conductors (their resistance must remain low over a multi-year lifetime).

Summary of Action Items

- Critical driver for cable cost is maximum allowed ΔV and total cable length. If ΔV can be increased from 2V up to 3-4V, very substantial savings could be found. If half of supplies can be moved to US15, cable runs can be shortened significantly. Should re-consider implementing supply sensing up to module connection and possibly regulation at PP3. Requires better understanding of grounding scheme, transient behavior of supplies/electronics, plus transient protection prototyping.
- Need to perform electrical characterization of carbon-carbon in Stave/Sector prototypes and carry out detailed electrical modeling of fully populated structures.
- Need to make sure that evolving beampipe design provides best Faraday cage possible within other constraints, and includes proper electrical contact points.
- Need to include appropriate metalization of new Support Tube in design to be sure we provide a low-impedance shielding and shunting path for noise currents.
- Need to begin multi-module system tests as soon as possible to investigate whether shunt-shields between modules and support structure are needed. Also need to further explore how module attachment would be modified if a shunt shield is needed, a back-side chip connection is needed, or both are needed.
- Need to prototype different grounding schemes for pigtailed and PP0, with full length power cables. Of particular concern is the case of barrel modules whose services run out in opposite directions from the detector, where the loop area of the services bundles is very large. The performance may depend critically on whether or not electrical isolation can be achieved between the two stave halves.