# VIII. Digitization of Pulse Height and Time – Analog to Digital Conversion

For data storage and subsequent analysis the analog signal at the shaper output must be digitized.

Important parameters for ADCs used in detector systems:

1. Resolution
   The "granularity" of the digitized output

2. Differential Non-Linearity
   How uniform are the digitization increments?

3. Integral Non-Linearity
   Is the digital output proportional to the analog input?

4. Conversion Time
   How much time is required to convert an analog signal to a digital output?

5. Count-Rate Performance
   How quickly can a new conversion commence after completion of a prior one without introducing deleterious artifacts?

6. Stability
   Do the conversion parameters change with time?

Instrumentation ADCs used in industrial data acquisition and control systems share most of these requirements. However, detector systems place greater emphasis on differential non-linearity and count-rate performance. The latter is important, as detector signals often occur randomly, in contrast to measurement systems where signals are sampled at regular intervals.

*Introduction to Radiation Detectors and Electronics, 16-Mar-99*
*VIII. Digitization of Pulse Height and Time*
*Helmuth Spieler*
*LBNL*

1. Resolution

Digitization incurs approximation, as a continuous signal distribution is transformed into a discrete set of values. To reduce the additional errors (noise) introduced by digitization, the discrete digital steps must correspond to a sufficiently small analog increment.
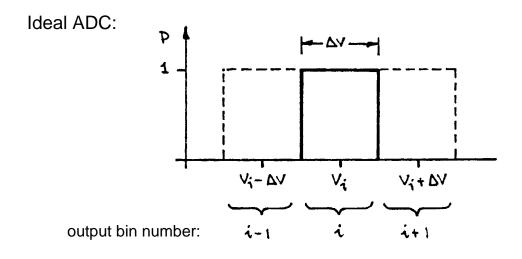
Simplistic assumption:

Resolution is defined by the number of output bits, e.g.

$$13 \text{ bits} \quad \rightarrow \quad \frac{\Delta V}{V} = \frac{1}{8192} = 1.2 \cdot 10^{-4}$$

True Measure: Channel Profile

Plot probability vs. pulse amplitude that a pulse height corresponding to a specific output bin is actually converted to that address.
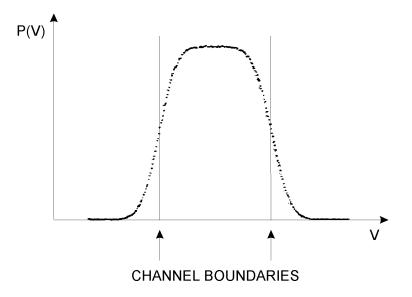
Ideal ADC:



output bin number:

Measurement accuracy:

- If all counts of a peak fall in one bin, the resolution is $\Delta V$.

- If the counts are distributed over several (>4 or 5) bins, peak fitting can yield a resolution of $10^{-1} - 10^{-2}\ \Delta V$, *if the distribution is known and reproducible* (not necessarily a valid assumption for an ADC).
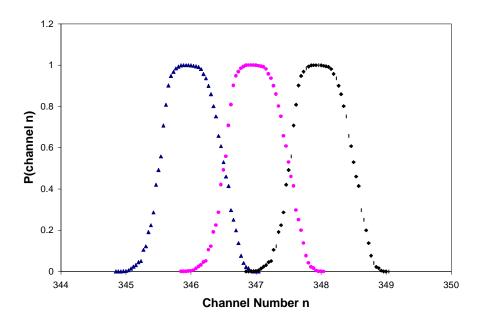
In reality, the channel profile is not rectangular as sketched above.

Electronic noise in the threshold discrimination process that determines the channel boundaries "smears" the transition from one bin to the next.
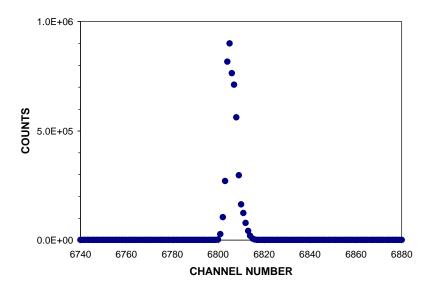
Measured channel profile (13 bit ADC)



CHANNEL BOUNDARIES

The profiles of adjacent channels overlap

Channel profile can be checked quickly by applying the output of a precision pulser to the ADC.
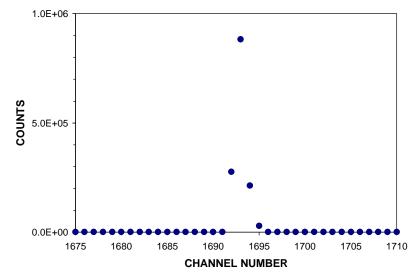
If the pulser output has very low noise, i.e. the amplitude jitter is much smaller than the voltage increment corresponding to one ADC channel or bin, all pulses will be converted to a single channel, with only a small fraction appearing in the neighbor channels.

Example of an ADC whose digital resolution is greater than its analog resolution:

8192 ch conversion range (13 bits)



2048 ch conversion range (11 bits)



2K range provides maximum resolution – higher ranges superfluous.

## 2. Differential Non-Linearity

Differential non-linearity is a measure of the inequality of channel profiles over the range of the ADC.

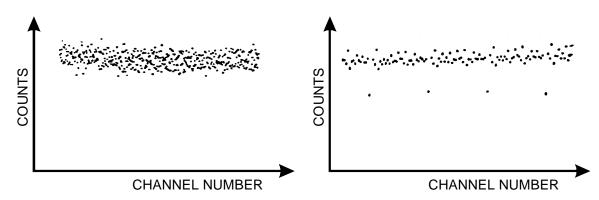Depending on the nature of the distribution, either a peak or an rms specification may be appropriate.

$$DNL = \max\left\{\frac{\Delta V(i)}{\langle \Delta V \rangle} - 1\right\}$$

or

$$DNL = \text{r.m.s.}\left\{\frac{\Delta V(i)}{\langle \Delta V \rangle} - 1\right\}$$

where $\langle \Delta V \rangle$ is the average channel width and $\Delta V(i)$ is the width of an individual channel.

Differential non-linearity of $< \pm1\%$ max. is typical, but state-of-the-art ADCs can achieve $10^{-3}$ rms, i.e. the variation is comparable to the statistical fluctuation for $10^6$ random counts.

Note:   Instrumentation ADCs are often specified with an accuracy of $\pm0.5$ LSB (least significant bit), so the differential non-linearity may be 50% or more.

Typical differential non-linearity patterns ("white" input spectrum).
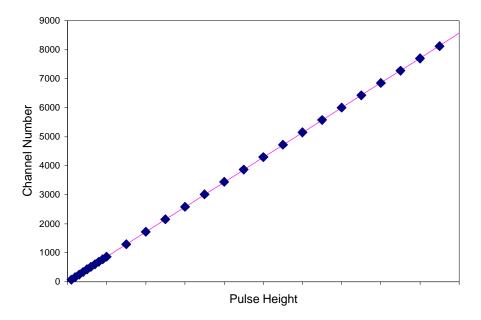


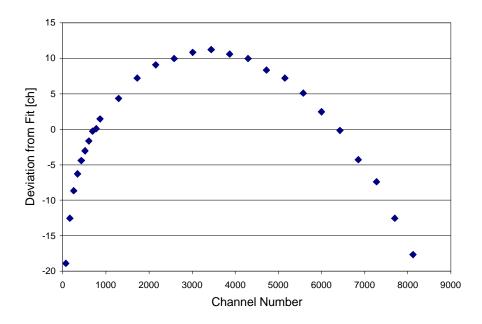An ideal ADC would show an equal number of counts in each bin.

The spectrum to the left shows a random pattern, but note the multiple periodicities visible in the right hand spectrum.

## 3. Integral Non-Linearity

Integral non-linearity measures the deviation from proportionality of the measured amplitude to the input signal level.



The dots are measured values and the line is a fit to the data.

This plot is not very useful if the deviations from linearity are small.

Plotting the deviations of the measured points from the fit yields:

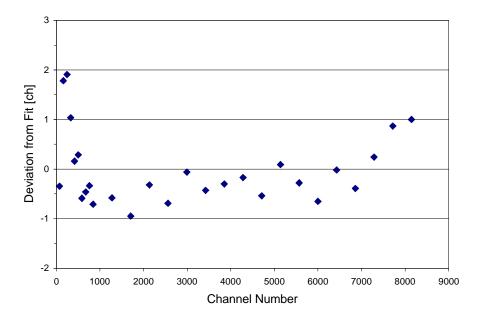The linearity of an ADC can depend on the input pulse shape and duration, due to bandwidth limitations in the circuitry.

The differential non-linearity shown above was measured with a 400 ns wide input pulse.

Increasing the pulse width to 3 $\mu$s improved the result significantly:

## 4. Conversion Time

During the acquisition of a signal the system cannot accept a subsequent signal ("dead time")

Dead Time =

signal acquisition time $\rightarrow$ time-to-peak + const.

+ conversion time $\rightarrow$ can depend on pulse height

+ readout time to memory $\rightarrow$ depends on speed of data transmission and buffer memory access - can be large in computer-based systems

Dead time affects measurements of yields or reaction cross-sections. Unless the event rate << 1/(dead time), it is necessary to measure the dead time, e.g. with a reference pulser fed simultaneously into the spectrum.

The total number of reference pulses issued during the measurement is determiend by a scaler and compared with the number of pulses recorded in the spectrum.

Does a pulse-height dependent dead time mean that the correction is a function of pulse height?

Usually not. If events in different part of the spectrum are not correlated in time, i.e. random, they are all subject to the same average dead time (although this average will depend on the spectral distribution).

- Caution with correlated events!
  Example: Decay chains, where lifetime is < dead time. The daughter decay will be lost systematically.

## 5. Count Rate Effects

Problems are usually due to internal baseline shifts with event rate or undershoots following a pulse.
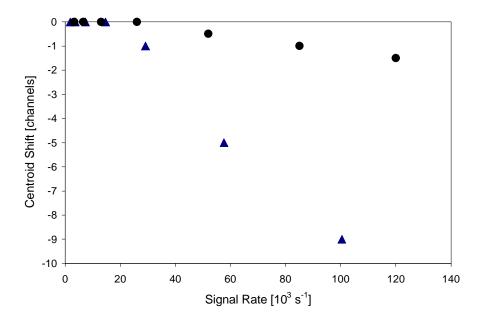
If signals occur at constant intervals, the effect of an undershoot will always be the same.

However, in a random sequence of pulses, the effect will vary from pulse to pulse.

$\Rightarrow$    spectral broadening

Baseline shifts tend to manifest themselves as a systematic shift in centroid position with event rate.

Centroid shifts for two 13 bit ADCs vs. random rate:

6. Stability

Stability vs. temperature is usually adequate with modern electronics in a laboratory environment.

• Note that temperature changes within a module are typically much smaller than ambient.

However: Highly precise or long-term measurements require spectrum stabilization to compensate for changes in gain and baseline of the overall system.

Technique: Using precision pulsers place a reference peak at both the low and high end of the spectrum.

(Pk. Pos. 2) – (Pk. Pos. 1)  $\rightarrow$    Gain, … then
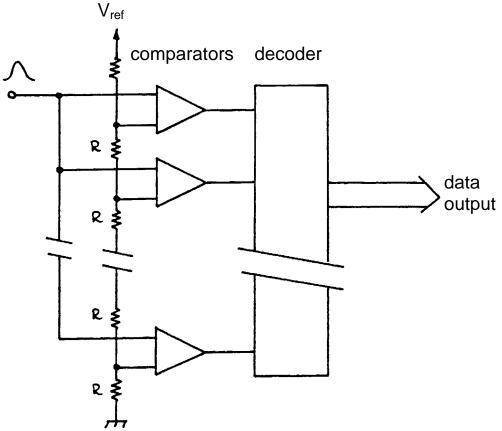
(Pk. Pos. 1) or (Pk. Pos. 2) $\rightarrow$    Offset

Traditional Implementation: Hardware, spectrum stabilizer module

Today, it is more convenient to determine the corrections in software. These can be applied to calibration corrections or used to derive an electrical signal that is applied to the hardware (simplest and best in the ADC).

# Analog to Digital Conversion Techniques

1. Flash ADC



The input signal is applied to $n$ comparators in parallel. The switching thresholds are set by a resistor chain, such that the voltage difference between individual taps is equal to the desired measurement resolution.

$2^n$ comparators for $n$ bits (8 bit resolution requires 256 comparators)

Feasible in monolithic ICs since the absolute value of the resistors in the reference divider chain is not critical, only the relative matching.

Advantage:      short conversion time (<10 ns available)
Drawbacks:     limited accuracy (many comparators)
                   power consumption
                   Differential non-linearity ~ 1%
                   High input capacitance (speed is often limited by the analog driver feeding the input)

## 2. Successive Approximation ADC

Pulse Stretcher　　　　Comparator　　　　Control Logic,
　　　　　　　　　　　　　　　　　　　　　Register + DAC



Sequentially add levels proportional to
$2^n$, $2^{n-1}$, … $2^0$ and set corresponding
bit if the comparator output is high
(DAC output < pulse height)

$n$ conversion steps yield $2^n$ channels,
　　　　　　　　　　i.e. 8K channels require 13 steps

Advantages:　　　speed (~ $\mu$s)
　　　　　　　　　high resolution
　　　　　　　　　ICs (monolithic + hybrid) available

Drawback:　　　Differential non-linearity (typ. 10 – 20%)

　　　　　　　Reason:　　Resistors that set DAC output must be
　　　　　　　　　　　　extremely accurate.

　　　　　　　For DNL < 1% the resistor determining the $2^{12}$ level
　　　　　　　in an 8K ADC must be accurate to $< 2.4 \cdot 10^{-6}$.

## 3. Wilkinson ADC



The peak signal amplitude is acquired by a pulse stretcher and transferred to a memory capacitor. Then, simultaneously,

1. the capacitor is disconnected from the stretcher,
2. a current source is switched to linearly discharge the capacitor,
3. a counter is enabled to determine the number of clock pulses until the voltage on the capacitor reaches the baseline.

Advantage:     excellent differential linearity
                        (continuous conversion process)

Drawbacks:     slow – conversion time = $n \cdot T_{clock}$
                        ($n=$ channel number $\propto$ pulse height)

$T_{clock}=$ 10 ns $\rightarrow T_{conv}=$ 82 $\mu$s for 13 bits

Clock frequencies of 100 MHz typical, but >400 MHz possible with excellent performance

"Standard" technique for high-resolution spectroscopy.

# Time Digitizers

## 1. Counter

Simplest arrangement.

Count clock pulses between start and stop.

Limitation:  Speed of counter

Current technology limits speed of counter system
to about 1 GHz

$\Longrightarrow$    $\Delta t$ = 1 ns

Multi-hit capability

## 2. Analog Ramp

Commonly used in high-resolution digitizers ($\Delta t$ = 10 ps)

Principle:   charge capacitor through switchable current source

Start pulse:        turn on current source

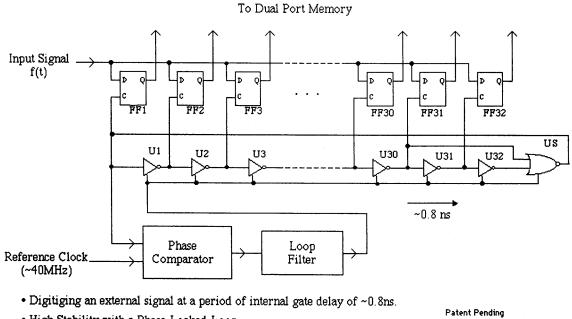Stop pulse:        turn off current source

$\Longrightarrow$    Voltage on storage capacitor

Use Wilkinson ADC with smaller discharge current
to digitize voltage.

Drawbacks:        No multi-hit capability
Deadtime

## 3. Digitizers with Clock Interpolation

Most experiments in HEP require multi-hit capability, no deadtime

Commonly used technique for time digitization (Y. Arai, KEK)

To Dual Port Memory

Input Signal f(t)

FF1 FF2 FF3 FF30 FF31 FF32

U1 U2 U3 U30 U31 U32 US

~0.8 ns

Reference Clock (~40MHz) → Phase Comparator → Loop Filter

- Digitizing an external signal at a period of internal gate delay of ~0.8ns.
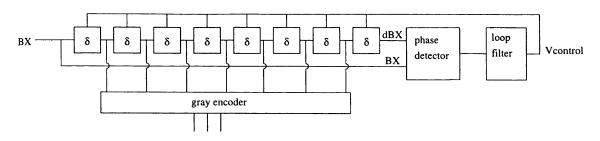- High Stability with a Phase Locked Loop.
- Long time range (>3 us) & No deadtime by a Dual Port Memory.
- High precision, High Density & Low Cost LSI.

Patent Pending
- S63-067314 (JP)
- H3-133169 (JP)
- H6-69507 (JP)
- 95300652.5 (EU)

Clock period interpolated by inverter delays (U1, U2, …).
Delay can be fine-tuned by adjusting operating point of inverters.

Delays stabilized by delay-locked loop

BX — δ δ δ δ δ δ δ δ dBX → phase detector → loop filter → Vcontrol

BX

gray encoder

Devices with 250 ps resolution fabricated and tested.

see Y. Arai et al., IEEE Trans. Nucl. Sci. **NS-45/3** (1998) 735-739
and references therein.