IX.5. Noise in Transistors

a) Noise in Field Effect Transistors

The primary noise sources in field effect transistors are

a) thermal noise in the channel (as in resistors)

b) gate current in JFETs

Since the area of the gate is small, this contribution to the noise is very small and usually can be neglected.

Thermal velocity fluctuations of the charge carriers in the channel superimpose a noise current on the output current.

The spectral density of the noise current at the drain is

$$i_{nd}^2 = \frac{N_{C,tot} q_e}{L^2} \mu_0 \, 4k_B T_e$$

The current fluctuations depend on the number of charge carriers in the channel $N_{C,tot}$ and their thermal velocity, which in turn depends on their temperature T_e and low field mobility μ_0. Finally, the induced current scales with 1/L because of Ramo's theorem.

To make practical use of the above expression it is necessary to express it in terms of directly measureable device parameters. Since the transconductance in the saturation region

$$g_m \propto \frac{W}{L} \mu N_{ch} d$$

one can express the noise current as

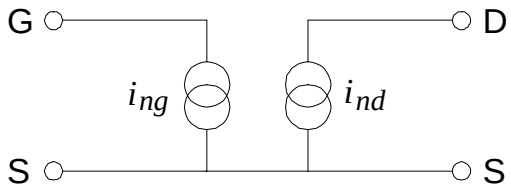
$$i_{nd}^2 = \gamma_n g_m \, 4k_B T_0$$

where T_0= 300 K and γ_n is a semi-empirical constant that depends on the carrier concentration in the channel and the device geometry.

In a JFET the gate noise current is the shot noise associated with the reverse bias current of the gate-channel diode

$$i_{ng} = 2q_e I_G$$

The noise model of the FET



The gate and drain noise currents are independent of one another.

However, if an impedance Z is connected between the gate and the source, the gate noise current will flow through this impedance and generate a voltage at the gate

$$v_{ng} = Z\, i_{ng}$$

leading to an additional noise current at the output $g_m v_{ng}$, so that the total noise current at the output becomes

$$i_{no}^2 = i_{nd}^2 + (g_m Z\, i_{ng})^2$$

To allow a direct comparison with the input signal, this cumulative noise will be referred back to the input to yield the equivalent input noise voltage

$$v_{ni}^2 = \frac{i_{no}^2}{g_m^2} = \frac{i_{nd}^2}{g_m^2} + Z i_{ng}^2 \equiv v_n^2 + Z i_n^2$$

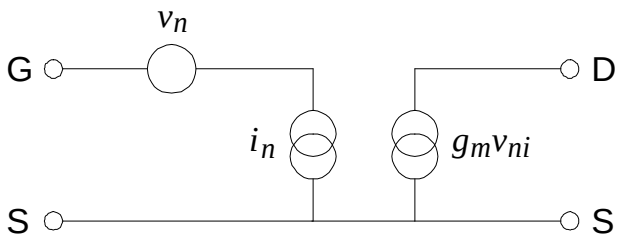
i.e. referred to the input, the drain noise current i_{nd} translates into a noise voltage source

$$v_n^2 = 4k_B T_0 \frac{\gamma_n}{g_m}$$

The noise coefficient γ_n is usually given as 2/3, but is typically in the range 0.5 to 1 (exp. data will shown later).

This expression describes the noise of both JFETs and MOSFETs.

In this parameterization the noise model becomes



where v_n and i_n are the input voltage and current noise. As was shown above, these contribute to the total input noise voltage v_{ni}, which in turn translates to the output through the transconductance g_m to yield a noise current at the output $g_m v_{ni}$.

The equivalent noise charge

$$Q_n^2 = i_n^2 F_i T_S + v_n^2 C_i^2 \frac{F_v}{T_S}$$

For a typical JFET g_m= 0.02, C_i= 10 pF and I_G < 150 pA. If F_i=F_v=1

$$Q_n^2 = 1.9 \cdot 10^9 T_S + \frac{3.25 \cdot 10^{-3}}{T_S}$$

As the shaping time T_S decreases, the current noise contribution decreases and the voltage noise contribution increases. For T_S= 1 μs the current contribution is 43 el and the voltage contribution 3250 el, so the current contribution is negligible, except in very low frequency applications.

Optimization of Device Width

For a given device technology and normalized operating current I_D/W both the transconductance and the input capacitance are proportional to device width W

$$g_m \propto W \quad \text{and} \quad C_i \propto W$$

so that the ratio

$$\frac{g_m}{C_i} = const$$

Then the signal-to-noise ratio can be written as

$$\left(\frac{S}{N}\right)^2 = \frac{(Q_s/C)^2}{v_n^2} = \frac{Q_s^2}{(C_{\text{det}} + C_i)^2}\frac{g_m}{4k_B T_0 \Delta f}$$

$$\left(\frac{S}{N}\right)^2 = \frac{Q_s^2}{\Delta f}\frac{1}{4k_B T_0}\left(\frac{g_m}{C_i}\right)\frac{1}{C_i\left(1+\frac{C_{\text{det}}}{C_i}\right)^2}$$

S/N is maximized for $C_i = C_{det}$ (“capacitive matching”).

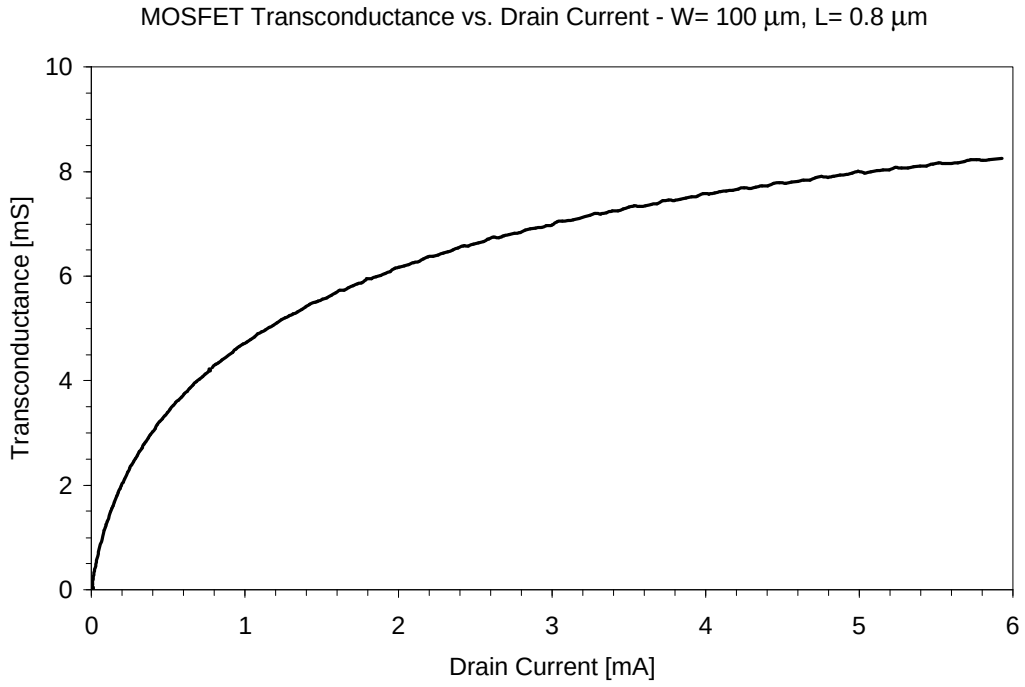
$C_i << C_{det}$: The detector capacitance dominates, so the effect of increased transistor capacitance is negligible.
As the device width is increased the transconductance increases and the equivalent noise voltage decreases, so S/N improves.

$C_i > C_{det}$: The equivalent input noise voltage decreases as the device width is increased, but only with $1/\sqrt{W}$, so the increase in capacitance overrides, decreasing S/N.

Minimum Obtainable Noise Charge

Device scaling can be used to determine the minimum obtainable noise charge for a given device technology.

The transconductance of an FET increases with drain current as shown below.



However, noise only decreases up to a certain current. The reason is that the noise from parasitic source and gate resistances becomes significant.

$$v_{ni}^2 = 4k_B T\left(\frac{\gamma_n}{g_m} + R_G + R_S\right)$$

Assume that a transistor of width W assumes its minimum noise at a current I_d with an associated transconductance g_m.

Since the parasitic gate and source resistances are both inversely proportional to device width, their relative contribution at constant current density I_d/W will be the same for all widths of transistors using the same technology (and device length).

Thus, to obtain minimum noise one can tailor the FET to a given detector by scaling the device width and keeping the current density I_d/W constant.

Within this framework one can characterize the device technology by the normalized transconductance and input capacitance

$$g_m' = \frac{g_m}{W} \quad \text{and} \quad C_i' = \frac{C_i}{W}$$

and use these quantities to scale to any other device width. Since the equivalent input noise voltage

$$v_n^2 \propto \frac{1}{g_m}$$

the normalized input noise voltage is

$$v_n' = v_n \sqrt{W}$$

Using these quantities the equivalent noise charge can be written as

$$Q_n^2 = 4k_B T_0 \frac{\gamma_n}{W g_m'} \frac{F_v}{T_S} (C_d + C_s + W C_i')^2$$

where C_s is any stray capacitance present at the input in addition to the detector capacitance C_d and the FET capacitance WC_i'.

For $WC_i' = C_d + C_s$ the noise attains its minimum value

$$Q_{n,\min} = \sqrt{\frac{16 k_B T_0}{\kappa_n} \frac{F_v}{T_S} (C_d + C_s)}$$

where

$$\kappa_n \equiv \frac{g_m}{\gamma_n C_i}$$

is a figure of merit for the noise performance of the FET.

Example:

CMOS transistor with 1.2 μm channel length

At I_d/W= 0.3 A/m g_m/C_i= 3·10^{-9} s^{-1} and γ_n= 1.

For a CR-RC shaper with a 20 ns shaping time and an external capacitance

C_d+C_s= 7.5 pF

$Q_{n,min}$= 88 aC = 546 electrons,

achieved at a device width W= 5 mm, and a drain current of 1.5 mA.

The obtainable noise improves with the inverse square root of the shaping time, up to the point where $1/f$ noise becomes significant. For example, at T= 1 μs

$Q_{n,min}$= 1.8 aC = 11 electrons,

although in practice additional noise contributions will increase the obtainable noise beyond this value.

Measured values of the noise coefficient γ_n for various *n*- and *p*-MOSFETs of various geometries for three normalized drain currents I_d/W.

Type	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
Width	75	75	1332	1332	888	888	1332	1332
Length	1.2	1.2	1.2	1.2	2.2	2.2	3.2	3.2
***I*$_d$ */W*= 0.03**								
0 Mrad			0.81	0.61	0.64	0.59	0.66	0.50
5 Mrad			2.17	0.84	1.00	0.58	1.50	0.69
***I*$_d$ */W*= 0.1**								
0 Mrad	1.10	0.70	1.20	1.10	0.80	0.80	0.80	0.60
5 Mrad	3.80	1.10	3.40	1.60	1.30	0.90	1.70	0.70
***I*$_d$ */W*= 0.3**								
0 Mrad	1.60	1.30	2.00	1.70	1.10	1.00	1.10	0.77
5 Mrad	5.00	2.90	4.80	2.70	1.60	1.40	1.20	0.81

Short channel *n*-MOSFETs tend to have higher noise coefficients at short channel lengths, probably due to increased electron temperature at high fields.

The table also shows the noise degradation after irradiation.

Since they are majority carrier devices, MOSFETs are insensitive to displacement damage, but they are affected by ionization damage, which leads to charge buildup in the oxide and the formation of interface states.

See H. Spieler, Introduction to Radiation-Resistant Semiconductor Devices and Circuits, tutorial, in A.H. Lumpkin, C.E. Eyberger (eds.) *Beam Instrumentation, Proceedings of the Seventh Workshop*, AIP Conference Proceedings 390, American Institute of Physics, Woodbury, NY, 1997, ISBN 1-56396-612-3

and http://www-physics.lbl.gov/~spieler

The preceding discussion has neglected $1/f$ noise, which adds a constant contribution independent of shaping time

$$Q_{nf}^2 \propto A_f C_{tot}^2$$

Although excess low frequency noise is determined primarily by the concentration of unwanted impurities and other defects, their effect in a specific technology is also affected by device size. For some forms of $1/f$ noise

$$A_f = \frac{K_f}{WL\, C_g^2}$$

where C_g is the gate-channel capacitance per unit area, and K_f is an empirical constant that is device and process dependent.

Typical values of the noise constant for various device types:

p-MOSFET	$K_f \approx 10^{-32}$ C^2/cm^2
n-MOSFET	$K_f \approx 4{\cdot}10^{-31}$ C^2/cm^2
JFET	$K_f \approx 10^{-33}$ C^2/cm^2

Specific implementations can improve on these values.

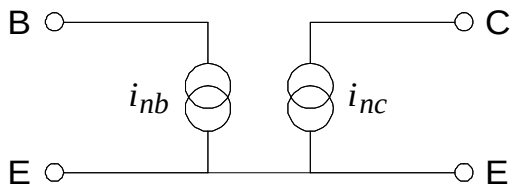
> One should note that this model is not universally applicable, since excess noise usually does not exhibit a pure $1/f$ dependence; especially in PMOS devices one often finds several slopes. In practice, one must test the applicability of this parameterization by comparing it with data before applying it to scaled amplifiers.

Nevertheless, as a general rule, devices with larger gate area $W{\cdot}L$ tend to exhibit better "$1/f$" noise characteristics.

b) Noise in Bipolar Transistors

In bipolar transistors the shot noise from the base current is important.

The basic noise model is the same as shown before, but the magnitude of the input noise current is much greater, as the base current will be 1 – 100 μA rather than <100 pA.



The base current noise is shot noise associated with the component of the emitter current provided by the base.

$$i_{nb}^2 = 2q_e I_B$$

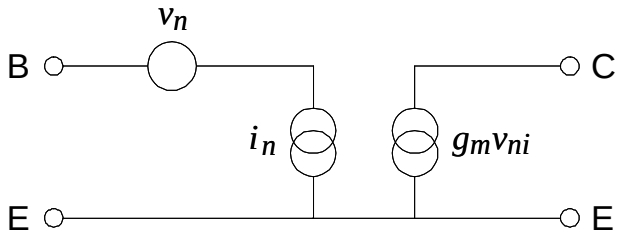
The noise current in the collector is the shot noise originating in the base-emitter junction associated with the collector component of the emitter current.

$$i_{nc}^2 = 2q_e I_C$$

Following the same argument as in the analysis of the FET, the output noise current is equivalent to an equivalent noise voltage

$$v_n^2 = \frac{i_{nc}^2}{g_m^2} = \frac{2q_e I_C}{(q_e I_C / k_B T)^2} = \frac{2(k_B T)^2}{q_e I_C}$$

yielding the noise equivalent circuit



where i_n is the base current shot noise i_{nb}.

The equivalent noise charge

$$Q_n^2 = i_n^2 F_i T_S + v_n^2 C_i^2 \frac{F_v}{T_S} = 2q_e I_B F_i T_S + \frac{2(k_B T)^2}{q_e I_C} C_{tot}^2 \frac{F_v}{T_S}$$

Since $I_B = I_C / \beta_{DC}$

$$Q_n^2 = 2q_e \frac{I_C}{\beta_{DC}} F_i T_S + \frac{2(k_B T)^2}{q_e I_C} C_{tot}^2 \frac{F_v}{T_S}$$

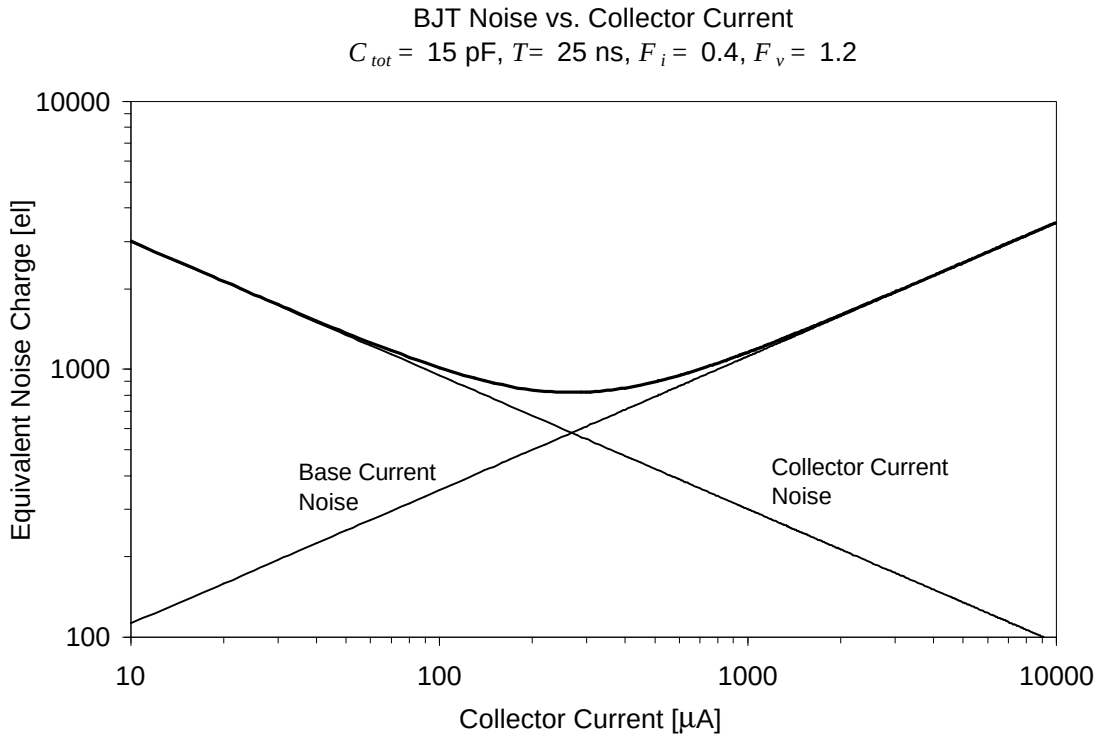
The current noise term increases with I_C, whereas the second (voltage) noise term decreases with I_C.

Thus the noise attains a minimum

$$Q_{n,\min}^2 = 4k_B T \frac{C_{tot}}{\sqrt{\beta_{DC}}} \sqrt{F_i F_v}$$

at a collector current

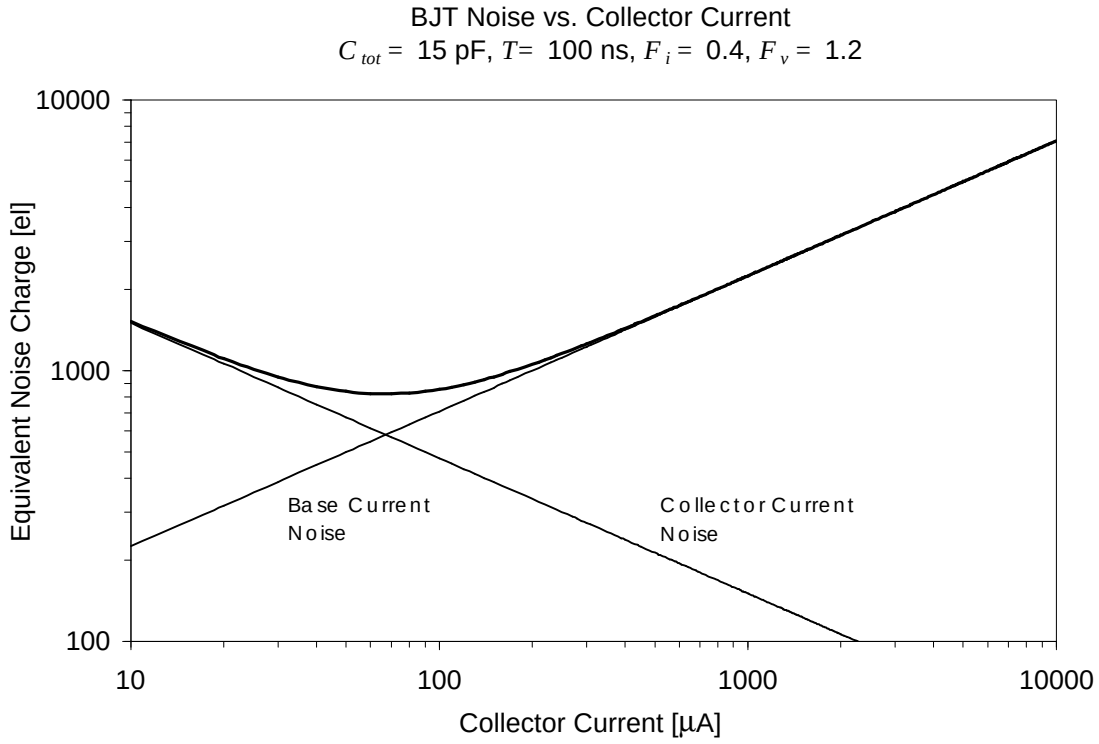
$$I_C = \frac{k_B T}{q_e} C_{tot} \sqrt{\beta_{DC}} \sqrt{\frac{F_v}{F_i}} \frac{1}{T_S}$$



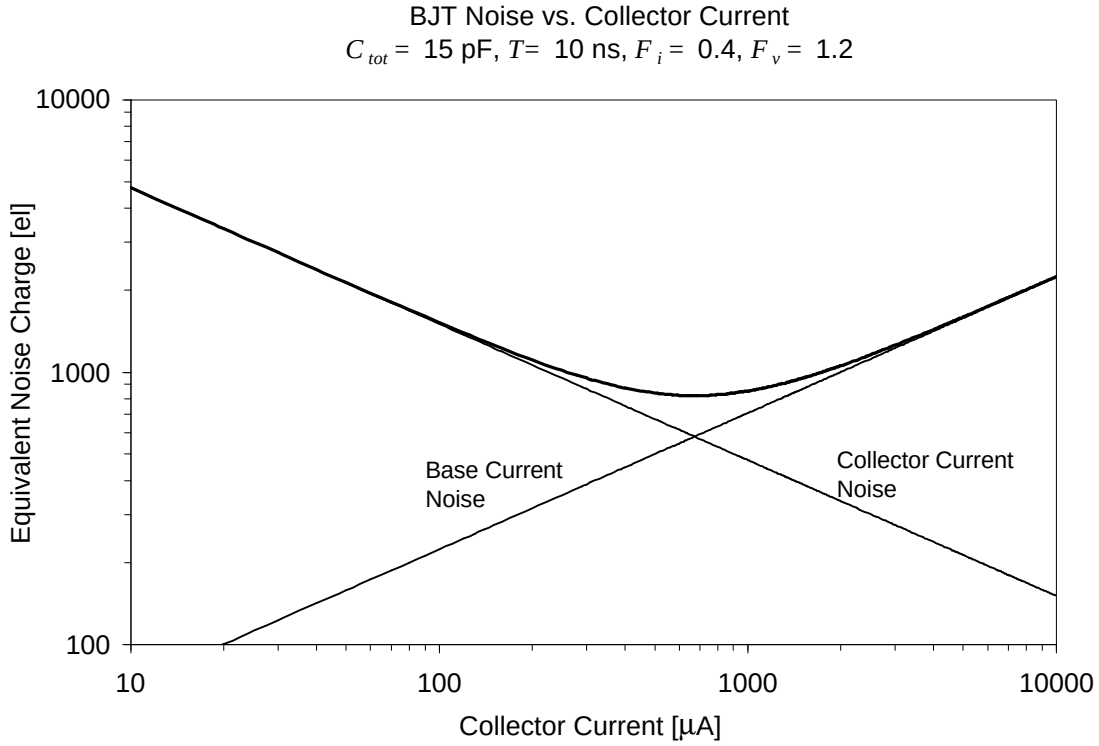
For a given shaper, the minimum obtainable noise is determined only by the total capacitance at the input and the DC current gain of the transistor, *not by the shaping time*.

The shaping time only determines the current at which this minimum noise is obtained

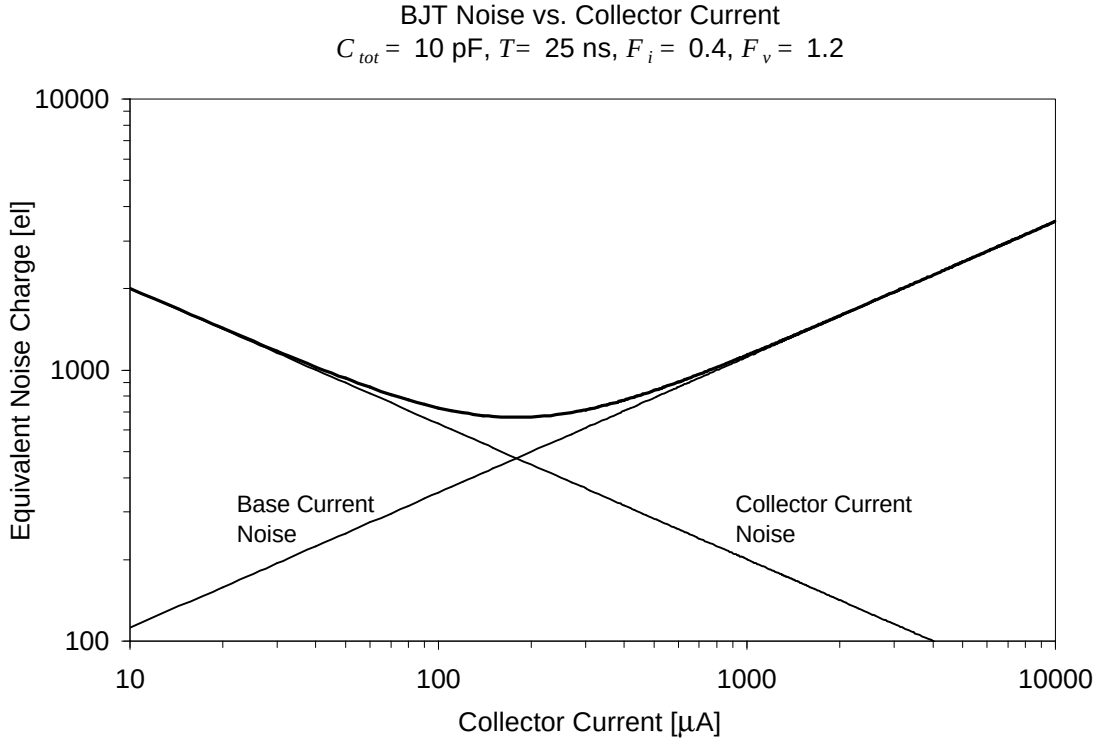
T= 100 ns

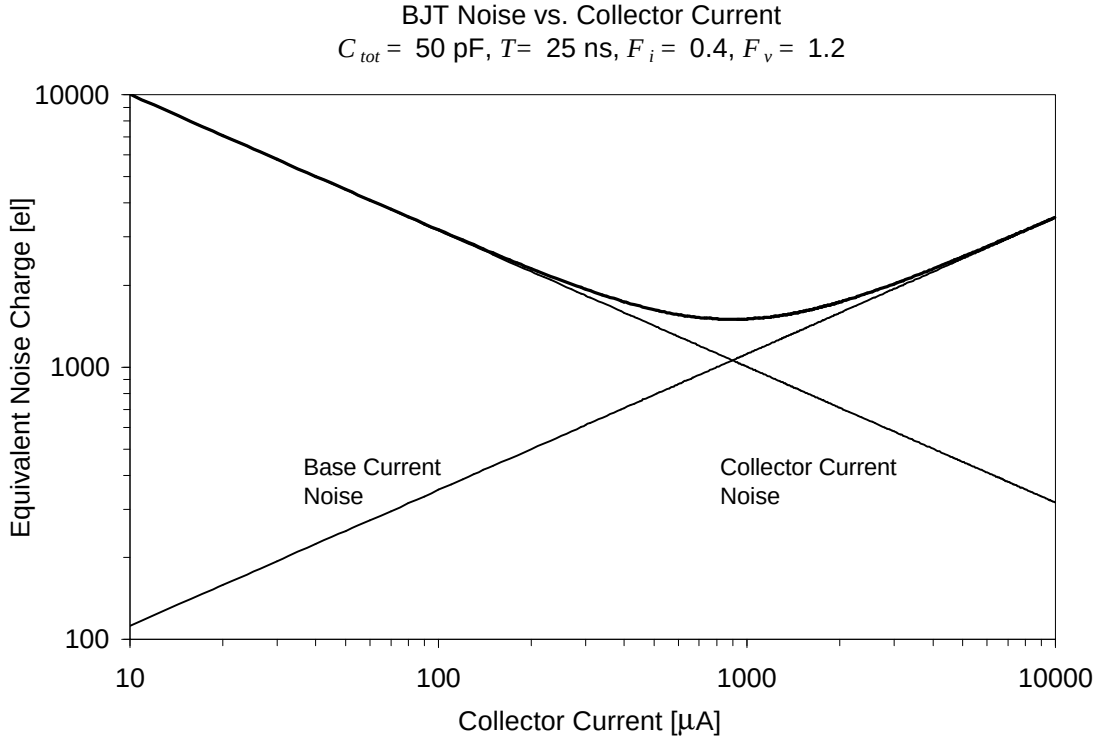


T= 10 ns



Increasing the capacitance at the input shifts the collector current noise curve upwards, so the noise increases and the minimum shifts to higher current.





For a CR-RC shaper

$$Q_{n,\min} = 772\left[\frac{el}{\sqrt{pF}}\right]\cdot\frac{\sqrt{C_{tot}}}{\sqrt[4]{\beta_{DC}}}$$

obtained at $$I_c = 26\left[\frac{\mu A\cdot ns}{pF}\right]\cdot\frac{C_{tot}}{\tau}\sqrt{\beta_{DC}}$$

Since typically $\beta_{DC} \approx 100$, these expressions allow a quick and simple estimate of the noise obtainable with a bipolar transistor.

- Note that specific shapers can be optimized to minimize either the current or the voltage noise contribution, so both the minimum obtainable noise and the optimum current will be change with respect to the above estimates.

The noise characteristics of bipolar transistors differ from field effect transistors in four important aspects:

1. The equivalent input noise current cannot be neglected, due to base current flow.
2. The total noise goes through a minimum as device current is increased, unlike an FET where noise decreases monotonically with current.
3. The minimum obtainable noise does not depend on the shaping time.
4. The input capacitance is usually negligible.

The last statement requires some explanation.

The input capacitance of a bipolar transistor is dominated by two components,

1. the geometrical junction capacitance, or transition capacitance C_{TE}, and
2. the diffusion capacitance C_{DE}.

The transition capacitance (i.e. the “geometrical” capacitance of the base-emitter depletion region) in small devices is typically about 0.5 pF.

The diffusion capacitance depends on the current flow I_E through the base-emitter junction and on the base width W, which sets the diffusion profile.

$$C_{DE} = \frac{\partial q_B}{\partial V_{be}} = \frac{q_e I_E}{k_B T}\left(\frac{W}{2D_B}\right) \equiv \frac{q_e I_E}{k_B T} \cdot \frac{1}{\omega_{Ti}}$$

where D_B is the diffusion constant in the base and ω_{Ti} is a frequency that characterizes carrier transport in the base. ω_{Ti} is roughly equal to the frequency where the current gain of the transistor is unity.

Inserting some typical values, I_E=100 μA and ω_{Ti} =10 GHz, yields C_{DE}= 0.4 pF. The transistor input capacitance C_{TE}+C_{DE}= 0.9 pF, whereas FETs providing similar noise values at comparable currents have input capacitances in the range 5 – 10 pF.

Except for low capacitance detectors, the current dependent part of the BJT input capacitance is negligible, so it will be neglected in the following discussion. For practical purposes the amplifier input capacitance can be considered constant at 1 ... 1.5 pF.

This leads to another important conclusion.

Since the primary noise parameters do not depend on device size and there is no significant linkage between noise parameters and input capacitance

- Capacitive matching does not apply to bipolar transistors.

Indeed, capacitive matching is a misguided concept for bipolar transistors. Consider two transistors with the same DC current gain but different input capacitances. Since the minimum obtainable noise

$$Q_{n,\min}^2 = 4k_B T \frac{C_{tot}}{\sqrt{\beta_{DC}}} \sqrt{F_i F_v} \ ,$$

increasing the transistor input capacitance merely increases the total input capacitance C_{tot} and the obtainable noise.

When to use FETs and when to use BJTs?

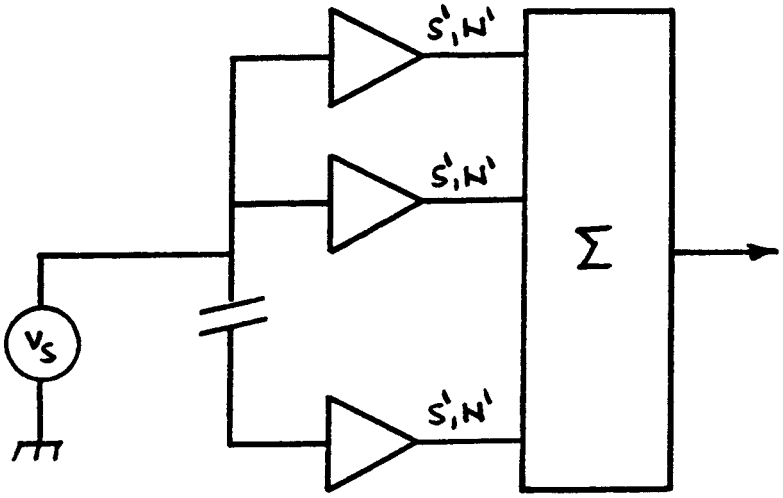
Since the base current noise increases with shaping time, bipolar transistors are only advantageous at short shaping times.

With current technologies FETs are best at shaping times greater than 50 to 100 ns, but decreasing feature size of MOSFETs will improve their performance.

Noise Optimization - Capacitive Matching Revisited

"Capacitive Matching" is often presented as a universal criterion for noise optimization. The results derived for bipolar transistors already show that capacitive matching does not apply in all amplifiers. This discussion is supposed to clarify where capacitive matching is useful and where it isn't.

Consider an array of amplifiers with both current and voltage noise sources. As in previous derivations of the equivalent noise charge, the amplifiers are assumed to have voltage-sensitive inputs. Furthermore, to simplify the analysis, the amplifiers do not utilize feedback.



Of course, in considering the current and voltage noise contributions, one can follow a formal argument based on the noise charge

$$Q_n^2 = i_n^2 F_i T_S + v_n^2 C_i^2 \frac{F_v}{T_S}$$

Since the current noise contribution does not depend on capacitance, matching the amplifier input capacitance to the detector capacitance should be irrelevant. On the other hand, since the voltage contribution does depend on capacitance, a correlation between v_n and C_i can yield an optimization condition.

Nevertheless, reviewing the formation of signal and noise in detail is useful to clarify the limits of capacitive matching.

1. Current Noise

For the noise currents originating in the individual amplifiers, the common connection to the signal source is a summing node, so if i_n' is the equivalent noise current of a single amplifier, for n amplifiers the total input noise current flowing through the signal source impedance is

$$i_n = \sqrt{n} \cdot i_n'$$

The flow of this current through the input impedance Z_i formed by the parallel connection of the detector capacitance and amplifier capacitances gives rise to a noise voltage

$$v_n = i_n Z_i$$

This voltage is applied in parallel to all amplifier inputs, so at the output of an individual amplifier (assuming gain A) the noise level is

$$N'(n) = Av_n = A\sqrt{n}\, i_n' Z_i$$

At the output of the summing circuit, the cumulative noise from all amplifier outputs becomes

$$N(n) = \sqrt{n}N'(n) = An\, i_n' Z_i$$

Since the amplifiers respond to voltage, the magnitude of the signal applied to all amplifiers is the same, which for a signal current i_s is

$$v_s = i_s Z_i$$

In the summed output the signals add coherently, so that

$$S(n) = nAi_s Z_i$$

and the signal-to-noise ratio

$$\frac{S(n)}{N(n)} = \frac{nAi_s Z_i}{Ani_n' Z_i} = \frac{i_s}{i_n'} = \frac{S(1)}{N(1)} \ ,$$

the same as for a single amplifier

Paralleling amplifiers does not affect the signal-to-noise ratio if only current noise is present.

Varying the amplifier input capacitance is irrelevant. As the total input capacitance increases, the noise voltage developed at the input decreases with Z_i, but so does the signal voltage, so the signal-to-noise ratio is unaffected.

2. Voltage Noise

The voltage noise contribution differs from the current noise in an important aspect:

- Voltage noise is not additive at the input.

This statement can be justified with two arguments, the first more physical and the second more formal.

1. Voltage noise tends to originate within a device (e.g. thermal noise of an FET channel or collector shot noise in a BJT) and appears as a noise current at the output, which is mathematically transformed to the input. This noise voltage is not physically present at the input and is not affected by any connections or components in the input circuit.

2. The noise voltage sources that represent all voltage noise contributions of a given amplifier are in series with the individual inputs. Since the input impedance of the amplifier is postulated to be infinite, the source impedance is by definition negligible in comparison, so the noise voltage associated with a given amplifier only develops across the input of that amplifier.

Assume that each amplifier has an input referred noise v_n' and an input capacitance C_i'.

Then the input signal voltage

$$v_s = \frac{Q_s}{C}$$

where C is the total input capacitance including the detector

$$C = C_{\text{det}} + nC_i'$$

The signal at each amplifier output is

$$S' = Av_s = A\frac{Q_s}{C_{\text{det}} + nC_i'}$$

The noise at each amplifier output is

$$N' = Av_n'$$

After summing the n outputs the signal-to-noise ratio

$$\frac{S(n)}{N(n)} = \frac{nS'}{\sqrt{n}N'} = \sqrt{n}\frac{S'}{N'} = \sqrt{n}\frac{A\dfrac{Q_s}{C_{\text{det}} + nC_i'}}{Av_n'} = \frac{Q_s}{v_n'/\sqrt{n}} \cdot \frac{1}{C_{\text{det}} + nC_i'}$$

which assumes a maximum when $C_{\text{det}} = nC_i$'.

Under this "capacitive matching" condition $\Sigma C_i' = C_{\text{det}}$ the signal-to-noise ratio

$$\frac{S}{N} = \frac{Q_s}{v_n'}\sqrt{\frac{C_{\text{det}}}{C_i'}}\frac{1}{C_{\text{det}} + nC_i'} = \frac{Q_s}{v_n'}\sqrt{\frac{C_{\text{det}}}{C_i'}}\frac{1}{2C_{\text{det}}}$$

or

$$\frac{S}{N} = \frac{1}{2}\frac{Q_s}{v_n'\sqrt{C_i'}} \cdot \frac{1}{\sqrt{C_{\det}}}$$

Since v_n' and C_i' are properties of the individual amplifier, i.e. constants, the signal-to-noise ratio decreases with the square root of detector capacitance

This relationship only holds if

1. the noise of the input amplifier/device decreases with increasing input capacitance.

2. the input capacitance is scaled with the detector capacitance ("capacitive matching")

The first point is critical; if the noise voltage of a device and its input capacitance are not correlated, capacitive matching is deleterious.

Example: A MOSFET operated in weak inversion has a transconductance that depends only on current, independent of geometry. If power consumption is to be kept constant, increasing the size of the device at the same operating current will not increase the transconductance, but it will increase the input capacitance and, as a result, the equivalent noise charge.

For both BJTs and FETs, the minimum obtainable noise increases with the square root of detector capacitance, although the physical origins for this behavior are quite different in the two types of devices.

Optimization for Low-Power

Optimizing the readout electronics in large vertex or tracking detector systems is not optimizing one characteristic, e.g. noise, alone, but finding an optimum compromise between noise, speed, and power consumption.

The minimum obtainable noise values obtained from the equations for both FETs and BJTs should be viewed as limits, not necessarily as desirable goals, since they are less efficient than other operating points.

First, consider two input transistors, which

provide the same overall noise with a given detector,

but differ in input capacitance.

Since the sum of detector and input capacitance determines the voltage noise contribution, the device with the higher input capacitance must have a lower equivalent noise voltage v_n, i.e. operate at higher current.

In general,

- low capacitance input transistors are preferable, and
- systems where the total capacitance at the input is dominated by the detector capacitance are more efficient than systems that are capacitively matched.

Capacitive matching – when it is applicable – should be viewed as a limit, not as a virtue.

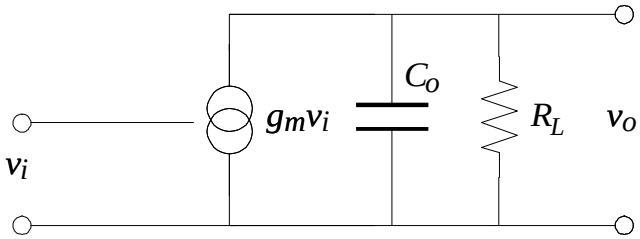
What is the optimum operating current for a given device?

Both response time, i.e. bandwidth, and noise depend on a common parameter, transconductance.

The relationship between noise and transconductance was shown above.

The dependence of bandwidth on transconductance is easy to derive.

Consider an amplifying device with transconductance g_m and a load resistance R_L.



The total capacitance at the output node is C_o.

The low frequency voltage gain is

$$A_v = \frac{v_o}{v_i} = g_m R_L$$

The bandwidth of the amplifier is determined by the output time constant

$$\tau_o = R_L C_o = \frac{1}{\omega_o}$$

Hence the gain-bandwidth product

$$A_v \omega_o = g_m R_L \cdot \frac{1}{R_L C_o} = \frac{g_m}{C_o}$$

is independent of the load resistance R_L, i.e. the voltage gain, but depends only on the device transconductance g_m and the capacitance at the output C_o.

The capacitance at the output node C_o depends on circuit topology and basic characteristics of the IC technology used. Often, the bandwidth is determined less by the inherent device speed, than by the stray capacitance to the substrate.

Since increasing transconductance yields both improved bandwidth and noise, a useful figure of merit for low power operation is the ratio of transconductance to device current g_m / I.

In a bipolar transistor

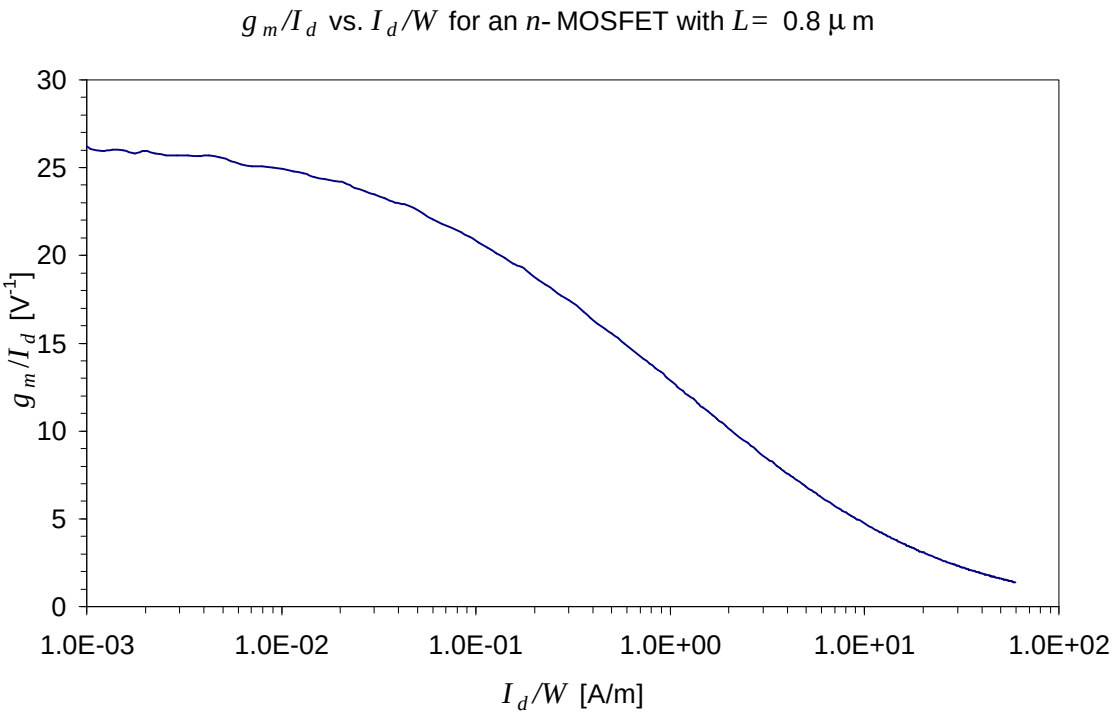
$$g_m = \frac{q_e}{k_B T} I_C$$

so g_m / I_c is constant

$$\frac{g_m}{I_C} = \frac{q_e}{k_B T}$$

In an FET the dependence of transconductance on drain current is more complicated.

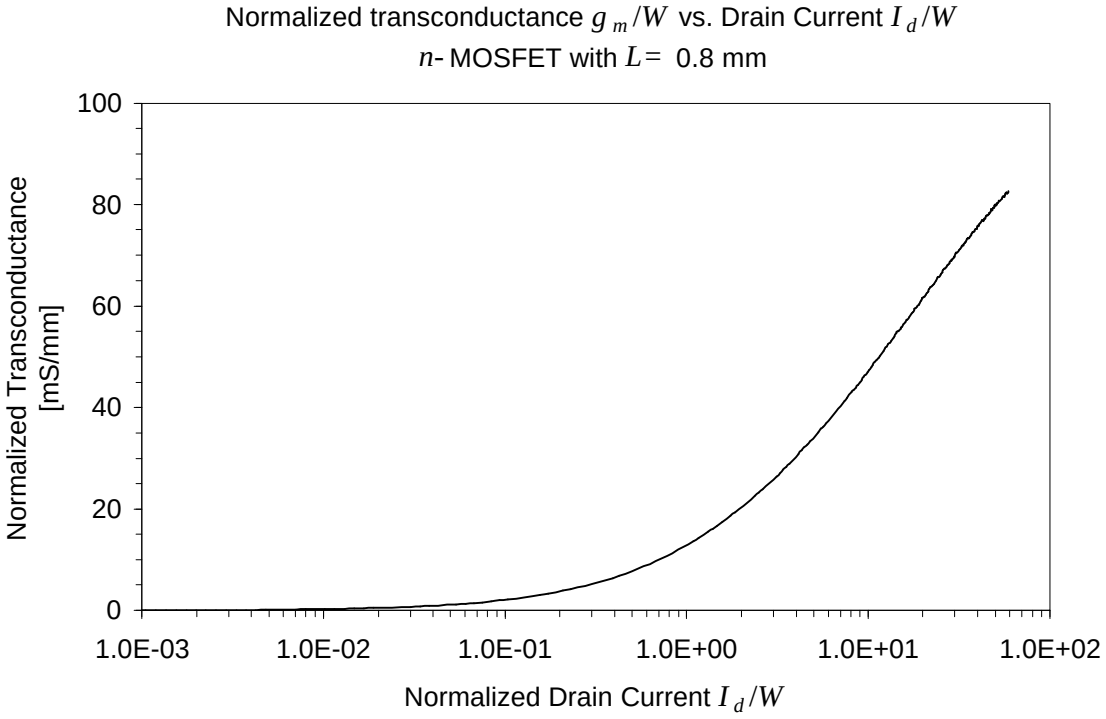
The figure below shows g_m/I_d as a function of normalized drain current I_d/W for a MOSFET with 0.8 µm channel length. This is a universal curve for all transistors using the same technology and channel length.



At low currents the MOSFET starts out with constant g_m/I_d, equal to a bipolar transistor. This is the weak inversion regime.

One then sees a rapid decrease in the regime 0.1 < I_d < 10 A/m (moderate inversion) and finally a gradual decrease at I_d > 10 A/m (strong inversion).

Note that although g_m/I_d is decreasing with current, the transconductance itself is increasing, but at a substantial penalty in current.



The strong inversion regime is most commonly used, especially when minimum noise is required, since it yields the highest transconductance.

Note, however, that the abscissa is logarithmic, and that the high transconductance in strong inversion comes at the expense of substantial power.

In systems where both speed and noise must be obtained at low power, for example HEP tracking detectors, the moderate inversion regime is advantageous, as it still provides 20 to 50% of the transconductance at 1/10 the power.

Having chosen a value of normalized drain current I_d/W that provides an adequate gain-bandwidth product, the required noise can be achieved adjusting the width of the FET, limited by capacitive matching.

Since in this scaling the current density remains constant, both the current and the transconductance increase proportionally with width. Thus the noise

$$v_n^2 \propto \frac{1}{g_m} \propto \frac{1}{I_D}$$

$$Q_n^2 \propto v_n^2 C_{tot}^2 \propto \frac{C_{tot}^2}{I_D}$$

so for a given noise level the required power

$$P \propto I_D \propto C_{tot}^2$$

A similar result obtains for bipolar transistors. The most efficient operating regime with respect to power is below the current for minimum noise

$$I_C = \frac{k_B T}{q_e} C_{tot} \sqrt{\beta_{DC}} \sqrt{\frac{F_v}{F_i}} \frac{1}{T_S}$$

In this regime the noise is dominated by voltage noise, so

$$Q_n^2 \approx \frac{2(k_B T)^2}{q_e I_C} C_{tot}^2 \frac{F_v}{T_S}$$

and as above for a given noise level

$$P \propto I_C \propto C_{tot}^2$$

The capacitance of the detector element strongly affects the required current in the input transistor, so reducing the capacitance not only improves noise performance, but also reduces power requirements.

As shown previously, this result can be used to compare the total power requirements for strip and pixel arrays.

Assume for a given area

strip detector:	n strips
pixel detector:	n x n pixels

If the capacitance is dominated by the strip-to-strip or pixel-to-pixel fringing capacitance.

$\Rightarrow$ capacitance proportional to periphery (pitch p and length l)

$$C \propto 2(l+p) \;\Rightarrow\; C_{pixel} \approx \frac{2}{n} C_{strip}$$

In the most efficient operating regime the power dissipation of the readout amplifier for a given noise level is proportional to the square of capacitance

$$P \propto C^2$$

$\Rightarrow$

$$P_{pixel} \approx \frac{4}{n^2} P_{strip}$$

n times as many pixels as strips

$\Rightarrow$

$$P_{pixel,tot} \approx \frac{4}{n} P_{strip}$$

$\Rightarrow$ Increasing the number of readout channels can reduce the total power dissipation!

The circuitry per cell does not consist of the amplifier alone, so a fixed power P_0 per cell must be added, bringing up the total power by $n^2 P_0$, so these savings are only realized in special cases.

Nevertheless, random addressable pixel arrays can be implemented with overall power densities comparable to strips.