Fabrication of Semiconductor Devices

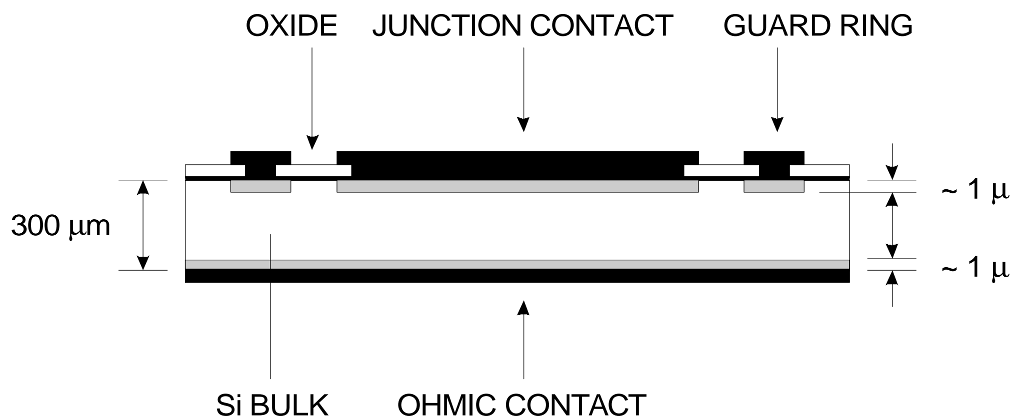
Ingredients of a semiconductor device fabrication process

1. bulk material, e.g. Si, Ge, GaAs
2. dopants to create *p*- and *n*-type regions
3. metallization to make contacts
4. passivation to protect the semiconductor surfaces from electrical and chemical contaminants

Practically all semiconductor devices are fabricated in a planar geometry (very few exceptions, e.g. large volume coaxial detectors)

1. the starting point is a semiconductor wafer
2. dopants are introduced from the surfaces

Typical planar detector diode structure



The guard ring is an additional junction that isolates the main junction from the edge of the wafer

Dopants are introduced by

1. thermal diffusion in a gaseous ambient at ~1000 °C

or

2. ion implantation

   accelerate dopant ions to 20 – 100 keV, depending on desired penetration depth

   The implanted ions will initially be distributed interstitially, so to render them electrically active as donors or acceptors they must be introduced to substitutional lattice sites ("activation".

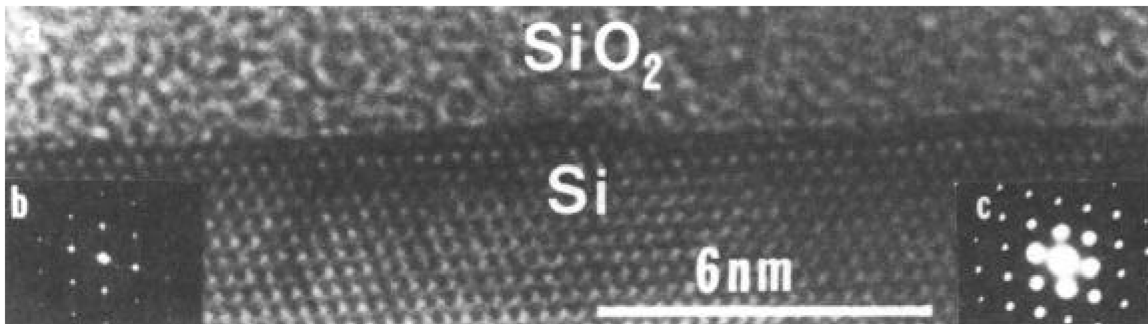
   This is accomplished by heating (annealing).

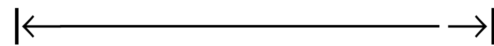
Protective layers immediately adjacent to the active semiconductor bulk must form a well controlled interface to the semiconductor lattice, to

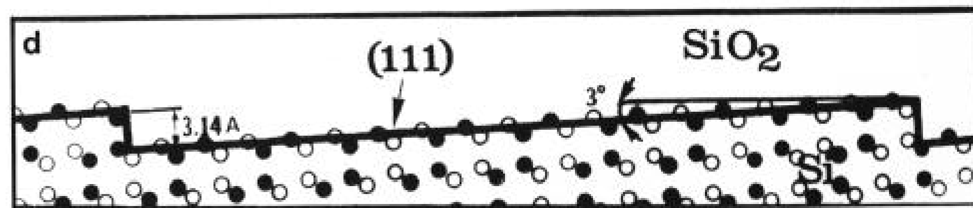
1. minimize additional charge states ("dangling" bonds)
2. avoid mechanical stress
   (mismatch of thermal expansion coefficients)

In these respects SiO_2 on Si is unequalled – indeed this is probably the single key ingredient that allows Si technology to achieve a circuit density that is at least an order of magnitude greater than in any other semiconductor.

Atomic resolution electron microscope image of SiO_2-silicon interface







(Gronsky et al., LBNL National Center for Electron Spectroscopy)

The highest quality oxides are “grown”, i.e. the silicon is exposed to an oxidizing ambient, which diffuses into the silicon and forms SiO_2.

Oxide can also be deposited. The quality of the interface is much inferior to grown SiO_2, so deposited oxide is used primarily for protective layers on non-critical surfaces or after the silicon has already been protected by a grown oxide.

Growth of a high-quality oxide with minimum contamination is time consuming, so a common technique is to grow a thin oxide layer to provide a good electrical interface and then deposit an additional layer of lesser quality oxide.

Oxide can be deposited at relatively low temperatures (low temperature oxide – LTO), which is advantageous if the duration of high-temperature steps must be limited (to minimize diffusion and preserve shallow junctions)

Metallization is applied either by evaporation or sputtering.

Since all of these processes are only to be applied to specifically controlled areas, “masks” are used to expose only selected areas to difusion, ion implantation, or etchants.

The patterning is accomplished by photolithography.

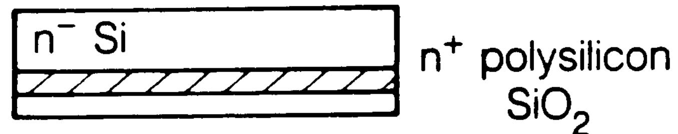
A photoresist is applied to the surface.

Exposure to light through a “mask” to cross-links the polymer in the desired areas.
(or the inverse – once can use positive or negative resist)

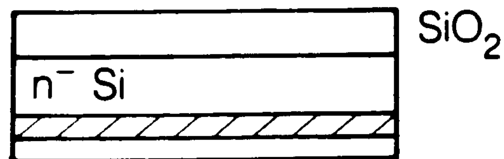
The exposed portions are removed by an appropriate solvent.

1. Backside contact (typically P diffusion or implant) – here P-doped polysilicon (discussed later)

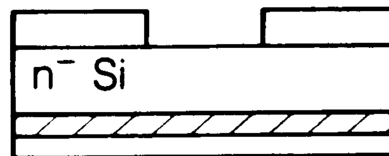
2. Deposition of silicon dioxide on the backside



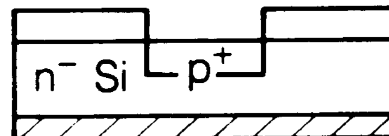
3. Thermal oxidation of the top surface



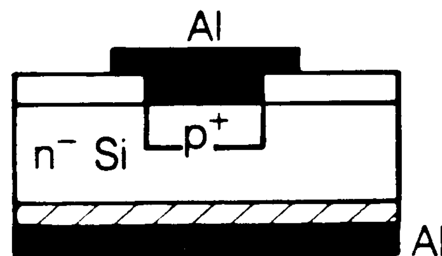
4. Photolithography and etching of the silicon dioxide



5. Boron doping to form p-type electrode and subsequent removal of backside oxide



6. Aluminum metallization and patterning to form contacts



All of these process steps provide many opportunities for the introduction of deleterious contaminants.

Especially critical are

a) wet-process steps

Immersion in a liquid bath exposes the sample to many more molecules than in air, so liquid chemicals and the water used for dilution must be extremely pure (sub ppb contaminant levels).

b) thermal processing (high temperatures promote diffusion)

Two approaches have been taken in the fabrication of silicon detectors with low reverse bias currents.

a) low temperature processing

(J. Kemmer, Nucl. Instr. and Meth. **226** (1984) 89)

pro: relatively simple and economical
(no deposition systems required)
most commonly used for detectors

con: marginal activation of implants,
restricts use of most IC techniques
not compatible with monolithically integrated electronics on same substrate

b) gettering

(S. Holland, IEEE Trans. Nucl. Sci. **NS-36** (1989) 282,
Nucl. Instr. and Meth. **A275** (1989) 537)

pro: very effective and removal of critical contaminants
reproducible
fully compatible with conventional IC processing

con: requires polysilicon deposition
some additional process complexity

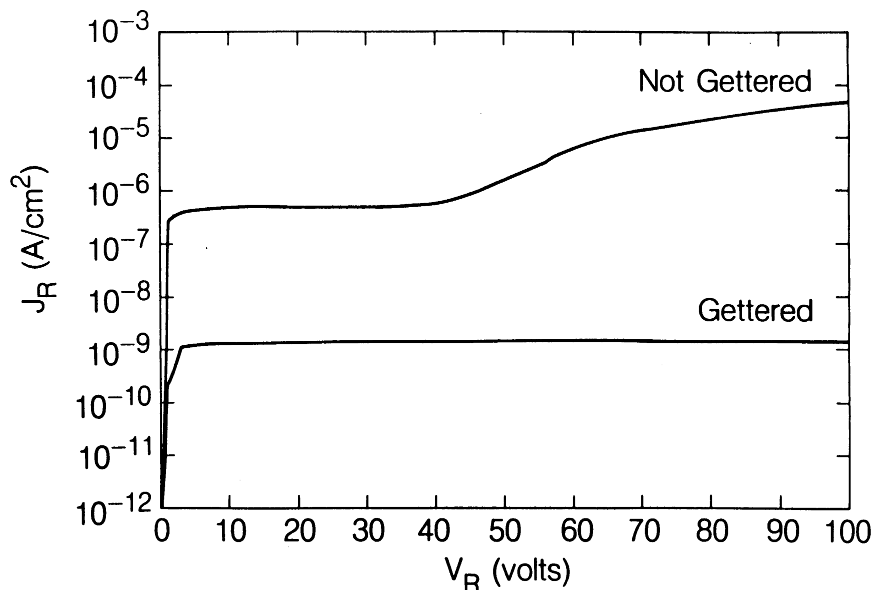
Gettering can be used to remove contaminants from the sensitive regions by providing capture sites for contaminants. This requires that the critical contaminants are sufficiently mobile so that they will diffuse to the gettering sites and be captured.

Fortuitously, the most common contaminants that introduce mid-gap states are fast diffusers!

Disordered materials tend to be efficient getters (e.g. polysilicon).
Gettering can be promoted by chemical affinity (Phosporus)

Both can be combined, e.g. P-doped polysilicon

Reduction of diode reverse bias current by gettering:



(S. Holland)

Next – just to get a flavor of the required attention to detail – listings of process steps in fabricating a detector diode.
First, a simplified sequence and then a more detailed sequence.

Detector Fabrication Process

(S. Holland, LBNL)

High-temperature process with very effective gettering to actively remove electrically active impurities from detector volume.

Fully compatible with conventional IC fabrication. Detectors and electronics have been integrated monolithically

S. Holland, H. Spieler: IEEE Trans. Nucl. Sci. **NS-37** (1990) 463
W. Snoeys et al.: IEEE Trans Nucl. Sci. **NS-39** (1992) 1263

1. Gettering Layer
   (also forms ohmic electrode of detector diode)
   a) Deposition of ~0.5 μm low-temperature oxide (LTO)
      ~1 hr at 400 °C
   b) Spin photoresist on wafer front side
   c) Etch backside oxide
   d) Deposit ~1.2 μm phosphorus-doped polysilicon
   e) Spin photoresist on wafer backside
   f) Remove front-side polysilicon
   g) Deposit capping LTO
   h) Spin photoresist on wafer back side to protect capping layer
   i) Remove LTO from wafer front side
2. Grow thermal oxide (steam, 4 hrs at 900 °C)
   forms 400 nm thick oxide
3. Deposit photoresist
4. Expose photoresist through mask with strip pattern, develop
5. Etch exposed oxide
6. Introduce p-dopant, typically boron, to form strip electrodes
   Two methods possible:
   a) thermal diffusion: expose to $B_2 0_3$ source for 30 min at 900 °C
   b) ion implantation: 30 keV B ions at dose of $2 \cdot 10^{15}$ cm^2
7. Drive-in and thermal anneal of implant, combined with oxidation
   40 min at 900 °C in steam followed by 80 min at 900 °C in N_2
8. Deposit 500 nm aluminum-silicon alloy for contacts

9. Spin on photoresist
10. Expose through contact mask to form strip metallization and bonding pads, develop resist
11. Etch metal
12. Coat front side with photoresist
13. Etch away backside oxide
14. Deposit 100 nm aluminum on back side to form ohmic contact
15. Forming gas anneal to reduce density of interface states at Si-SiO_2 interface: 20 min at 400 °C in 80% H_2 + 20% N_2

Additional intermediate steps:

Wafer cleaning prior to each furnace step (except post-metallization anneal):

1. immerse in 5:1 H_2S0_4:H_20_2 at 120 °C
2. HF etch
3. rinse in DI water
4. immerse in 5:1:1 solution of H_20:NH_4OH:H_20_2 at 65 °C
5. dilute HF etch
6. rinse in DI water
7. immerse in 5:1:1 solution of H_20:HCl:H_20_2 at 65 °C
9. rinse in DI water

This is just an outline!

Many more detailed steps are involved, so that a detector fabrication run requires 4 to 5 weeks.

For illustration, see the following detailed process flow.

Process flow for pixels on p-type substrates

S. Holland, 9/22/94

Starting material: >5kΩcm, 300 μm thick, <100> p-type silicon (Wacker).

(1) 4000A field oxidation

a. Standard prediffusion clean:
   5 minute piranha at l00 °C (WPS 2)
   DI water rinse (WPS 2)
   Dilute HF etch (WPS 2)
   DI water rinse (WPS 2)
   5 minute megasonic RCA I clean at 40°C (WPS 2)
   DI water rinse (WPS 2)
   Dilute HF etch (WPS 2)
   DI water rinse (WPS 1)
   5 minute megasonic RCA II clean at 40 °C (WPS 1)
   DI water rinse
b. Steam oxidation to grow 4000A field oxide, 4 hours at 900 °C using Thermco recipe WET4000A, tube 2-1, with TCA clean of furnace tube prior to oxidation using Thermco recipe 1TCACLN.
c. Measure oxide thickness on monitor wafers.

Approximate time required: I day.

(2) Mask 1 (n^+ diffusion)

a. Prime wafers in LP3 (HMDS application).
b. Spin OCG825 photoresist (MTI recipe #1).
c. Expose using Mask 1 (0.6 second exposure).
d. Develop in 3:1 DI water: OCG809 (WPS 3).
e. Inspect.

Approximate time required: I day.

(3) Oxide etch

a. Hard bake wafers for 30 minutes at 120 °C.
b. Determine etch rate of 6:1 buffered oxide etch (BOE) rate using 1000A thermal oxide test wafer.
c. Based on BOE etch rate and measured thickness calculate the required etch time. Etch wafers for this amount of time plus 20%, in addition to any time that may be required for wetting.
d. After DI water rinse inspect for hydrophobic surface behavior on large etched areas. Measure remaining oxide thickness on Nanospec to verify complete oxide removal.
e. Strip resist in piranha (WPS 5).

Approximate time required: 1 day.

(4) Phosphorus diffusion

a. Standard prediffusion clean with the addition of a dilute HF etch followed by a DI water rinse (need to remove native oxide before diffusion):
b. 50 minute $POCL_3$ doping with 20 minute anneal at 900 °C using Thermco recipe POCL3, tube 2-3.
c. Measure sheet resistance on monitor wafers.
d. Remove phosphorus-doped glass with dilute HF dip (determine etch time using monitor wafer).

Approximate time required: 1 day.

(5) Mask 2 (p^+ isolation)

a. Prime wafers in LP3 (HMDS application).
b. Spin OCG825 photoresist (MTI recipe #1).
c. Expose using Mask 2 (0.6 second exposure).
d. Develop in 3:1 DI water: OCG809 (WPS 3).
e. Inspect.

Approximate time required: 1 day.

(6) Oxide etch

a. Hard bake wafers for 30 minutes at 120 °C.
b. Determine etch rate of 6:1 buffered oxide etch (BOE) rate using 1000A thermal oxide test wafer.
c. Based on BOE etch rate and measured thickness calculate the required etch time. Etch wafers for this amount of time plus 20%, in addition to any time that may be required for wetting.
d. After DI water rinse inspect for hydrophobic surface behavior on large etched areas. Measure remaining oxide thickness on Nanospec to verify complete oxide removal.
e. Strip resist in piranha (WPS 5).

Approximate time required: 1 day.

(7) Mask 3 (p^+ isolation implant)

a. Prime wafers in LP3 (HMDS application).
b. Spin OCG825 photoresist (MTI recipe #1).
c. Expose using Mask 3 (0.6 second exposure).
d. Develop in 3:1 DI water: OCG809 (WPS 3).
e. Inspect.
f. Hard bake wafers for 30 minutes at 120G.

Approximate time required: 1 day.

(8) Isolation implant

a. Ion implant B^+ using photoresist mask (for high dose implants either the beam current must be limited or the wafers must be implanted in hybrid mode). Vendor: IICO.
b. Remove implanted resist in 0_2 plasma (campus), 7 minutes at 300W, 300 mTorr.

Approximate time required: 3-4 days.

(9) 5000A low-temperature oxide deposition/densification

a. Standard prediffusion clean.
b. LPCVD of SiO_2, 30 minute deposition at 425 °C using Thermco recipe UDLTO.
c. Anneal for 30 minutes in N_2 at 900 °C using Thermco recipe PRANNEAL, tube 1-1, with TCA clean of furnace tube prior to oxidation using Thermco recipe 1TCACLN. Wafers should be transferred directly from the LPCVD tube to the anneal tube with no clean in between.
d. Measure oxide thickness on monitor wafers. Keep monitor wafers for subsequent BOE etch rate calibration.

Approximate time required: I day.

(10) Backside n^+ removal

a. Prime wafers in LP3 (HMDS application).
b. Spin OCG825 photoresist (MTI recipe #1).
c. Hard bake wafers for 30 minutes at 120 °C.
d. Etch off backside oxide in 6:1 BOE.
e. Strip resist in piranha (WPS 5).
f. Prime wafers in LP3 (HMDS application).
g. Spin OCG825 photoresist (MTI recipe #1).
h. Hard bake wafers for 30 minutes at 120 °C.
i. Etch off backside n^+ in the silicon etch, monitoring progress with 4-point probe measurements of backside sheet resistance.
j. Strip resist in piranha (WPS 5).

Approximate time required: 2 days.

(11) 5000A backside, undoped polysilicon deposition

a. Standard prediffusion clean.
b. LPCVD of undoped polysilicon on wafer backside, 81 minute deposition at 620 °C using Thermco recipe POLY5K. Include low-temperature oxide monitor wafers.

Approximate time required: 1 day.

(12) Backside p^+ polysilicon doping

a. Standard prediffusion clean.
b. Boron predeposition at 900 °C for 1 hour (campus). Include low-temperature oxide monitor wafers.
c. Plasma etch frontside polysilicon (campus).
d. Measure sheet resistance on monitor wafers.

Approximate time required: 1 day.

(13) Anneal

a. Standard prediffusion clean.
b. Anneal using Thermco recipe WPLX900C (10 minute steam, 1 hour N_2 anneal, both at 900 °C). Include low-temperature oxide monitor wafers.
c. Measure oxide thickness on monitor wafers.

Approximate time required: 1 day.

(14) Mask 4 (contact mask)

a. Prime wafers in LP3 (HMDS application).
b. Spin OCG825 photoresist (MTI recipe #1).
c. Expose using Mask 4 (0.6 second exposure).
d. Develop in 3:1 DI water:OCG8O9 (WPS 3).
e. Inspect.

Approximate time required: 1 day.

(15) Contact etch

a. Hard bake wafers for 30 minutes at 120 °C.
b. Determine etch rate of 6:1 buffered oxide etch (BOE) rate using low-temperature oxide monitor wafers.
c. Based on BOE etch rate and measured thickness calculate the required etch time. Etch wafers for this amount of time plus 20%, in addition to any time that may be required for wetting.
d. After DI water rinse inspect for hydrophobic surface behavior on large etched areas. Measure remaining oxide thickness on Nanospec to verify complete oxide removal.
e. Strip resist in piranha (WPS 5).

Approximate time required: 1 day.

(16) 0.5 μm aluminum deposition

a. Determine etch rate of dilute HF bath.
b. Based on etch rate measurement, etch to remove 60A of oxide.
c. Load wafers into MRC603.
d. Sputter aluminum at 6 kW, 15 cm/mm, 10 mTorr.

Approximate time required: 1 day.

(17) Mask 5 (metal mask)

a. Prime wafers in LP3 (HMDS application).
b. Spin OCG825 photoresist (MTI recipe #1).
c. Expose using Mask 5 (0.6 second exposure).
d. Develop in 3:1 DI water: OGG809 (WPS 3).
e. Inspect.

Approximate time required: 1 day.

(18) Metal etch

a. Hard bake wafers for 30 minutes at 120 °C.
b. Etch wafers in aluminum etchant at 30 °C.
c. Remove silicon residue in freckle etch (2 minutes).
e. Strip resist in oxygen plasma (campus).

Approximate time required: I day.

(19) 0.1μm backside aluminum deposition/sinter

a. Prime wafers in LP3 (HMDS application).
b: Spin OGG825 photoresist (MTI recipe #1).
c. Hard bake wafers for 30 minutes at 120 °C.
d. Short BOE etch to remove backside oxide.
c. Load wafers into MRC603.
d. Sputter aluminum at 1 kW, 15 cm/min, 10 mTorr.
e. Strip resist in oxygen plasma (campus).
f. Sinter at 400 °C in forming gas using Thermco recipe SINT400, tube 1-2.

Approximate time required: 1 day.

Comments/Random thoughts

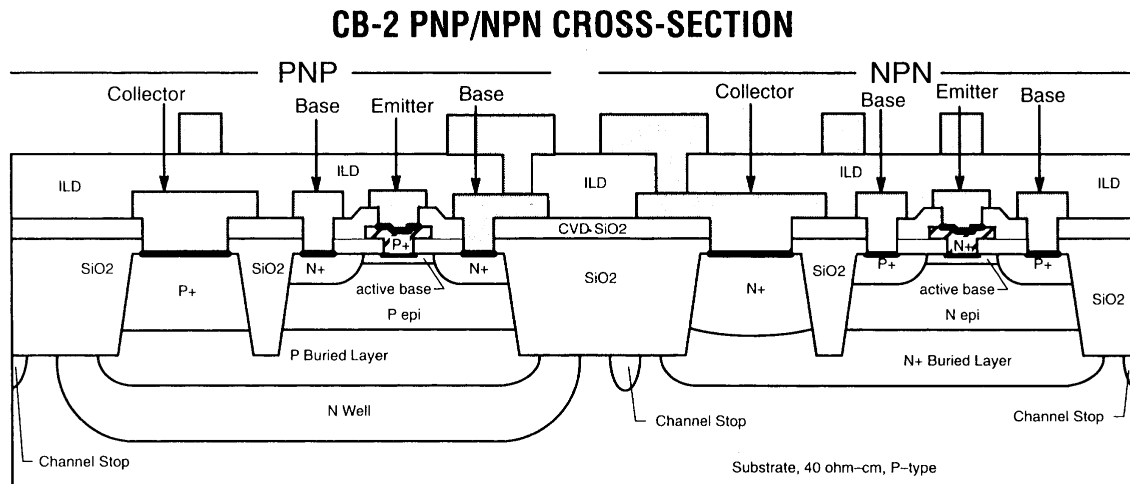
The total processing time at this pace is 22-23 days (about 4.5 weeks). The actual time required for the first run was 20 days. In this run the beginning lot size was 25 wafers, including 6 n-type. A total of 4 p-type wafers and all 6 n-type wafers have been completed. Processing on ten wafers was stopped just before the backside p^+ doping step (I did not want to risk all the wafers given that we had never tried removing a backside, doped layer before), and five were held back at the isolation implant step.
The rate limiting step is lithography. The Thermco furnaces can achieve good uniformity over a 50 wafer load and we should take advantage of this capability, although the standard lot size for lithography and etching would be 25 wafers. Several steps were performed on campus, including p^+ doping, oxygen plasma removal of resist, and plasma etching of frontside polysilicon. The doping process could be done at LBL with the addition of boron source wafers to tube 1-1. We will have an oxygen plasma system in hand soon, but we would still have to go to campus to remove the polysilicon off the wafer frontside.

There may be some yield concerns regarding doping of the backside polysilicon with solid source wafers rather than ion implantation. The original LBL detector process used solid source doping for the contact but we found that this resulted in poor yield on large area strip detectors (our work with Micron several years ago). Doping through a polysilicon layer may clean up the contaminants coming from the solid source doping. Ion implantation would be preferred, but we would have to work with IICO to develop a wafer holder that didn't result in damage to the front side of the wafer during the backside implant. Implanting the backside would add a couple of days to the total process time.

We may not want to go with such a thick deposited oxide (step 10). For this particular run it was included to reduce the line capacitance for the detectors containing bump pads with traces to wire bond pads. This oxide is over the p^+ isolation region and hence a relatively thin oxide would be desired for radiation hardening purposes. However, this oxide must act as a barrier for the p^+ diffusion, and must also be a reliable etch stop for the frontside polysilicon etching. Apparently a BPSG oxide can be made radiation hard, and this might be a potential candidate for the oxide over n^+/p^+.

A detector is a rather simple device.

The complexity of an integrated circuit is much greater, with a correspondingly larger number of masks and processing steps.



(Maxim Integrated Products)

Modern IC processes typically require 15 to 18 masks, with more complicated processes using 24 or more.

Although it is possible to perform “microsurgery” in some situations, in general this technology is very unforgiving.

Once a circuit is “cast in silicon” and it doesn’t function, no tweaking or “cut and try” can change it.

Extreme care is required in

- the design of the devices and process
- the design of the circuit
    - Are models used for simulation reliable?
    - Does the circuit provide latitude for process variations?
    - “hooks” for external adjustments?
- conducting the fabrication process
- evaluation of prototypes

LBNL Microsystems Laboratory

Modern fabrication facility for specialized silicon devices.
Operated by Physics Division.

Ultra-clean facility with process capabilities not available in conventional detector laboratories

- class 1 clean room
- wide range of deposition processes
- sub-micron lithography
- water system with sub-ppb impurity levels

Emphasis on

- test of device concepts and technology beyond industrial mainstream
- rapid turn-around

Although primary emphasis on R&D and proof-of-principle, limited production runs (~1 - 3 m^2) feasible.

Complementary to campus microfabrication facility (Cory Hall)

Current Topics

Fully depleted CCDs for faint light imaging
Photodiode arrays for medical imaging
Test structures for device R&D

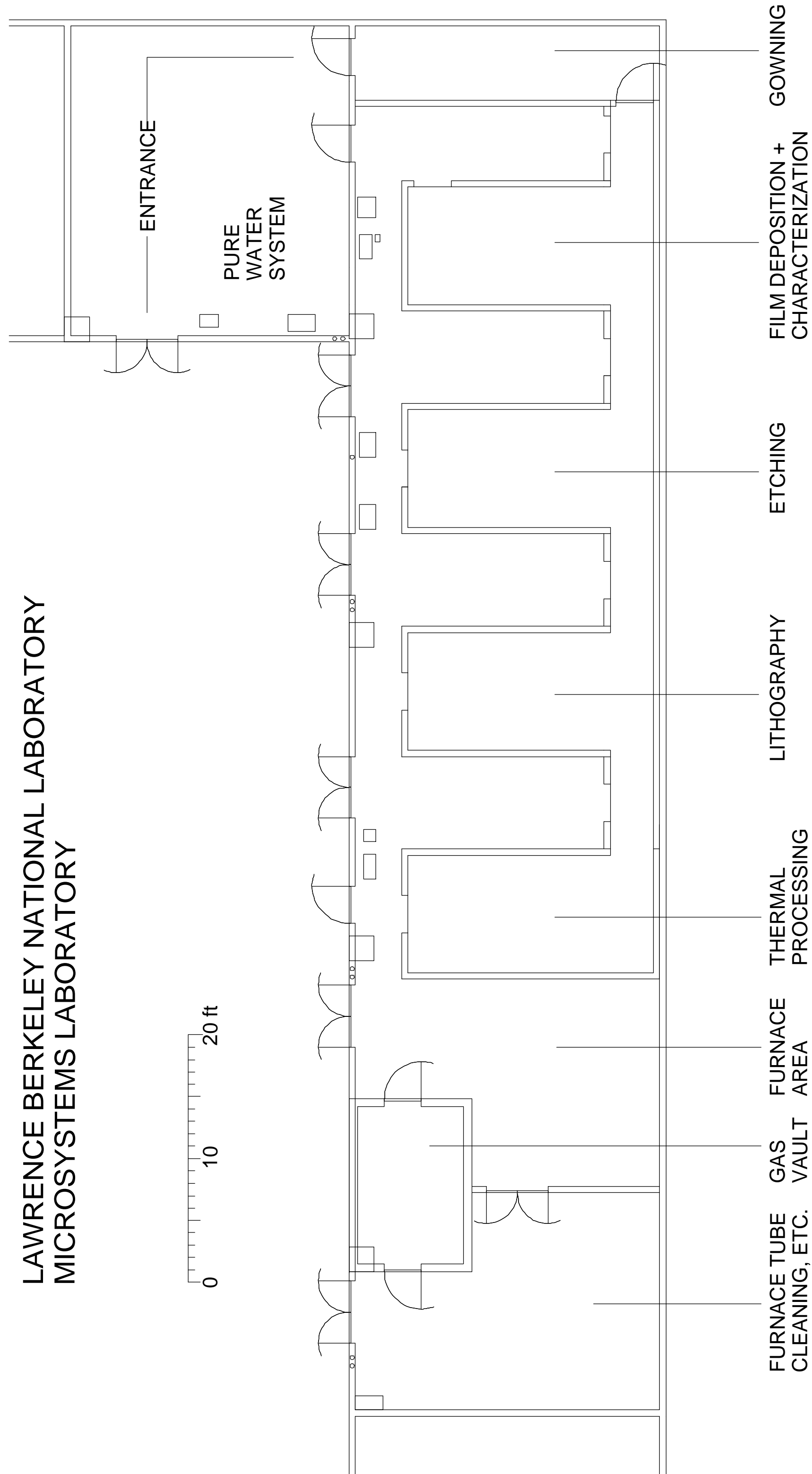
Laboratory Facilities

- ~700 ft^2 of class 1 - 10 fabrication area
- Floor plan chosen to allow maintenance with minimal disruption of clean room activities
- Tight temperature (±1C) and humidity (±2%) control
- Dedicated high-purity water system

Process equipment includes

- Semi-automated wet process stations for wafer cleaning and etching
- Sub-micron lithography
  GCA wafer stepper with programmable apertures
  MTI wafer track for highly uniform photoresist deposition
- Thermal processing
  - 5 atmospheric furnace tubes
    - for oxidation, doping by diffusion, drive-in of ion implants, sintering, and annealing
  - 3 low-pressure furnace tubes
    - for a variety of film depositions, *e.g.*
      - doped and undoped polysilicon
        (for detector bias resistors, MOSFETs)
      - Si nitride
      - High-temperature oxide
        (for combined oxide-nitride films, *e.g.* for detector blocking capacitors)
      - Low-temperature oxide
        (thick passivation layers)

  Furnaces are computer-controlled with extensive safety systems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