VIII. Detector Systems – Conflicts and Compromises

Conflicts

Custom integrated circuits essential for vertex detectors in HEP.

Requirements

1. low mass to reduce scattering
2. low noise
3. fast response
4. low power
5. radiation tolerance

reduction in mass $\Rightarrow$ thin detector

radiation tolerance $\Rightarrow$ thin detector

thin detector $\Rightarrow$ less signal
$\Rightarrow$ lower noise required

lower noise $\Rightarrow$ increased power

fast response $\Rightarrow$ increased power

increased power $\Rightarrow$ more mass in cabling
+ cooling

immunity to external pickup
$\Rightarrow$ shielding
$\Rightarrow$ mass

+ contain costs

How to deal with these conflicting requirements?

Example: Silicon Detectors at the LHC

LHC Parameters:

Colliding proton beams

7 TeV on 7 TeV (14 TeV center of mass)

Luminosity: 10^{34} $cm^{-2}s^{-1}$

Bunch crossing frequency: 40 MHz

Interactions per bunch crossing: 23

Charged particles per unit of rapidity: 150

$\Rightarrow$ hit rate $n' = \frac{2 \cdot 10^9}{r_\perp^2} \left[\mathrm{cm^{-2}s^{-1}} \right]$, where $r_\perp$ = distance from beam axis

If the detector subtends ± 2.5 units of rapidity,
the total hit rate in the detector is $3 \cdot 10^{10}$ s^{-1}

Hit rate at $r_\perp = 14$ cm: ~ 10^7 $cm^{-2}s^{-1}$

Overall detector to include

1. Vertexing for B-tagging
2. Precision tracking in magnetic field
3. Calorimetry (EM + hadronic)
4. Muon detection

The LHC luminosity upgrade also doubles the time between pulses from 25 to 50 ns, which increases the rate per collision $\Rightarrow$ pile-up problems at increased luminosity

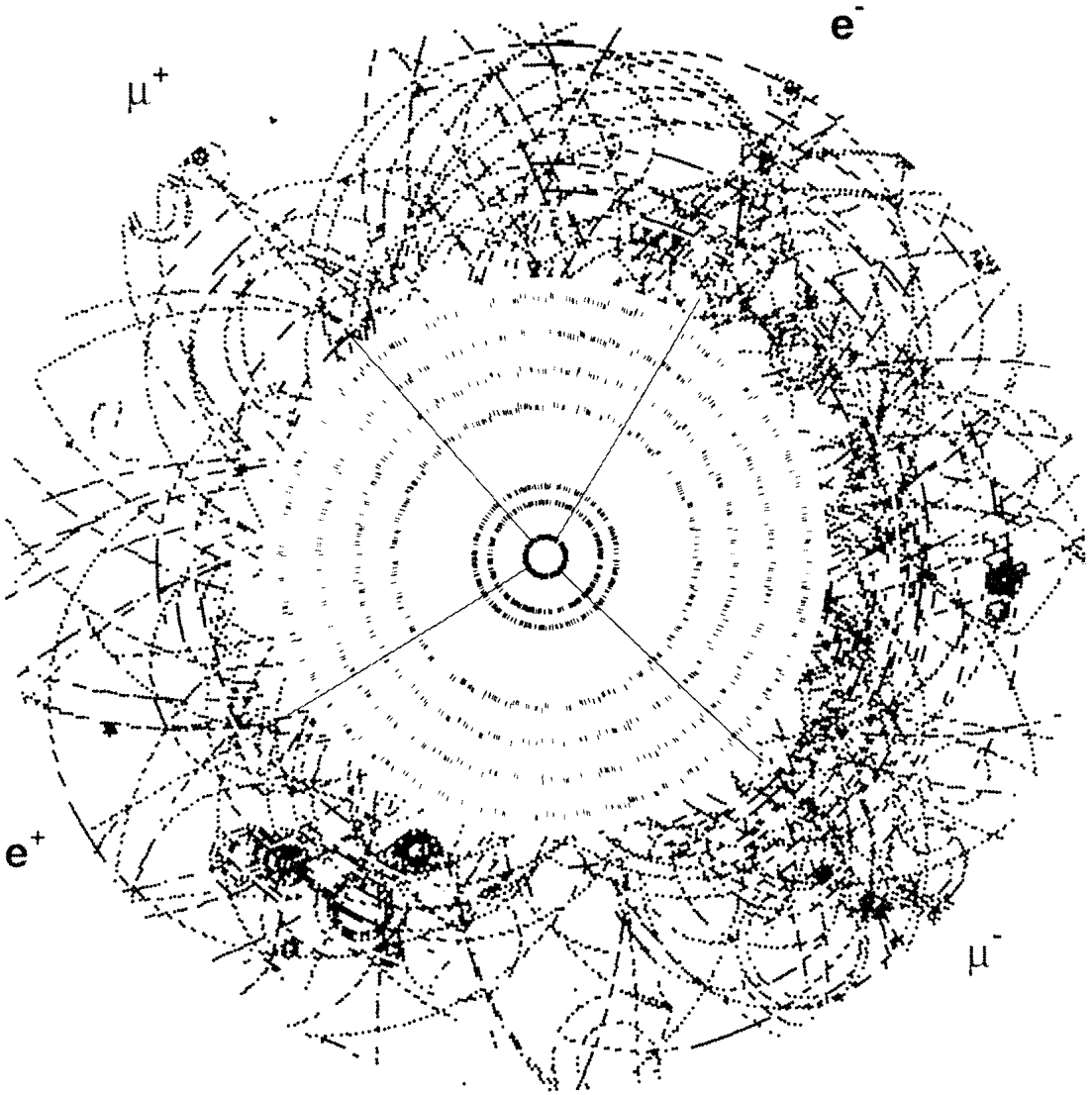
"Typical Event" – Axial View

$H \rightarrow ZZ^* \rightarrow \mu^+\mu^-e^+e^-$

(m_H= 130 GeV)

Appears worse than it is

– tracks spread azimuthally, but high track density at forward angles.



Radiation Damage

Two sources of particles

a) Beam collisions

b) Neutron albedo from calorimeter

Fluences per year (equivalent 1 MeV neutrons)

r ~ 10 cm typ. $5 \cdot 10^{13}$ cm^{-2}

r ~ 30 cm typ. $2 \cdot 10^{13}$ cm^{-2}

Ionizing Dose per year

r ~ 10 cm 30 kGy (3 Mrad)

r ~ 30 cm 4 kGy (400 krad)

In reality, complex maps are required of the radiation flux,
which is dependent on local material distribution.

How to cope with ...

- High total event rate

  a) Fast electronics

  High power required for both noise and speed

  b) Segmentation

  Reduce rate per detector element

  For example, at r= 30 cm the hit rate in an area of $5 \cdot 10^{-2}$ cm^2 is about 10^5 s^{-1}, corresponding to an average time between hits of 10 μs.

  $\Rightarrow$ Longer shaping time allowable

  $\Rightarrow$ Lower power for given noise level

- Large number of events per crossing

  a) Fast electronics (high power)

  b) Segmentation

  If a detector element is sufficiently small, the probability of two tracks passing through is negligible.

  c) Single-bunch timing

  Reduce confusion by assigning hits to specific crossing times

$\Rightarrow$ Segmentation is an efficient tool to cope with high rates.

With careful design, power requirements don't increase.

⇒ Fine segmentation feasible with semiconductor detectors

- "μm-scale" patterning of detectors
- Monolithically integrated electronics mounted locally

Large number of front-end channels requires simple circuitry

Single bunch timing ⇒ collection times <25 ns

Radiation damage is a critical problem in semiconductor detectors:

a) Detector leakage current $I_R = I_{R0} + \alpha \Phi A d$

⇒ Shot noise $Q_{ni}^2 = 2 q_e I_R F_i T_S$

⇒ Self-heating of detector $I_R(T) \propto T^2 e^{-E/2k_B T}$

Reduce current by cooling

Reduce shaping time

Reduce area of detector element

b) Increase in depletion voltage

(buildup of acceptor-like states ⇒ negative space charge)

⇒ Thin detector

⇒ Allow for operation below full depletion

⇒ Less signal

Requires lower noise to maintain minimum S/N

⇒ Decrease area of detector element (capacitance)

Use of a highly-developed technology, i.e. Si rather than “exotic” materials, provides performance reserves and design flexibility to cope with radiation damage.

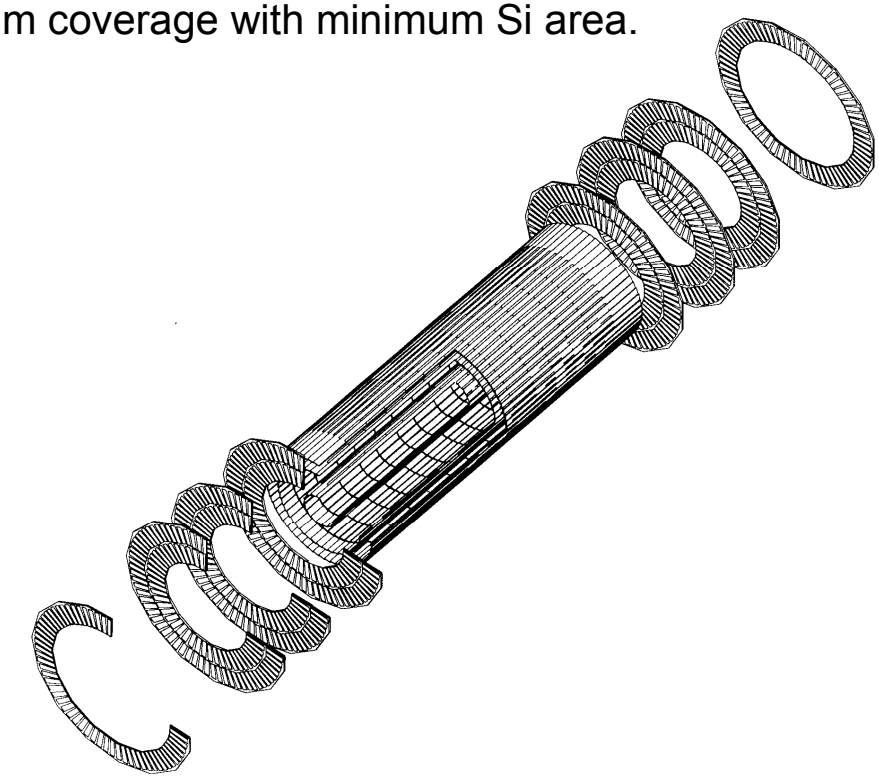
Layout

Full coverage is provided by a combination of barrel and disk layers.

Coverage provided by a) barrel in central region

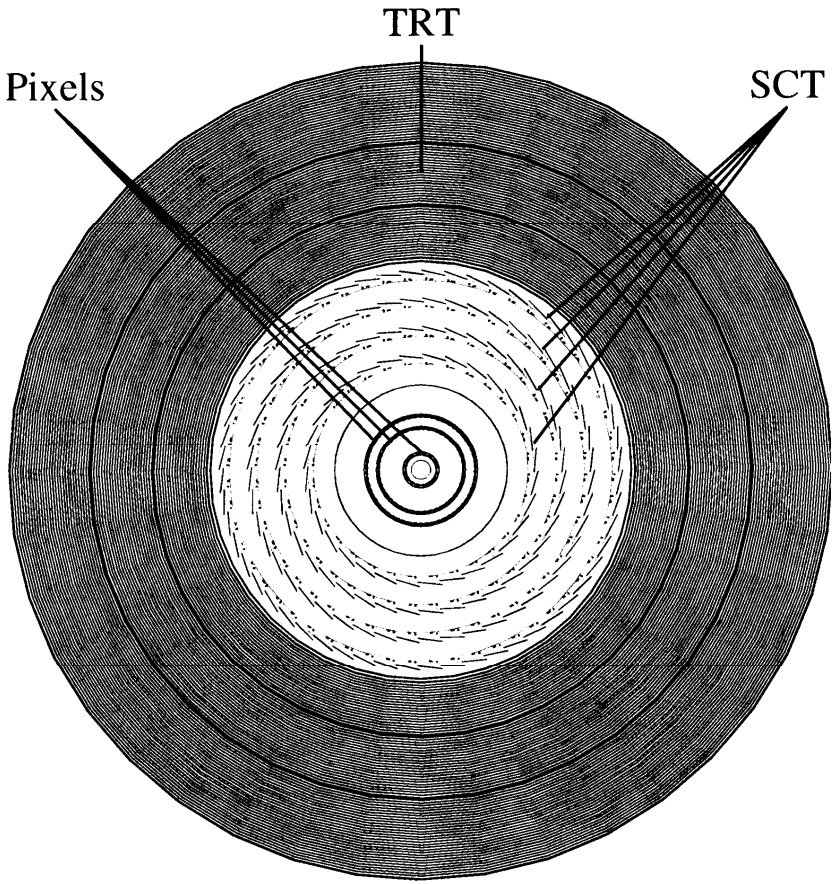
b) disks in forward regions

to provide maximum coverage with minimum Si area.



Pixels at small radii (4, 11, 14 cm) to cope with

- High event rate
  (2D non-projective structure)
- Radiation damage
  small capacitance ~ 100 fF
  $\Rightarrow$ low noise $Q_n \approx 200\ e$



Strips at larger radii (30, 37, 45, 52 cm) minimize material, cost

Pixels and strips provide primary pattern recognition capability

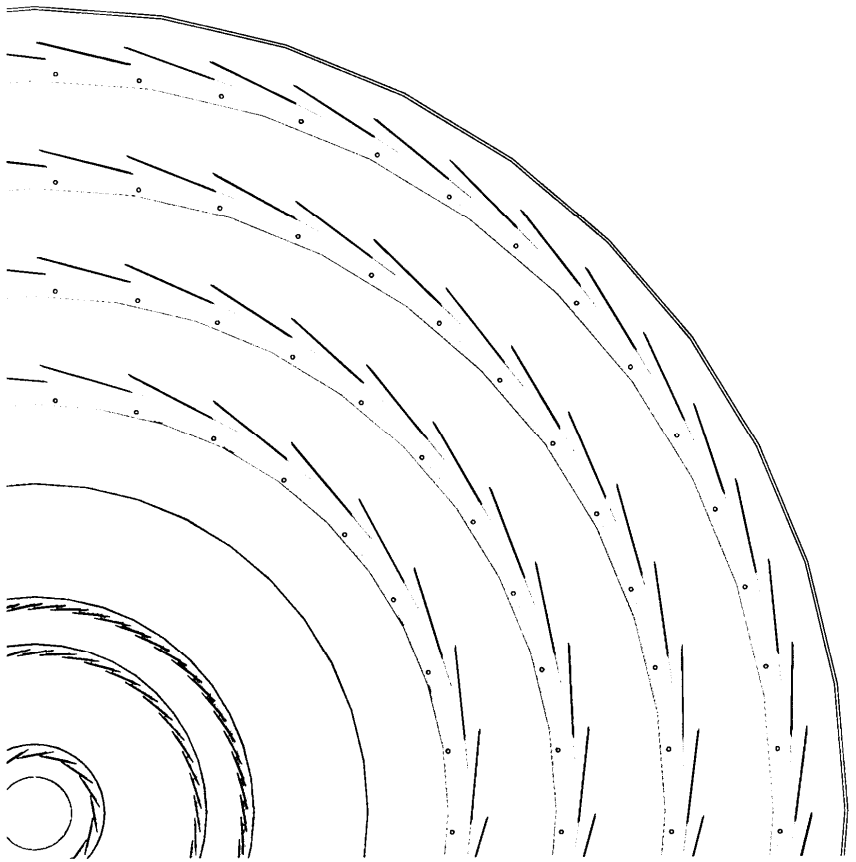
ATLAS uses straw drift chambers at outer radius (56 – 107 cm)

~70 layers yield 40 space points at large r and augment pattern recognition by continuous tracking (least expensive solution)

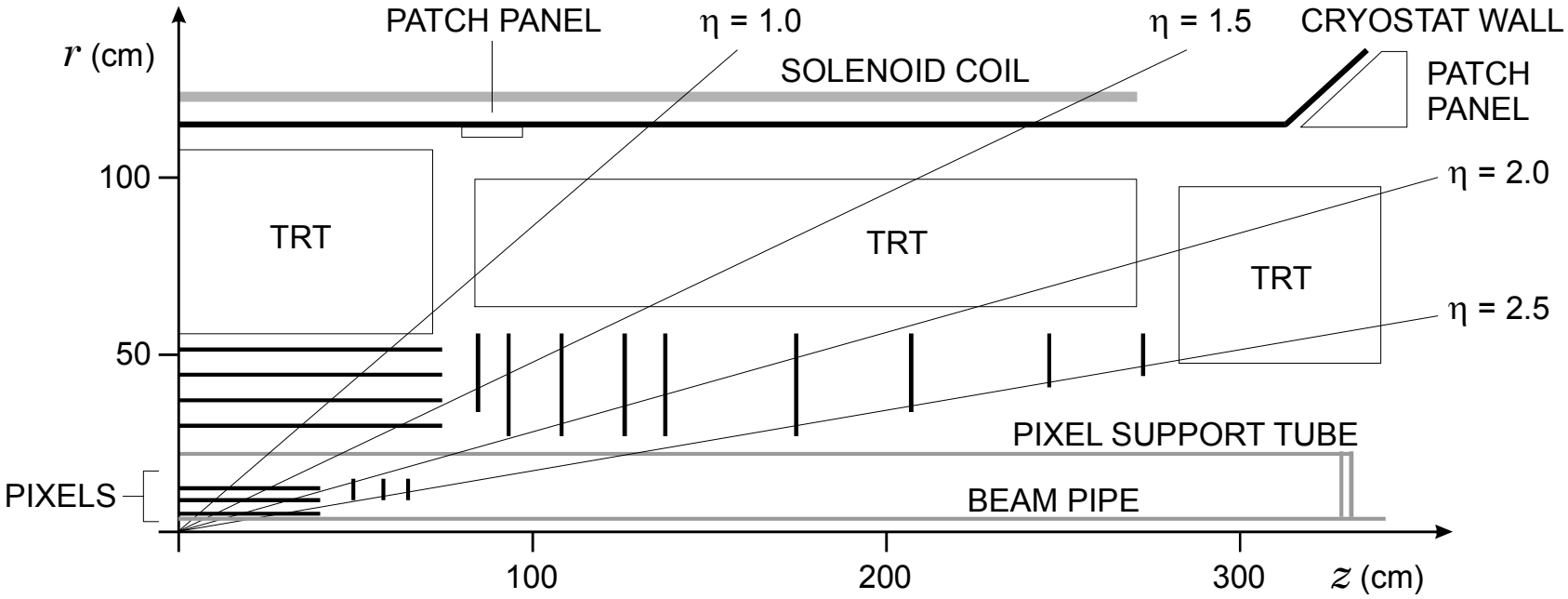
CMS uses all-silicon tracker
(210 m^2 of Si with ~10^7 channels)

Detector modules are arranged in cylindrical shells (barrels).

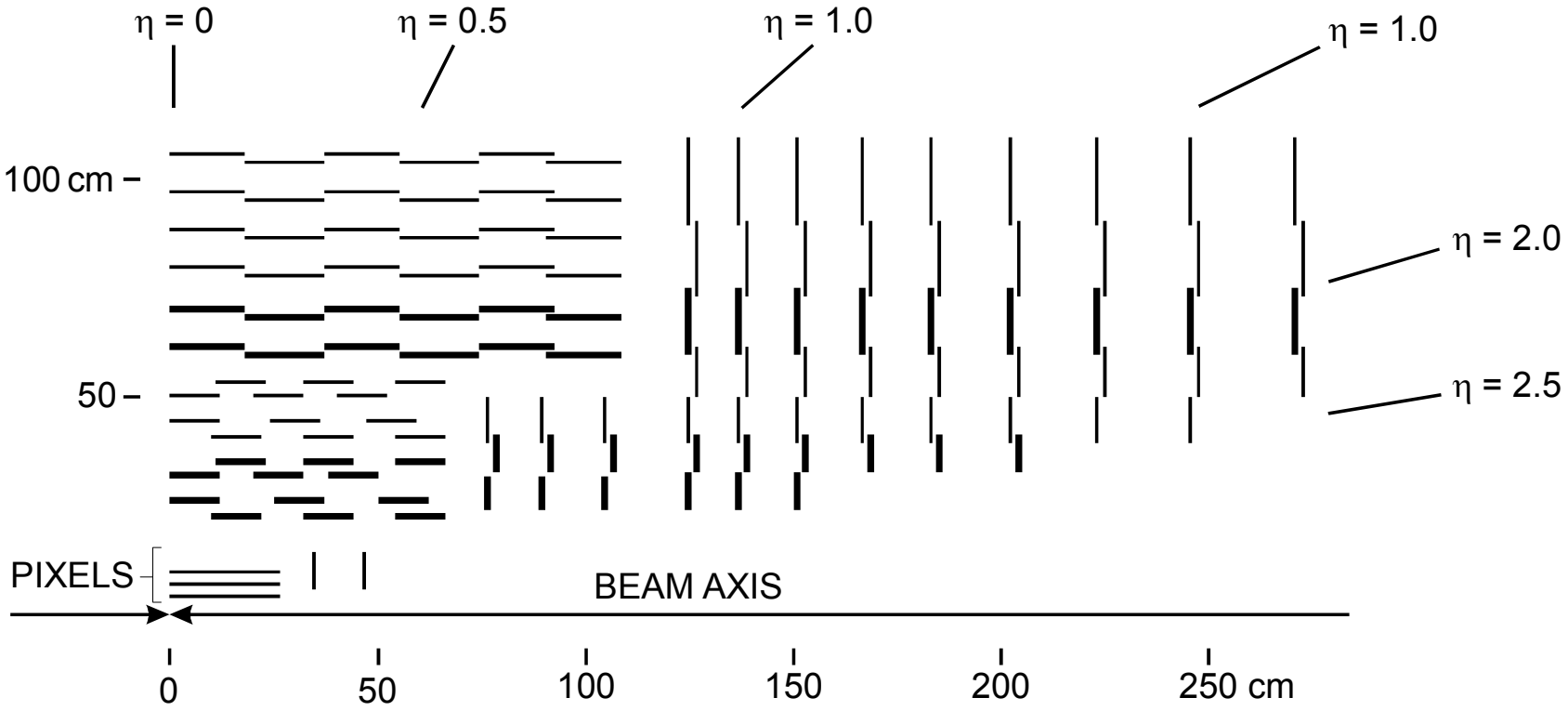
Modules are “shingled” to provide full coverage and overlap to facilitate relative position calibration.



ATLAS Silicon Tracker Layout (strips + pixels)



CMS Tracker Layout



Thick lines denote double-sided modules (back-to-back single-sided detectors).

Segmentation ⇒ Large number of data channels

Total number of channels and area (ATLAS):			
	Pixels	1.4×10^8 channels	2.3 m^2
	Strips	6.2×10^6 channels	61 m^2
	Straws	4.2×10^5 channels	

But, only a small fraction of these channels are struck in a given crossing

Occupancy for pixels, 50 μm x 300 μm:		
	4 cm Pixel Layer	4.4×10^{-4}
	11 cm Pixel Layer	0.6×10^{-4}

Occupancy for strip electrodes with 80 μm pitch, 12 cm length:

30 cm Strip Layer	6.1×10^{-3}
52 cm Strip Layer	3.4×10^{-3}

Utilize local sparsification – i.e. on-chip circuitry that recognizes the presence of a hit and only reads out those channels that are struck.

⇒ data readout rate depends on hit rate, not on segmentation

First implemented in SVX chip

S.A. Kleinfelder, W.C. Carrithers, R.P. Ely, C. Haber, F. Kirsten, and H.G. Spieler, A Flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout, IEEE Trans. Nucl. Sci. **NS-35** (1988) 171

(actually built years earlier than published)

Readout

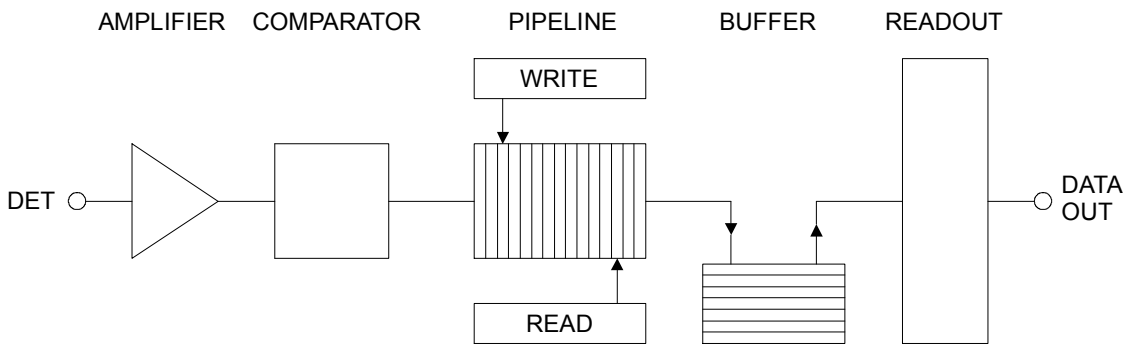
Strips + Pixels: many channels

Essential to minimize
- power
- material (chip size, power cables, readout lines)
- cost (chip size)
- failure rate (use simple, well controlled circuitry)

ATLAS criterion is to obtain adequate position resolution, rather than the best possible

⇒ Binary Readout
- detect only presence of hits
- identify beam crossing

Architecture of ATLAS strip readout



Unlike LEP detectors …

Crossing frequency >> readout rate

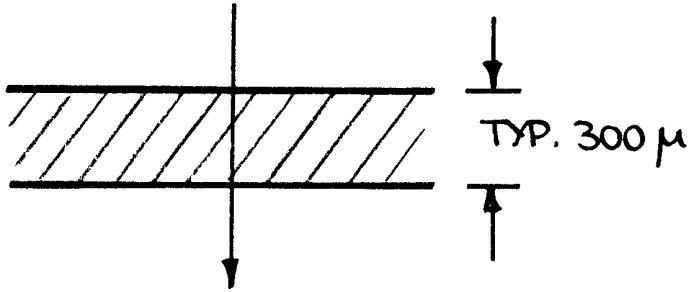
Data readout must proceed simultaneously with signal detection (equivalent to DC beam)

Single 128-channel BiCMOS chip (BJT + CMOS on same chip) in radiation-hard technology.

Required Signal-to-Noise Ratio

Acceptable noise level established by signal level and noise occupancy

1. Signal Level

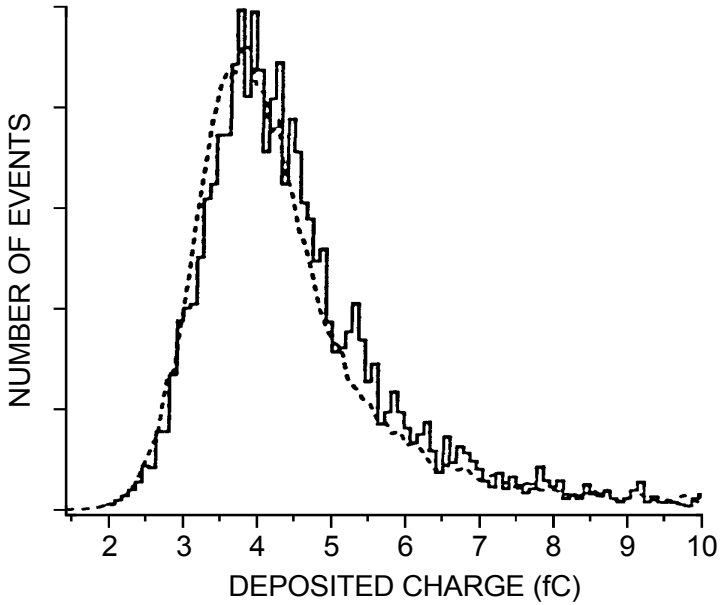


For minimum ionizing particles:
Q_s= 22000 *el* (3.5 fC)

Signals vary event-by-event according to Landau distribution

Measured Landau distribution in a 300 μm thick Si detector
(Wood et al., Univ. Oklahoma)

The Landau distribution peaks at the most probable energy loss Q_0 and extends down to about 0.5 Q_0 for 99% efficiency.



Assume that the minimum energy is $f_L Q_0$.

Tracks passing between two strips will deposit charge on both strips.

If the fraction of the signal to be detected is f_{sh}, the circuit must be sensitive signal as low as

$$Q_{\min} = f_{sh} f_L Q_0$$

2. Threshold Setting

It would be desirable to set the threshold much lower than Q_{min}, to be insensitive to threshold variations across the chip.

A lower limit is set by the need to suppress the noise rate to an acceptable level that still allows efficient pattern recognition.

As discussed in Part IV, the threshold-to-noise ratio required for a desired noise rate f_n in a system with shaping time T_S

$$\frac{Q_T}{Q_n} = \sqrt{-2\log(4\sqrt{3} f_n T_S)}$$

Expressed in terms of occupancy P_n in a time interval Δt $\quad \frac{Q_T}{Q_n} = \sqrt{-2\log\left(4\sqrt{3}_n T_S \frac{P_n}{\Delta t}\right)}$

In the strip system the average hit occupancy is about 5 x 10^{-3} in a time interval of 25 ns. If we allow an occupancy of 10^{-3} at a shaping time of 20 ns, this corresponds to

$$Q_T / Q_n = 3.2$$

The threshold uniformity is not perfect. The relevant measure is the threshold uniformity referred to the noise level. For a threshold variation ΔQ_T, the required threshold-to-noise ratio becomes

$$\frac{Q_T}{Q_n} = \sqrt{-2\log\left(4\sqrt{3}_n T_S \frac{P_n}{\Delta t}\right)} + \frac{\Delta Q_T}{Q_n}$$

If $\Delta Q_T / Q_n = 0.5$, the required threshold-to-noise ratio becomes $Q_T / Q_n = 3.7$.

To maintain good timing, the signal must be above threshold by at least Q_n, so $Q_T/Q_n > 4.7$.

Combining the conditions for the threshold

$$\left(\frac{Q_T}{Q_n}\right)_{min} Q_n \le Q_{min} \quad \text{and signal} \qquad Q_{min} = f_{sh} f_L Q_0$$

yields the required noise level $$Q_n \le \frac{f_{sh} f_L Q_0}{(Q_T / Q_n)_{\min}}$$

If charge sharing is negligible $f_{sh} = 1$, so with $f_L = 0.5$, $Q_0 = 3.5$ fC and $(Q_T/Q_n)_{\min} = 4.7$

$$Q_n \le 0.37 \text{ fC} \text{ or } Q_n \le 2300\, e$$

If the system is to operate with optimum position resolution, i.e. equal probability of 1- and 2-hit clusters, then $f_{sh} = 0.5$ and

$$Q_n \le 0.19 \text{ fC} \text{ or } Q_n \le 1150\, e$$

ATLAS requires $Q_n \le 1500\, e$.

Detector Structures I – ATLAS Strip Readout

ATLAS has adopted a single chip implementation (ABCD chip).

- 128 ch, bondable to 50 μm strip pitch
- Bipolar transistor technology, rad-hard
  $\Rightarrow$ minimum noise independent of shaping time
- Peaking time: ~20 ns (equivalent CR-RC^4)
- Double-pulse resolution (4 fC – 4 fC): 50 ns
- Noise, timing: following slides
- 1.3 to 1.8 mW/ch (current in input transistor adjustable)
- On-chip DACs to control threshold + operating point
- Trim DACs on each channel to reduce channel-to-channel gain and threshold non-uniformity
- Readout allows defective chips to be bypassed
- Optical fiber readout with redundancy
- Die size: 6.4 x 4.5 mm^2

For illustration, the following slides show data from a previous prototype IC, the CAFE chip.

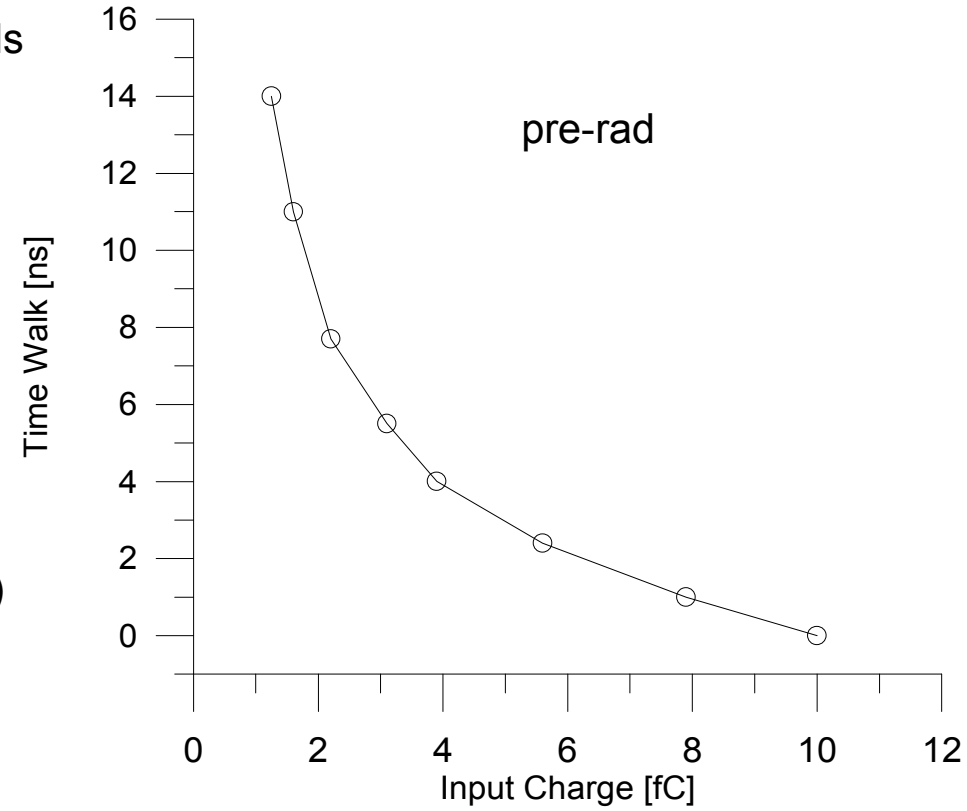
This was part of an initial 2-chip implementation (BJT analog chip and CMOS digital chip).

CAFE Timing Performance

Pre-rad chips measured on test boards

C_{load} = 15 pF, 1 fC threshold

Jitter at 1.25 fC ≈ 4 ns FWHM



Post-rad chips

- **irradiated to 10^{14} cm^{-2} (MIP equiv)**

Time Walk 16 ns (1.25 - 10 fC)
at 1 fC threshold

1.25 - 4 fC: 12 ns
4 fC - 10 fC: 4 ns

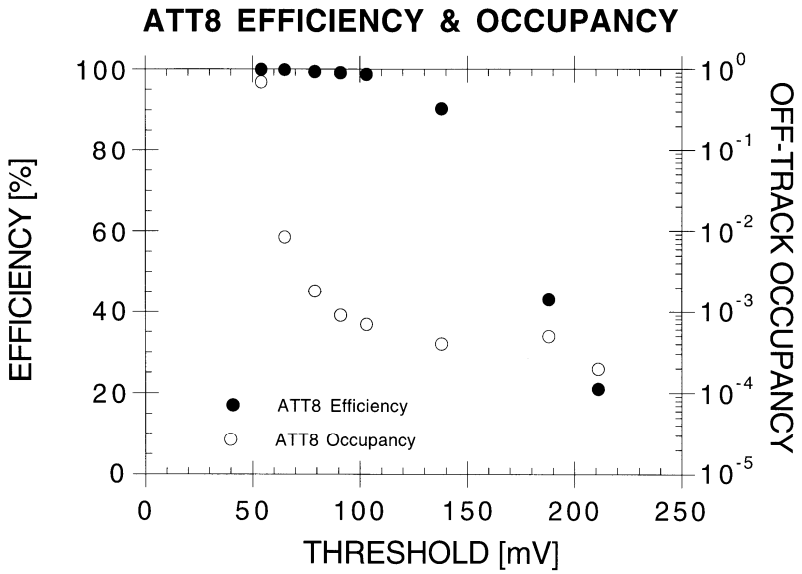
Jitter at 1.25 fC ≈ 4 ns FWHM, as above

Total time diistribution (99% efficiency) confined within about 18 ns.

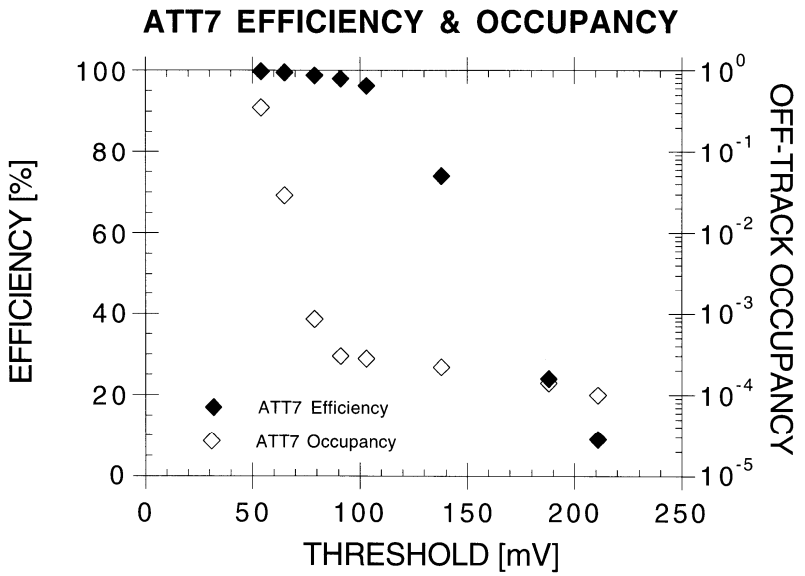
Test Beam Data

Tracking Efficiency vs. Occupancy for Full-Length Modules

non-irradiated module



irradiated module ($\Phi = 10^{14}$ cm^{-2})

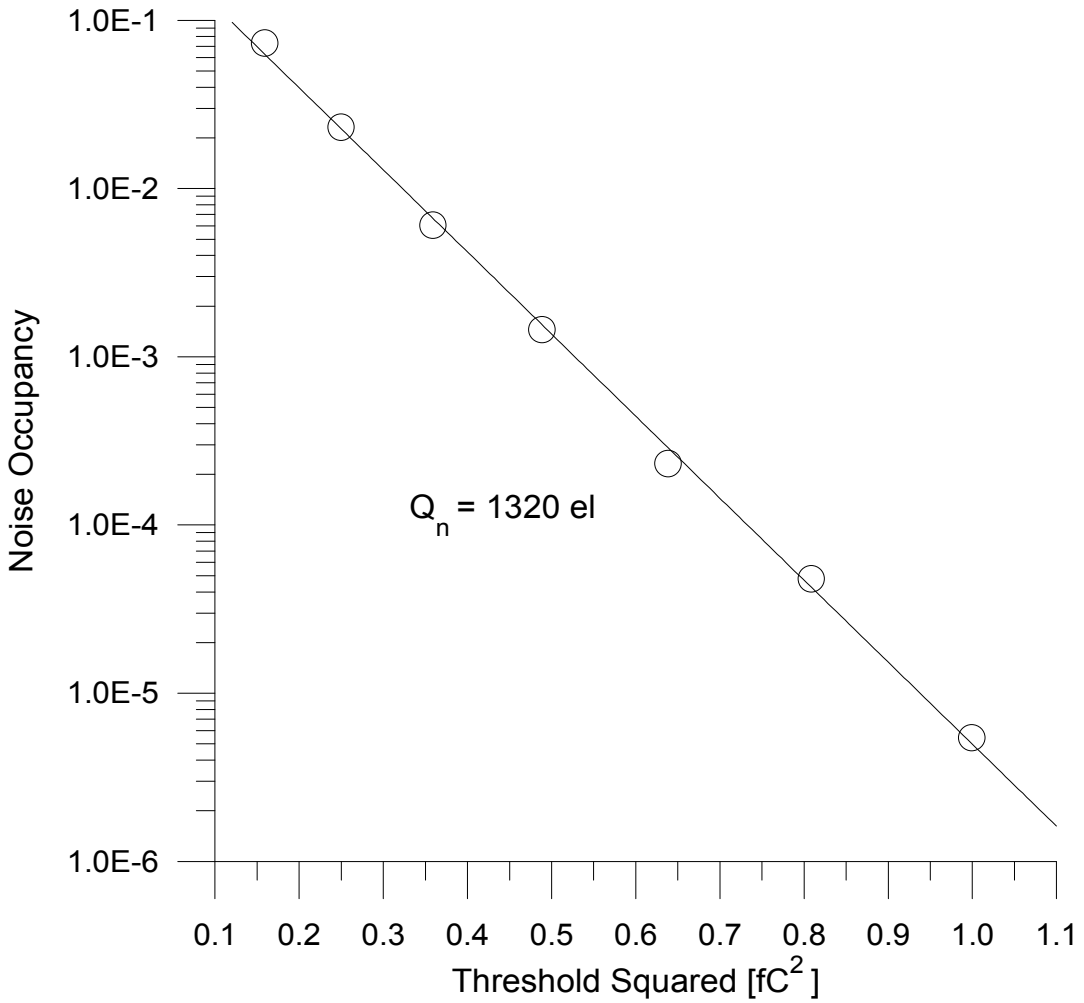


Noise Occupancy vs. Threshold

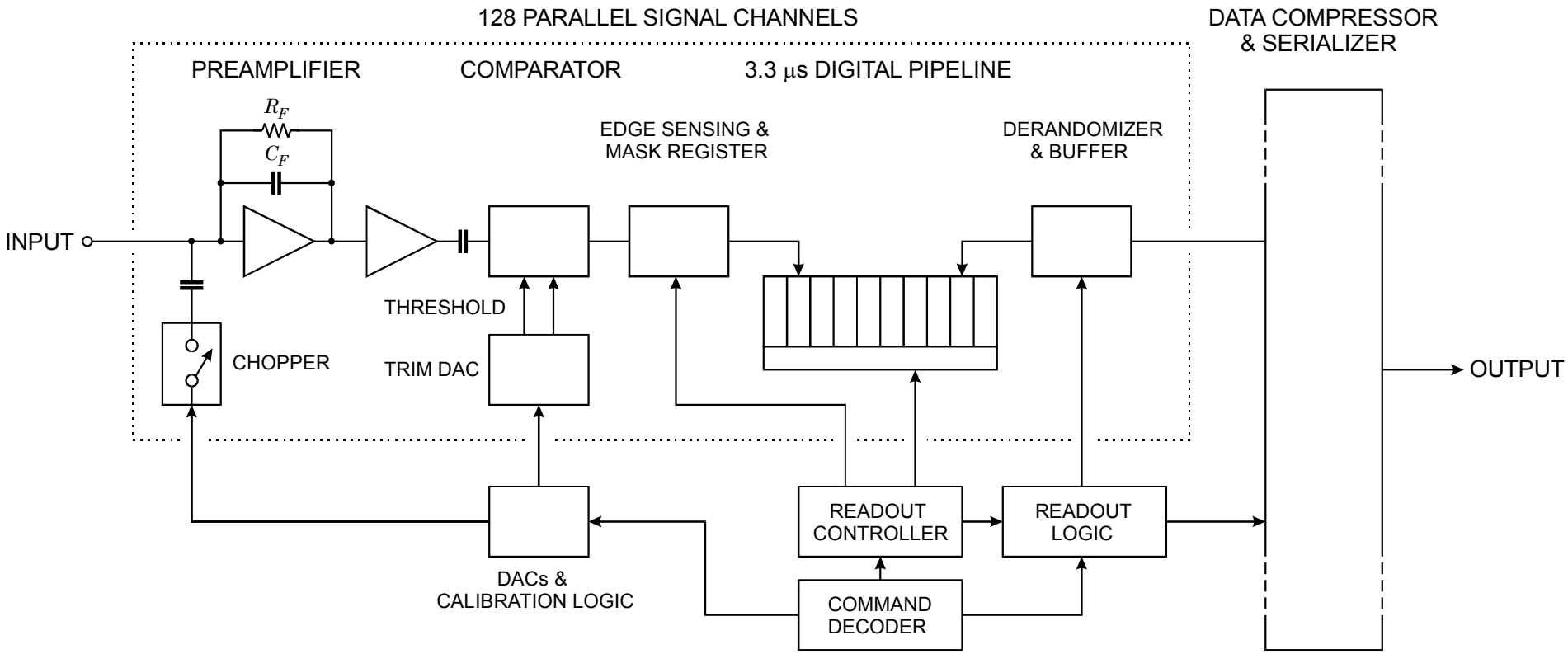
Module with CAFE chip in test beam position at KEK

Digital cross-talk is minimal:

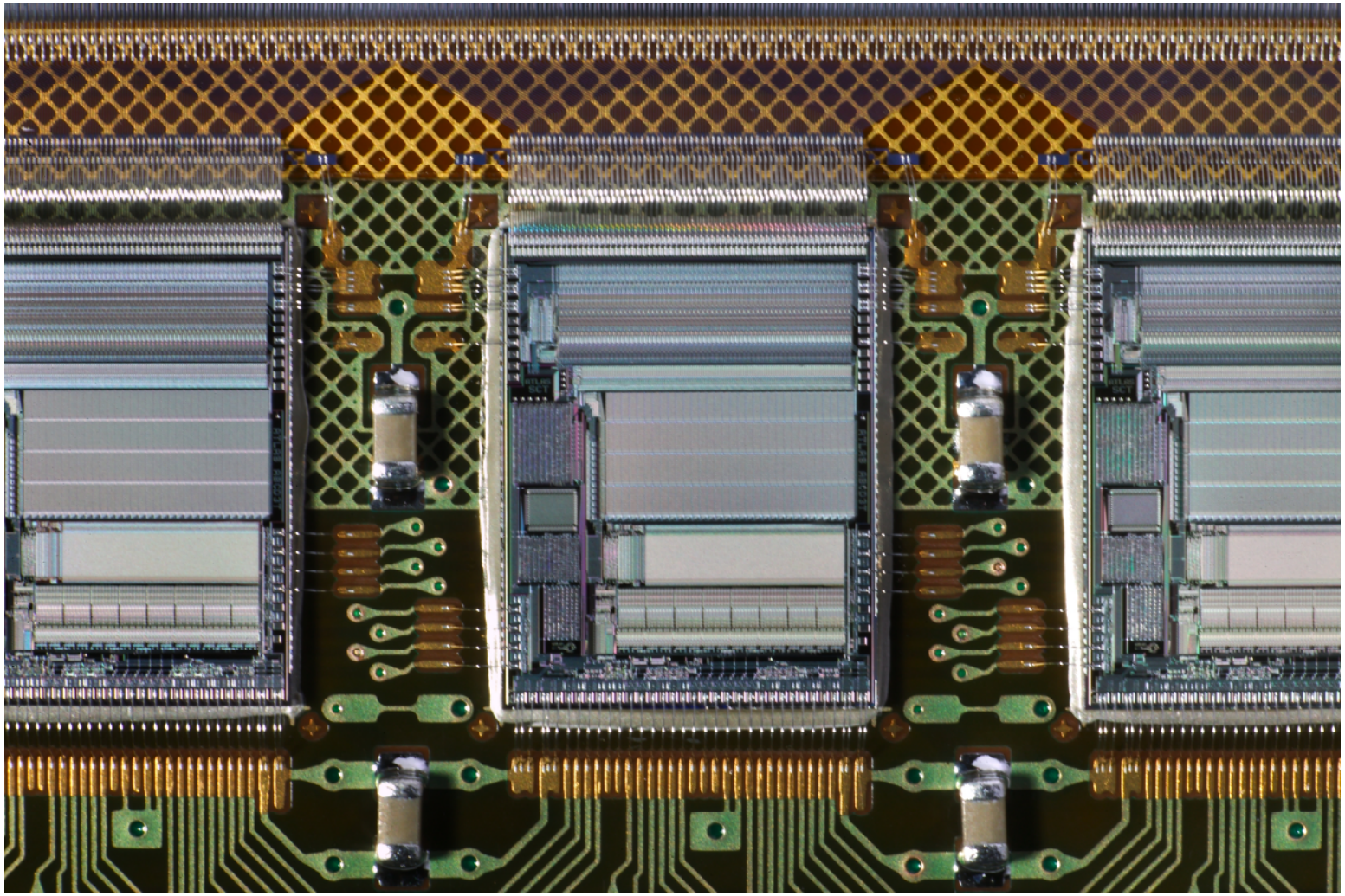
The straight line plot indicates Gaussian Noise



Block Diagram of ATLAS Strip Readout



ATLAS Silicon Strip system (SCT): ABCD chips – 128 channels each – mounted on hybrid



Note external bypass capacitors and space required for connections between ICs

ATLAS Silicon Strip Detector Module

Two 6 x 6 cm^2 single-sided Si strip detectors butted edge-to-edge to form
12 cm long detector

Two 6 x 12 cm^2 detectors glued back-to-back and rotated to one another by 40 mrad to form small-angle stereo

Six readout ICs – 128 channels each – mounted on each side.

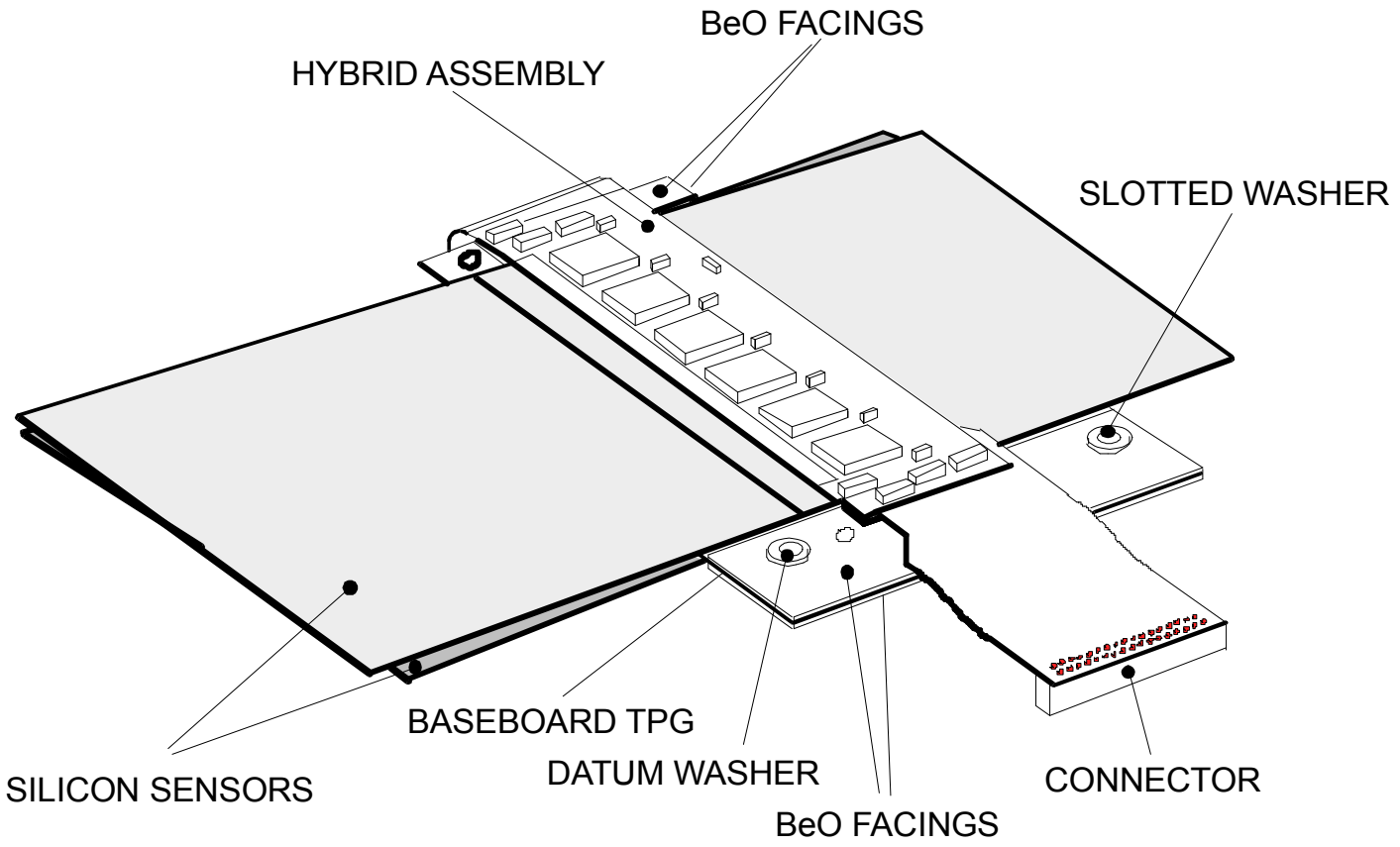
Strip pitch: 80 μm
Total no. of channels: 2 x 768

IC designed with ~50 mm pitch to provide space between ICs.

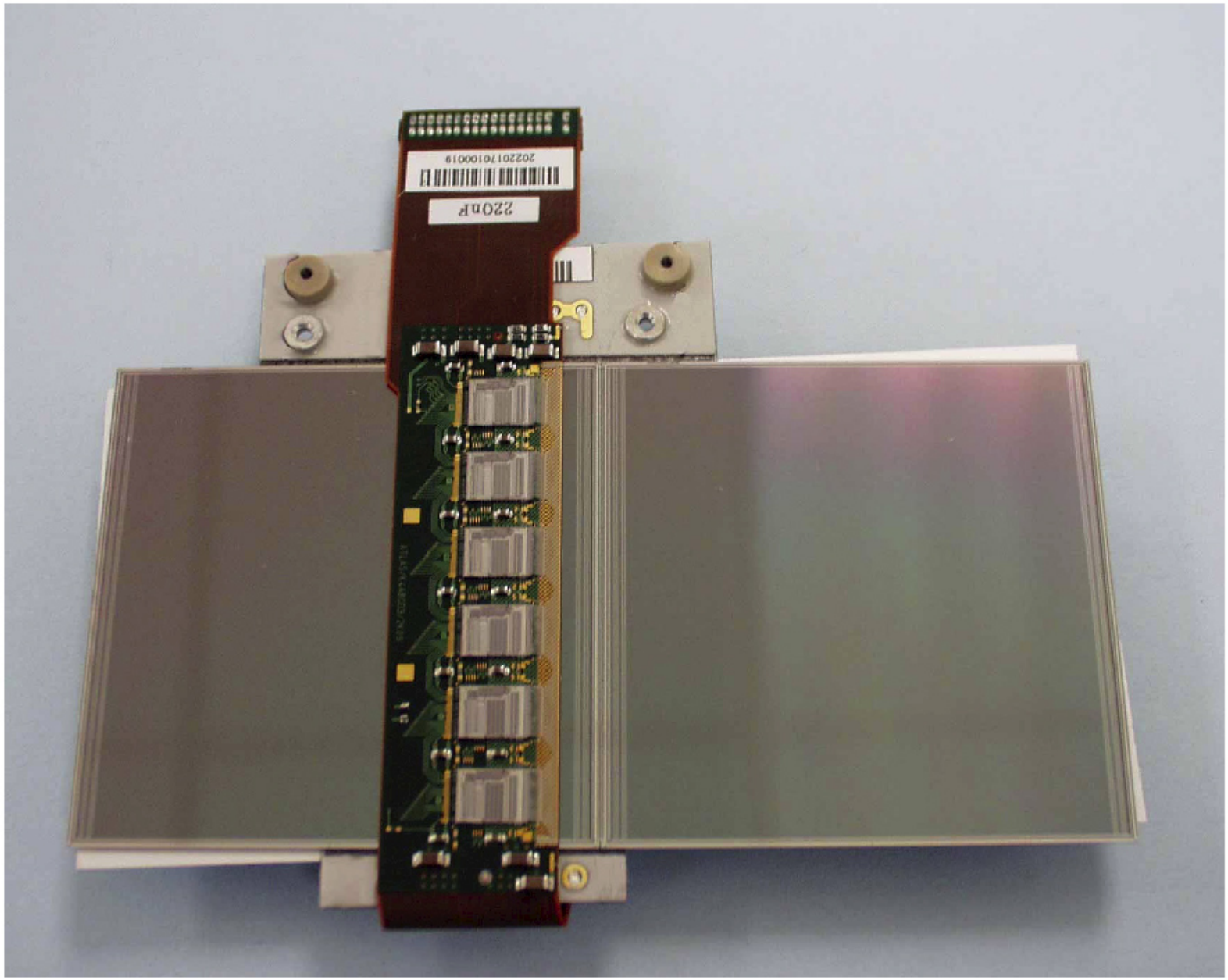
Binary readout with on-chip pipeline and readout sparsification

Kapton pigtail connects to local opto-module for clock, control, data transmission

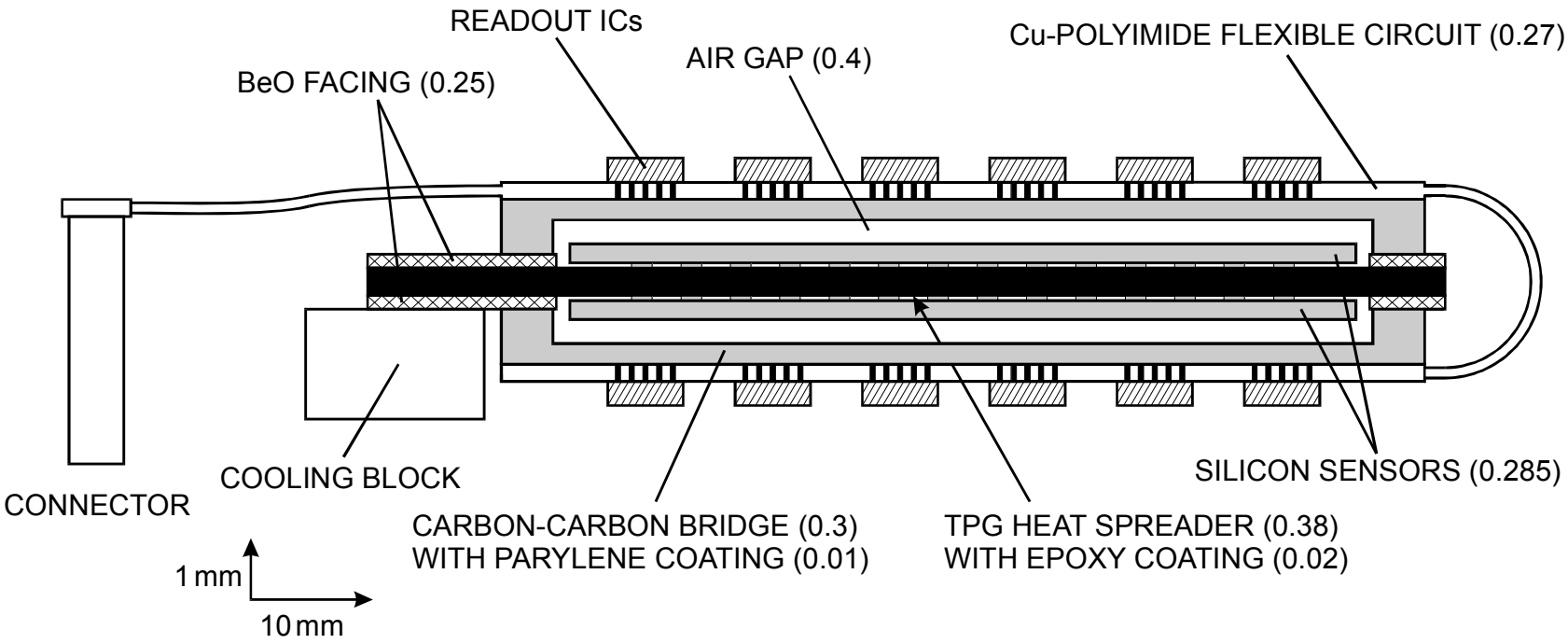
ATLAS SCT Detector Module



Readout ICs – 128 channels each – mounted on detectors and connected at middle (reduce thermal noise of strip electrode resistance).


220nF

Cross Section of Module



Readout ICs are mounted with a gap to avoid heating of the detector.

Thin field-fixing shielding (see Part IX) reduces cross-coupling of digital signals to the detector – no significant cross-talk.

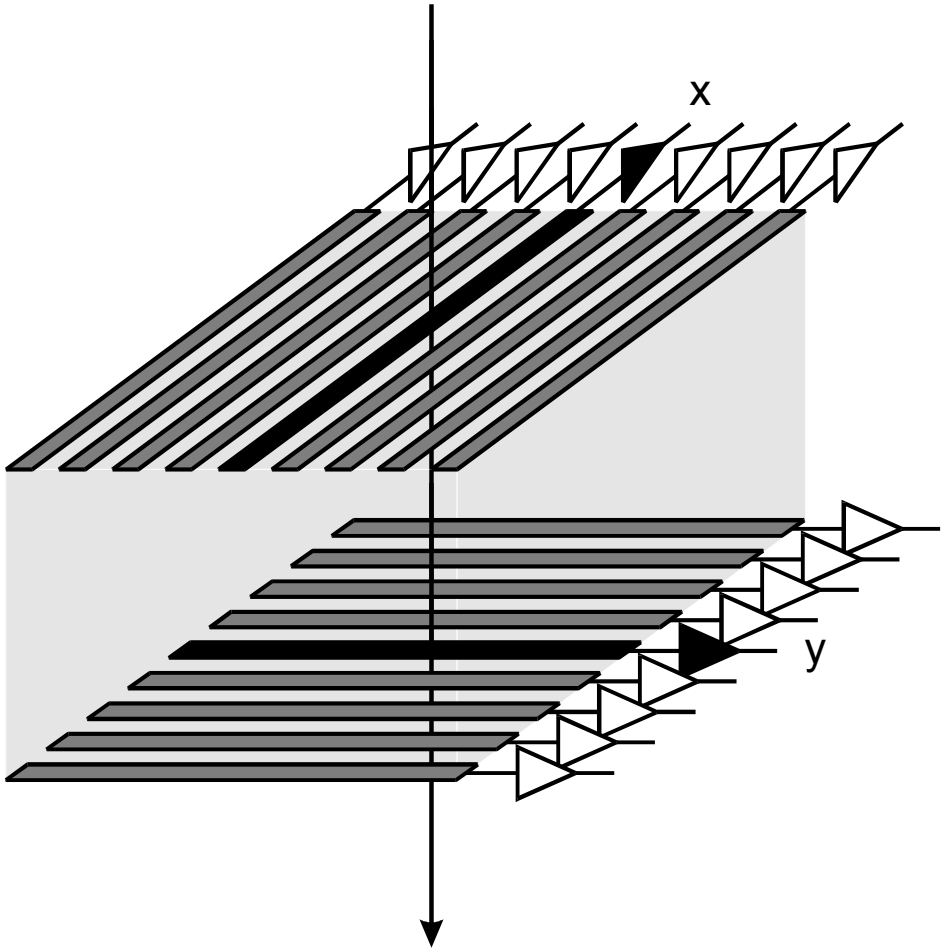
Problem with Two-Dimensional Strip Detectors

At low track densities (e.g. LEP):

Crossed strips on opposite sides of Si wafer yield practical two-dimensional data.

n readout channels $\Rightarrow$

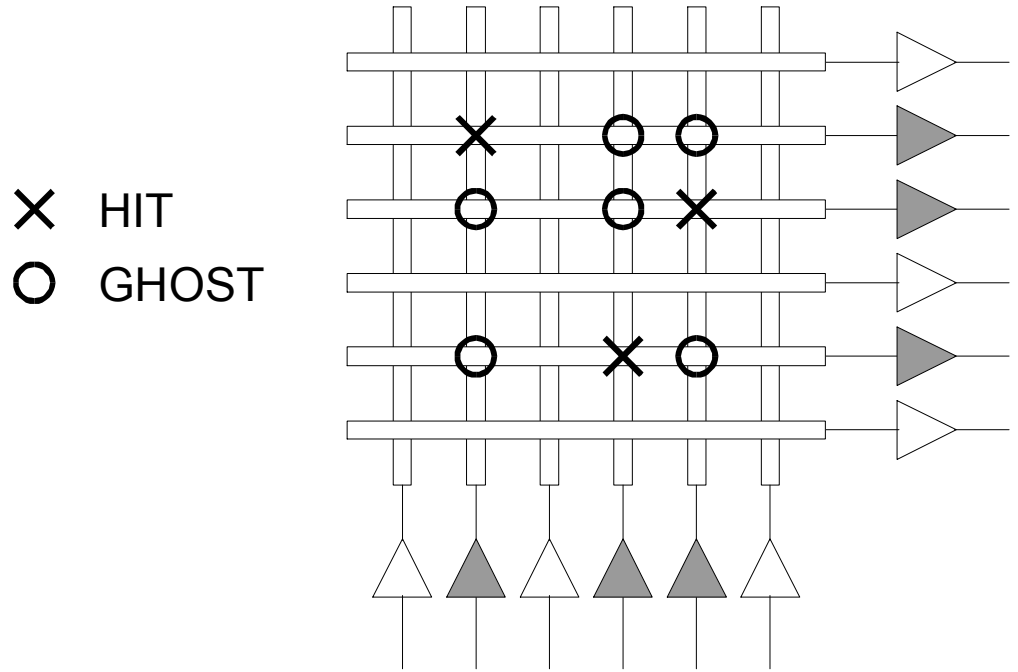
n^2 resolution elements



Problem:

Ambiguities with multiple hits

Ambiguities with multiple simultaneous hits ("ghosting")



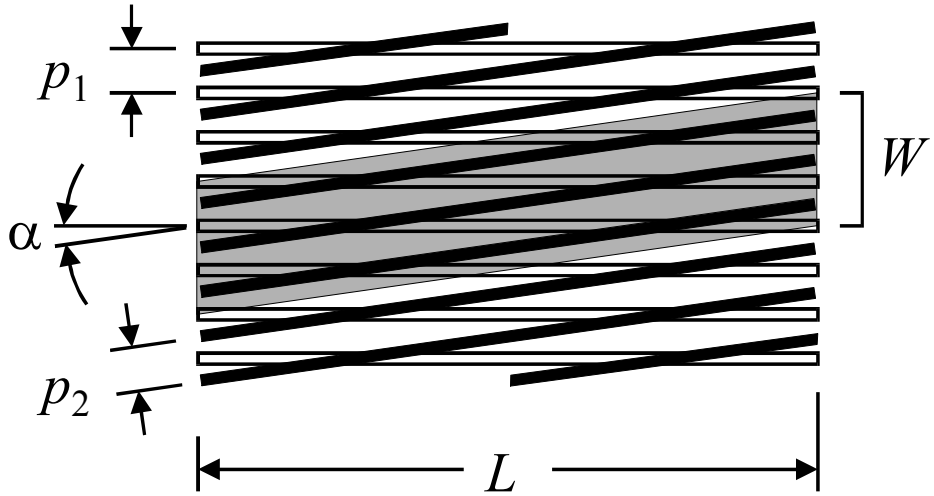
n hits in acceptance field $\Rightarrow$ n x-coordinates
n y-coordinates

$\Rightarrow$ n^2 combinations

of which $n^2 - n$ are "ghosts"

Reduce ambiguities by small-angle stereo

In collider geometries often advantageous, as z resolution less important than $r\varphi$.



The width of the shaded area subject to confusion is $L\frac{p_2}{p_1}\tan\alpha + p_2$

Example: ATLAS SCT uses 40 mrad small-angle stereo

Two single-sided strip detectors glued back-to-back

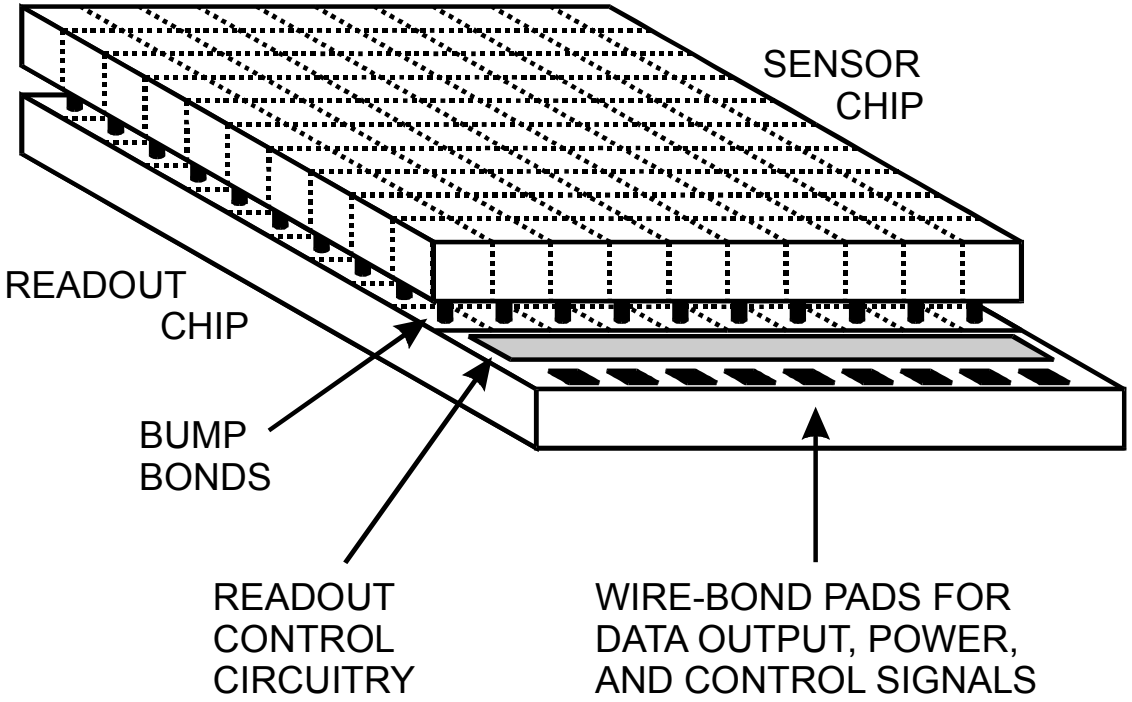
Not sufficient at small radii – need non-projective 2D detector

Detector Structures II – Pixel Devices

1. Hybrid Pixel Devices
   - Example: ATLAS Pixel System
2. Charge Coupled Devices (CCDs)
   - HEP
   - Astronomical Imaging
3. DEPFET Arrays
4. Silicon Drift Chamber
5. Monolithic Active Pixel Sensors (MAPS)
6. Multi-Tier Electronics (aka “SOI” or “3D”)

1. Hybrid Pixel Devices

Join separate sensor and readout.



Electronic design for low power crucial!

Hybrid pixels allow independent optimization of sensor and readout,
e.g. allows non-Si sensor,
but at the expense of material and cost.

Advantages of pixels at LHC

Hit rate at $r_\perp$ = 14 cm: ~ 10^7 $cm^{-2}s^{-1}$ $\Rightarrow$ Small pixels yield low rate per channel

Unambiguous position sensing

Essential for pattern recognition

Radiation damage:

Fluence per year at r ~ 10 cm: typ. $5 \cdot 10^{13}$ cm^{-2} (equivalent 1 MeV neutrons)

Ionizing Dose per year at r ~ 10 cm: 30 kGy (3 Mrad)

Small pixels:

- Detector bias current per element still small after radiation damage
- ~100 fF capacitance allows low noise, so system tolerates degradation of both detector signal and electronic noise due to radiation damage

Drawback: Engineering complexity order of magnitude greater than previous chips

Question: What is the ultimate limit of radiation resistance?

Current design could survive 5 – 10 years at nominal LHC luminosity.

Luminosity upgrade? Much R&D necessary.

Requires significant circuit complexity per pixel:

Each pixel cell includes

- Charge-sensitive-amplifier + shaper per pixel
- Threshold comparator per pixel
- Trim-DAC per pixel for fine adjustment of threshold
- Time-over-threshold analog digitization
- Test pulse circuitry per pixel (dual range)
- Buffer memory to accommodate trigger latency
- Circuitry to mask bad pixels

ATLAS Pixel Detector

Pixel size: 50 μm x 400 μm

Size is historical:
could be 50 μm x 200 μm

Power per pixel: < 40 μW

Each chip: 18 columns x 160 pixels
(2880 pixels)

Module size: 16.4 x 60.4 mm^2

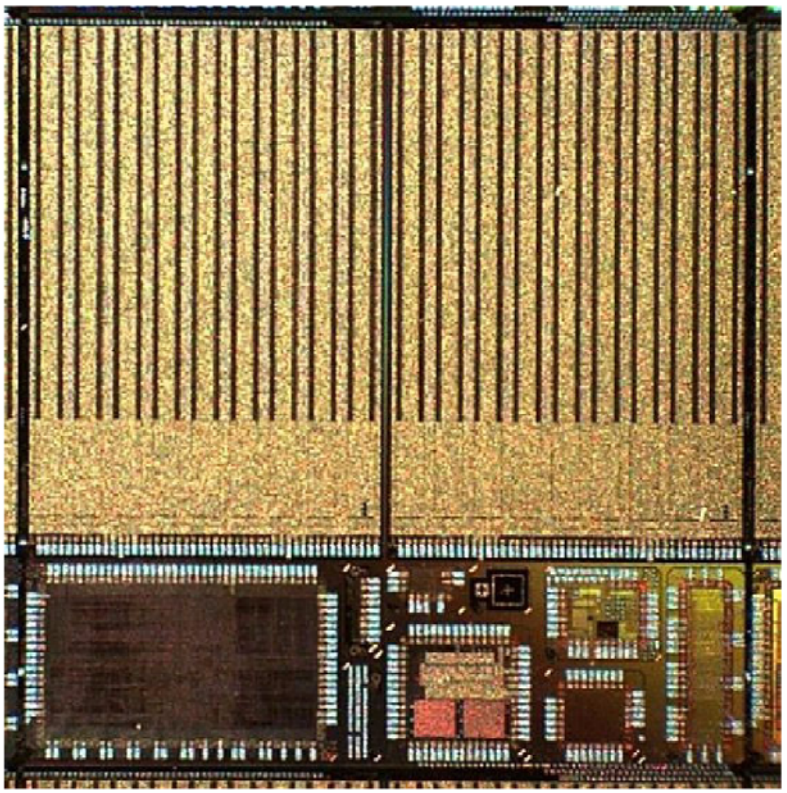
16 front-end chips per module

46080 pixels per module

fabricated in 0.25 μm CMOS

~ 3.5 $\cdot 10^6$ transistors per chip

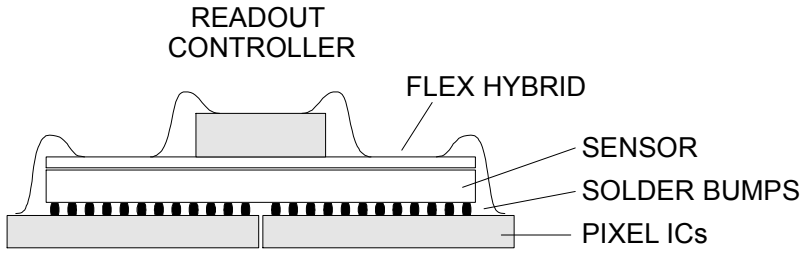
Functional to > 100 Mrad



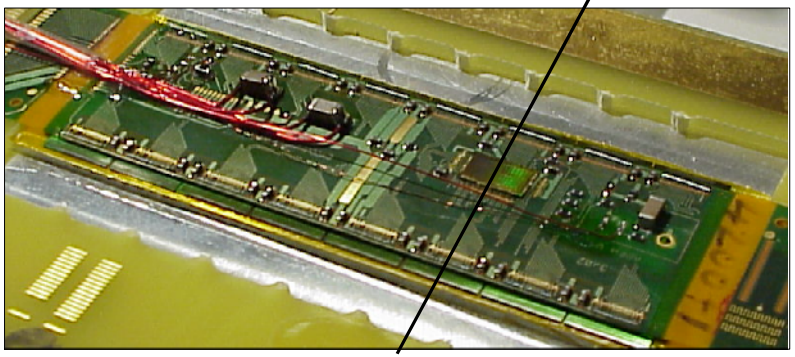
Radiation resistant to higher fluences than strips because low noise provides large performance reserves.

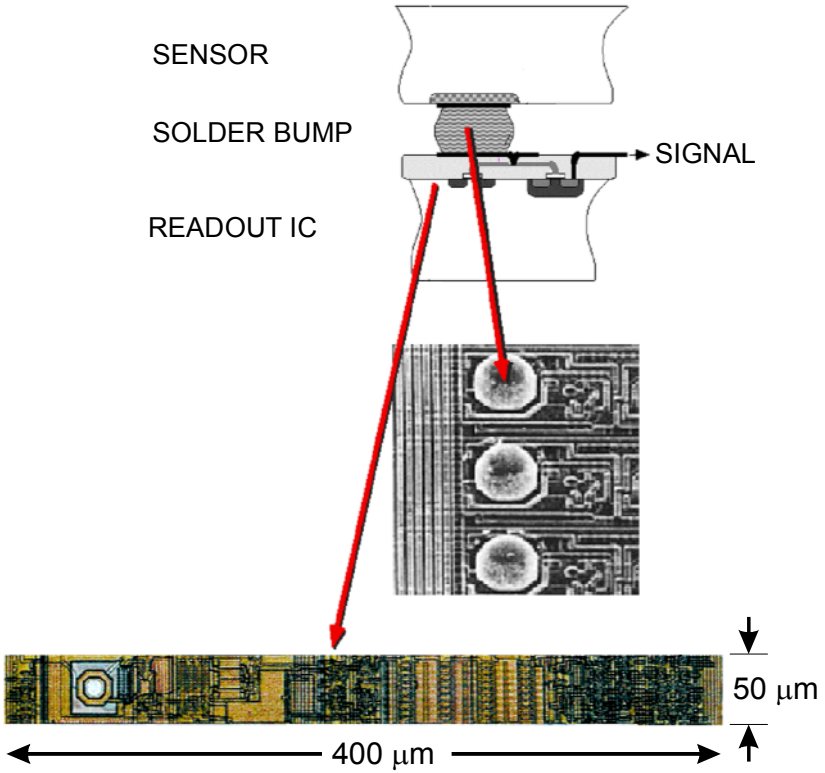
ATLAS Pixel Module

Sensor used as substrate to mount 16 readout ICs



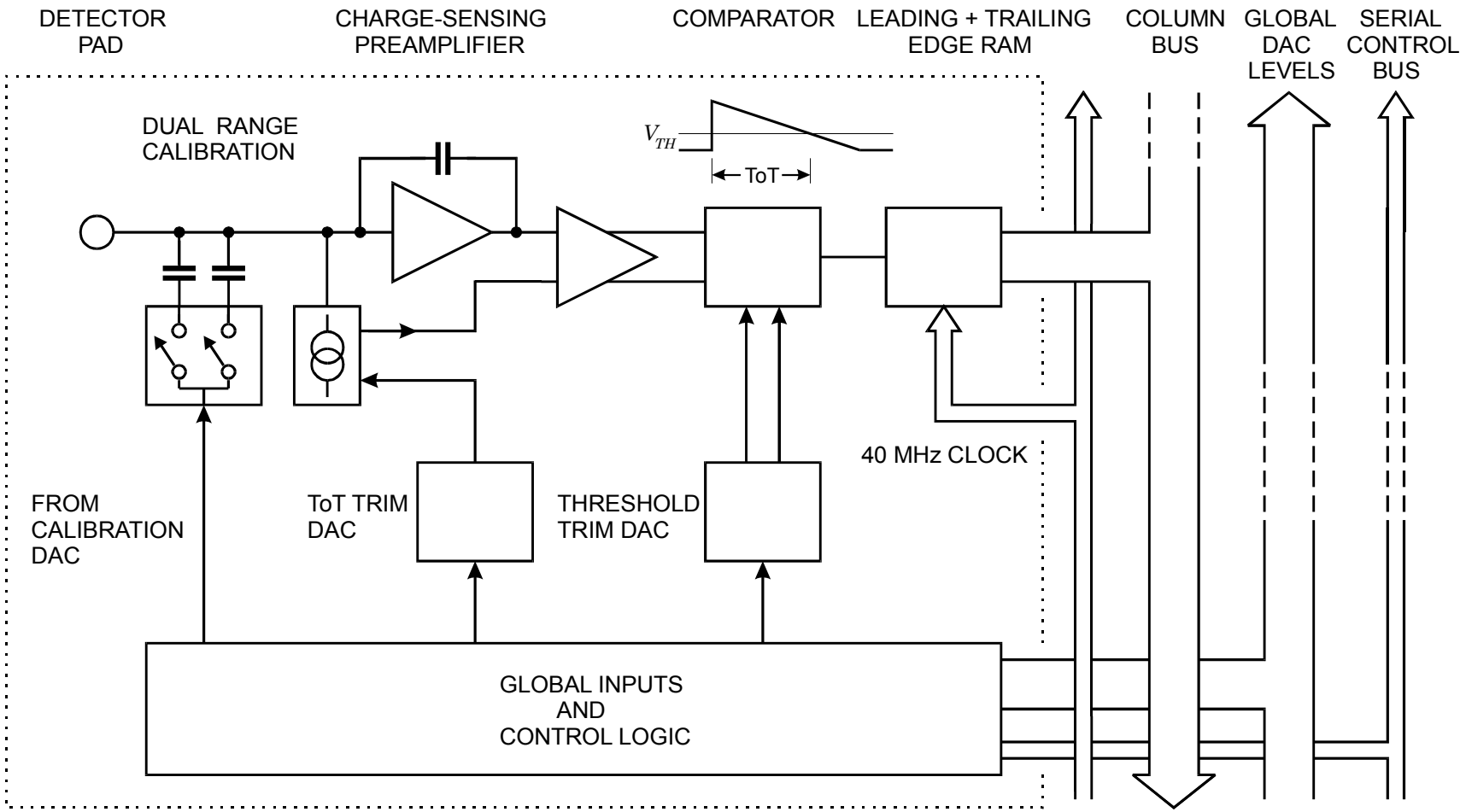
SCHEMATIC CROSS SECTION (THROUGH HERE)





Two-dimensional arrays of solder bump bonds connect ICs to sensor.
Bump bonding at small pitches not industry standard – requires large production quantities
Complicates prototyping relative to bump bonding, which can be done in lab.

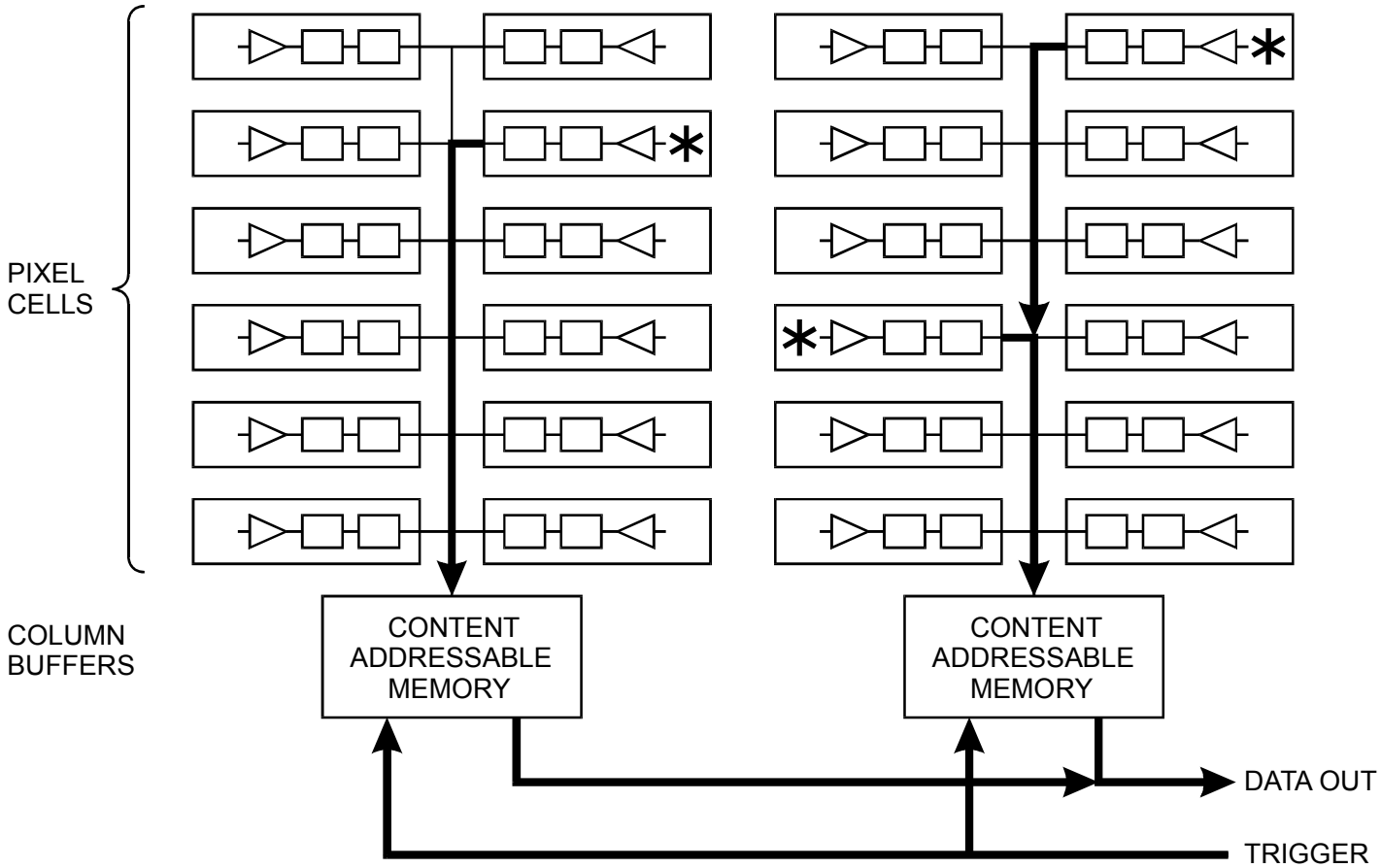
ATLAS Pixel Cell



0.25 μm CMOS, $Q_n \approx 170$ e

40 μW per cell; total power for 2880 pixels: 200 mW (incl. peripheral circuitry)

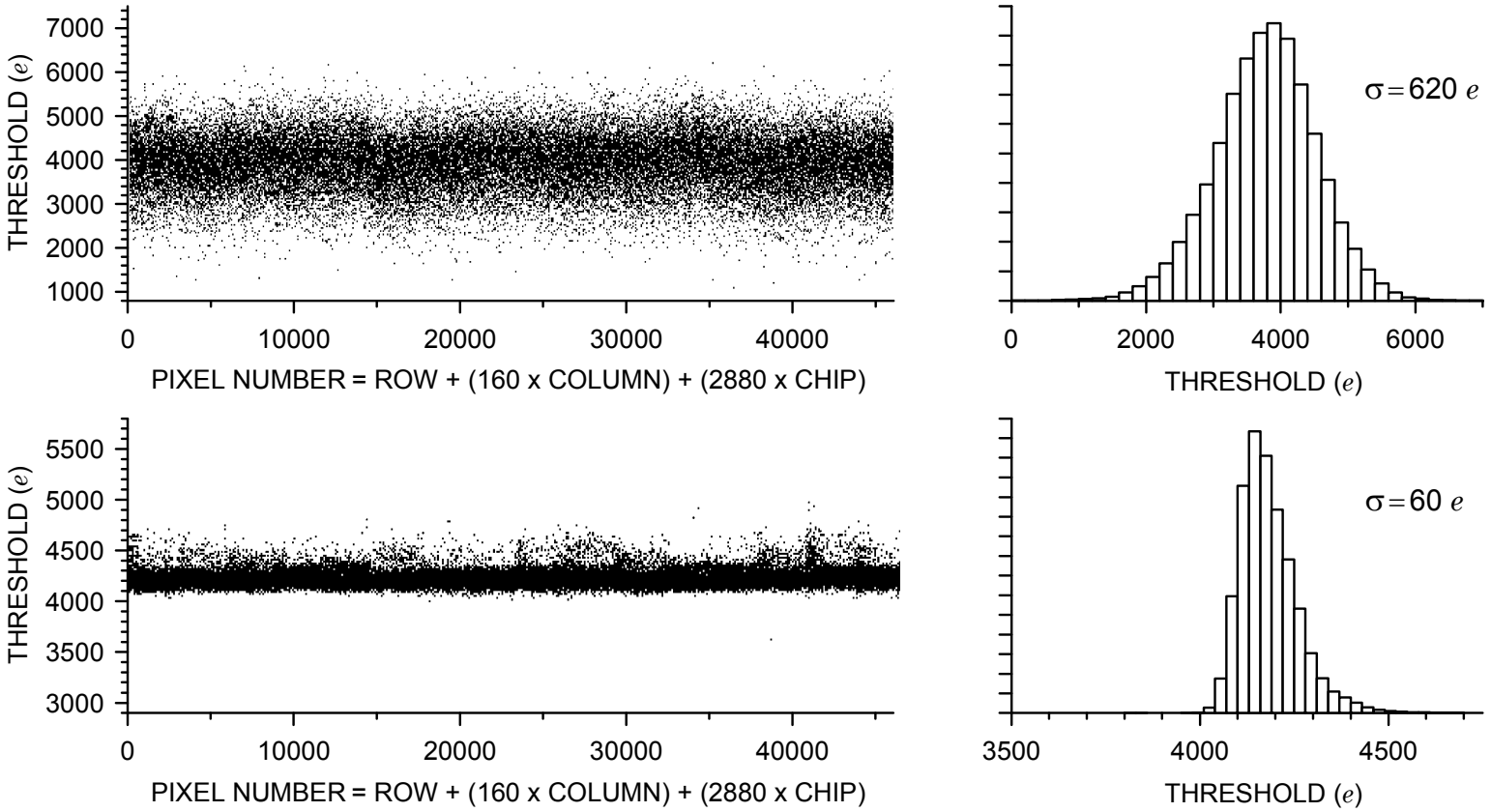
Readout Scheme



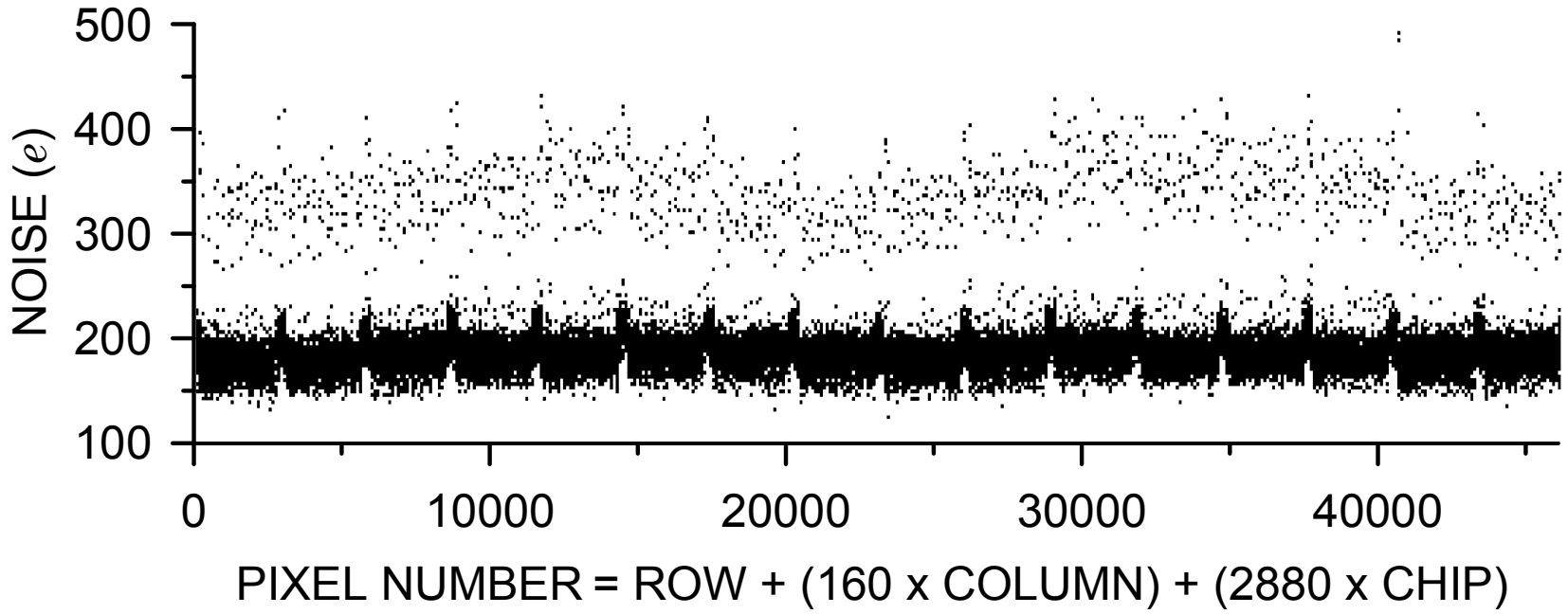
Pixels continuously active, but don't send signals until struck (self-triggered).
Time stamp for struck pixels stored immediately in Content Addressable Memory
Data stored in pixel until Level 1 trigger received for stored time stamp.

Threshold dispersion must be smaller than noise.
Small feature sizes ⇒ large threshold dispersion ⇒ correct with trim DAC

Threshold dispersion before and after trimming



Noise Distribution



Three groups visible:
1. nominal pixels
2. Extended pixels that bridge columns between ICs (spikes every 2880 pixels)
3. Ganged pixels to bridge rows between ICs

Where are we Going?

ILC: μm position resolution in vertex detector (1 – 5 μm)

$\Rightarrow$ ~20 μm pixels

Jet (multi-track) resolution

Minimal mass

$\Rightarrow$ monolithic pixel devices

(CCDs, MAPs, DEPFETs, multi-tier ICs?)

$\Rightarrow$ low-mass power distribution, cooling

sLHC: 10-fold luminosity

$\Rightarrow$ radiation hardness limited primarily by sensor

Charge trapping in the sensor $\Rightarrow$ reduced signal

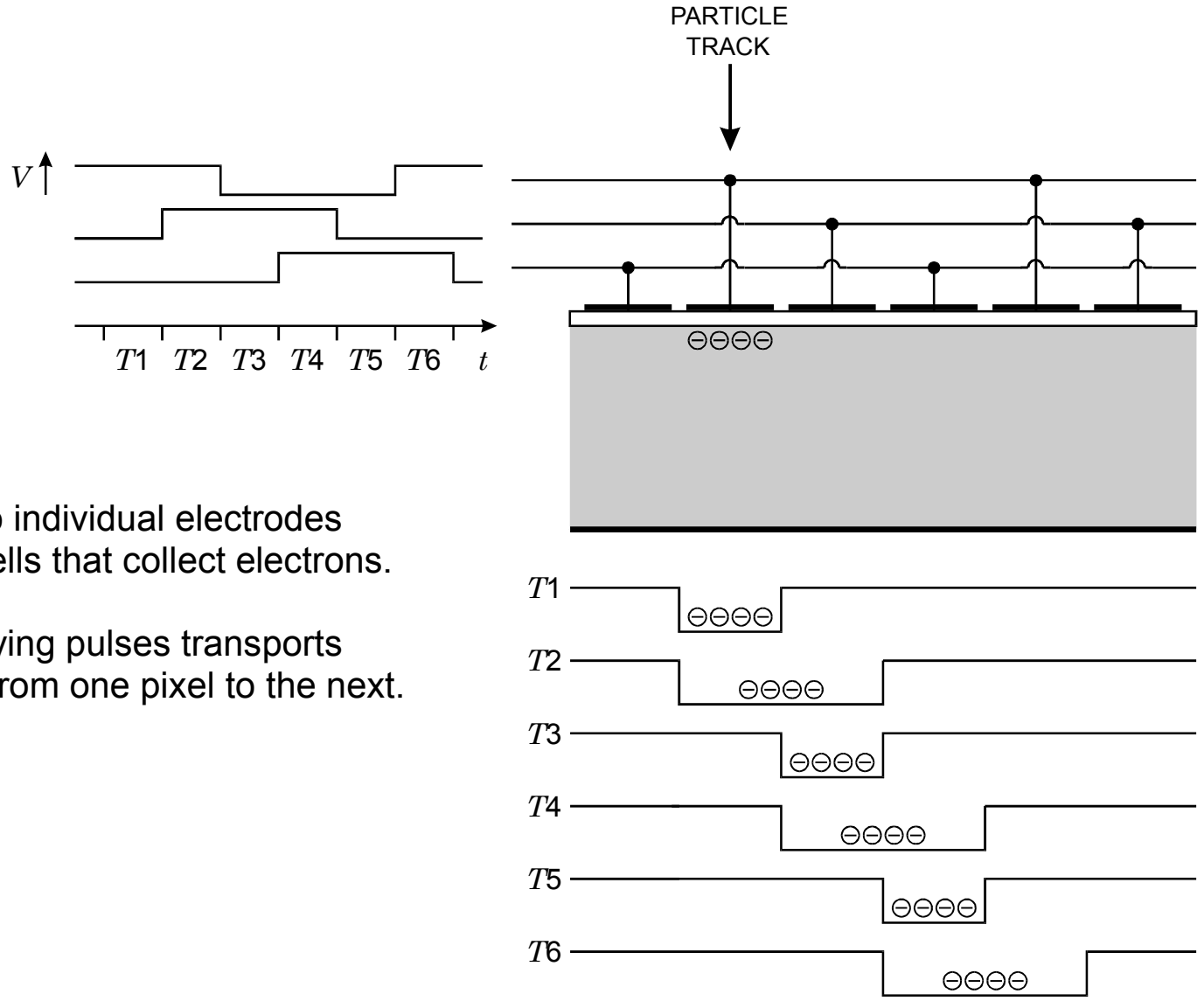
Hybrid pixels allow separate optimization of sensor material and readout,

but at the expense material and cost.

Other pixel types may be much better matched to different applications.

2. Charge Coupled Devices (CCDs)

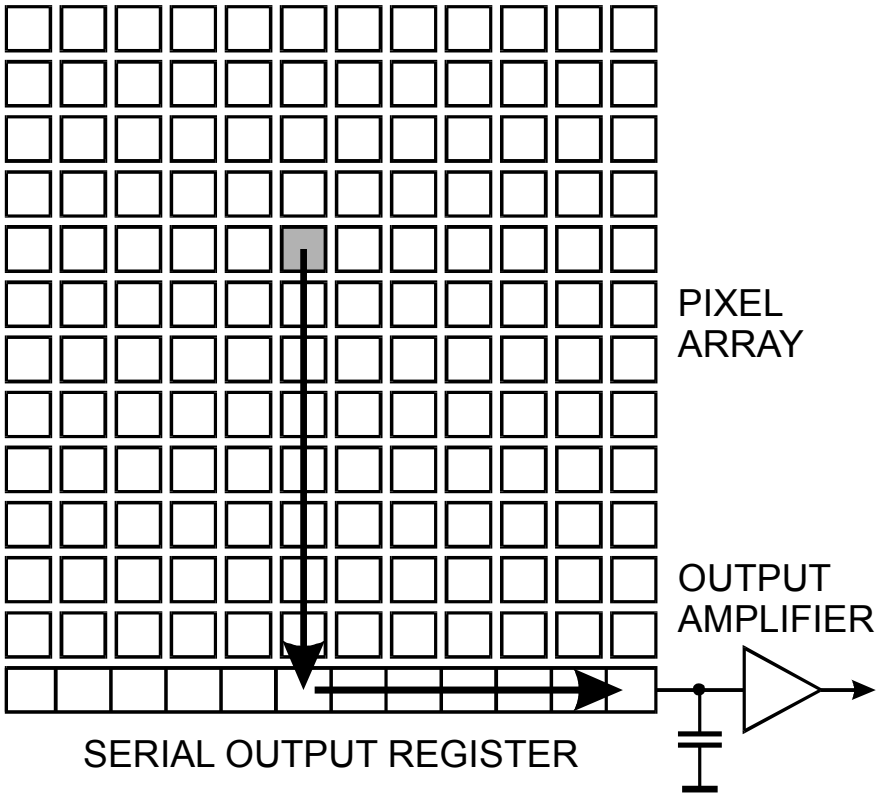
CCD Principle



Voltage applied to individual electrodes forms potential wells that collect electrons.

Sequentially applying pulses transports electron buckets from one pixel to the next.

CCD Readout



Sequential readout requires that some charge buckets have to traverse complete array.

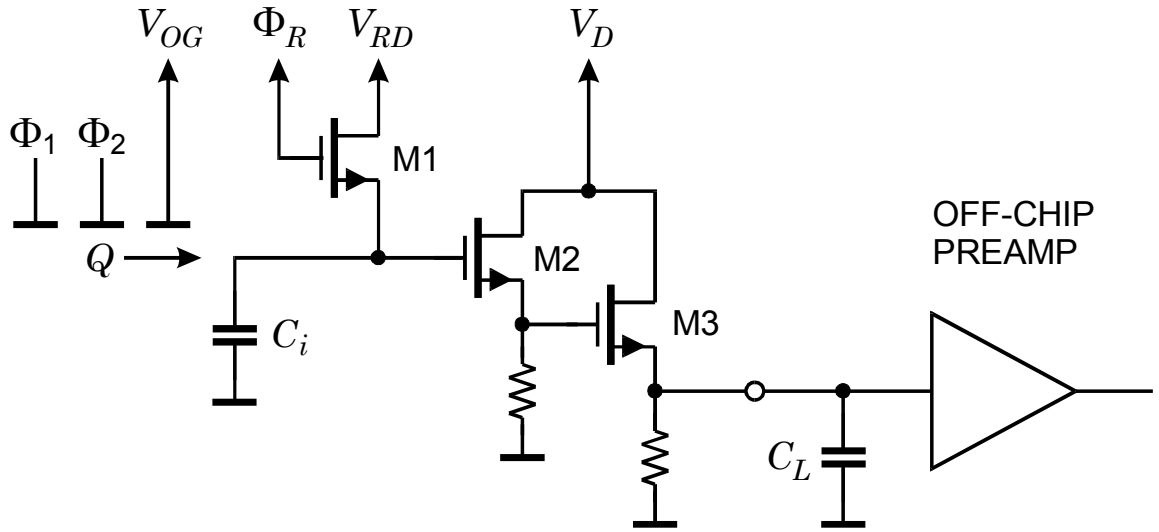
Requires extremely high transfer efficiency – achieved in practice!

Long readout times: $T = N_{col} N_{row} T_{clock}$ (e.g. 200 ms in VXD3)

Clock rates typ. 5 – 10 MHz, but 50 MHz in ILC prototype designs

Advanced designs have one readout amplifier per column to speed up readout.

Typical on-chip readout amplifier



Circuit in VXD3 vertex detector in SLD – Equivalent Noise Charge ~100 e.

Utilize correlated double sampling

CCDs cooled to achieve low noise and high transfer efficiency: VXD3 operated at 200K

Charge collected from 20 μm depth, so 20 μm pixels yield 20 $(\mu m)^3$ space points

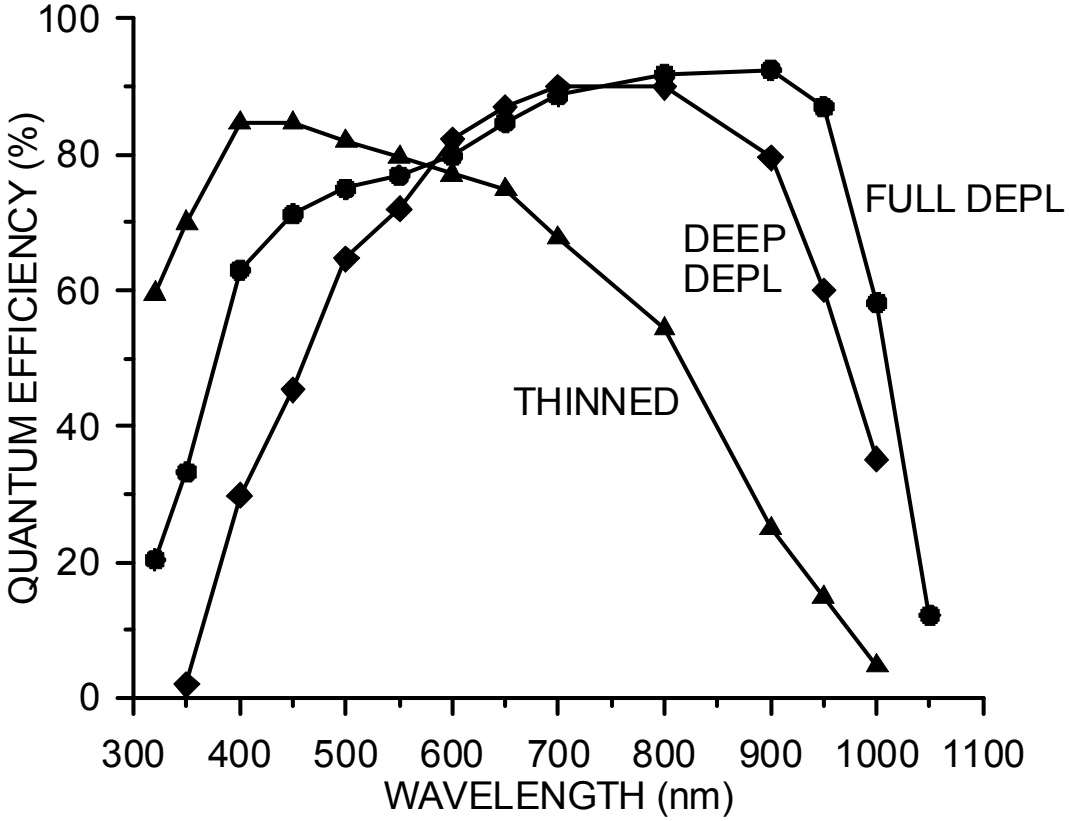
Large arrays: e.g. 80 x 16 mm^2 in VXD3. Larger arrays now available.

CCDs for Astronomical Imaging

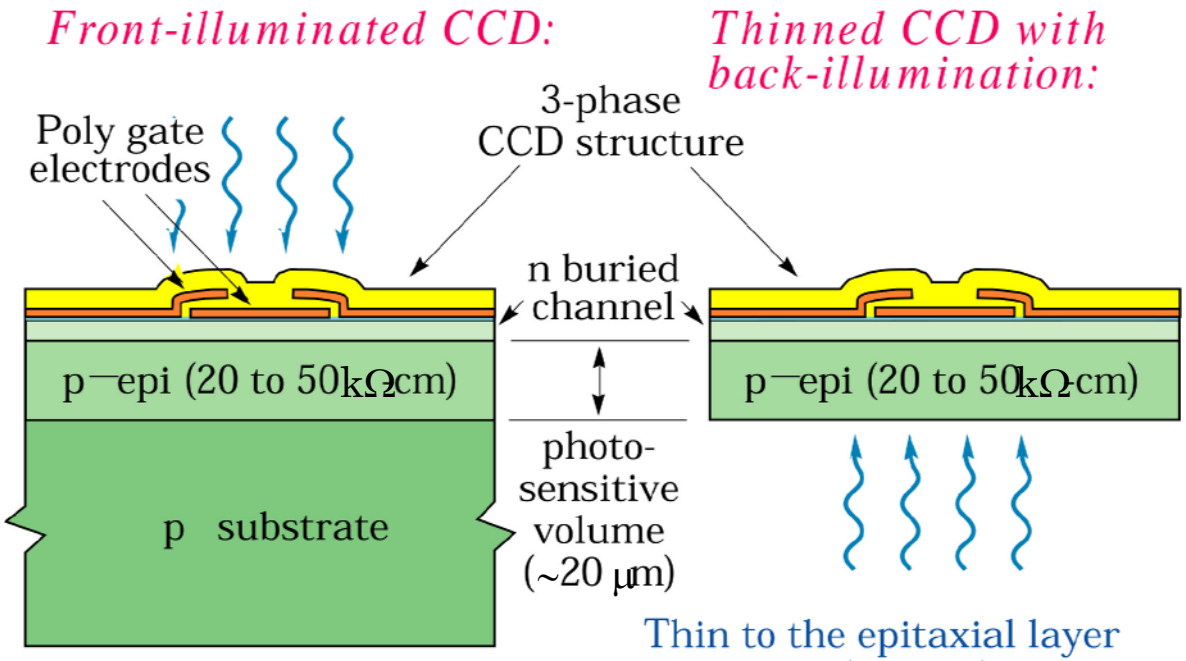
Astronomy requires long exposure times (up to 100s of s)

Single photon sensitivity requires extremely high transfer efficiency
Much larger signals in HEP or conventional imaging (digital cameras) fill traps.

CCD Quantum Efficiency (full depletion at 300 μm thickness)



Conventional CCD Structure



Thin to the epitaxial layer thickness (~20μm)

Drawbacks:

1) Poor blue response due to absorption in polysilicon gate electrodes
2) Poor near-IR response due to thinness of the epitaxial layer
3) Interference patterns due to gate structure

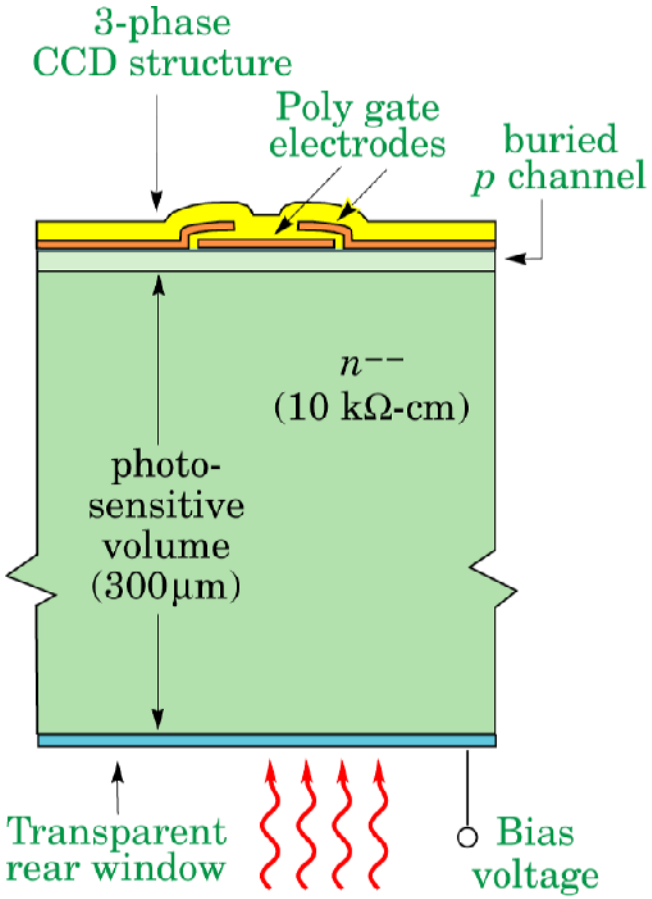
Drawbacks:

1) Thinning is difficult and expensive
2) Poor near-IR response
3) Interference (fringing)
4) Lateral diffusion in field-free region (degraded PSF)

(from S.E. Holland, LBNL)

Fully Depleted CCD
(S.E. Holland, LBNL)

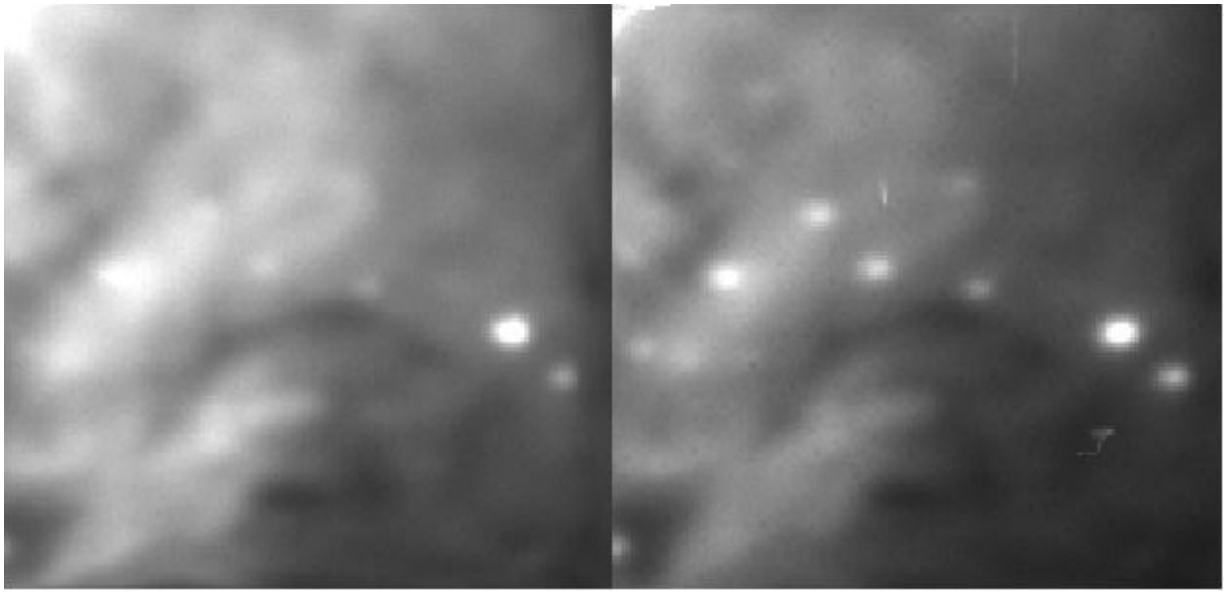
- High resistivity n-type substrate, fully depleted
- Backside illumination
- Transparent window with antireflection coating thin for good blue response
- 300 μm active thickness
  $\Rightarrow$ good QE up to λ= 1 μm
- No costly thinning of devices



Comparison between thinned CCD (bottom) and deep depletion device.

Interstellar dust tends to absorb in the blue, so extended red response of LBNL CCD shows features obscured in thinned CCDs.

“Conventional” thinned CCD Deep Depletion CCD



Lick 1m telescope, 4-Dec-1996

100 mm diameter wafer
fabricated at LBNL

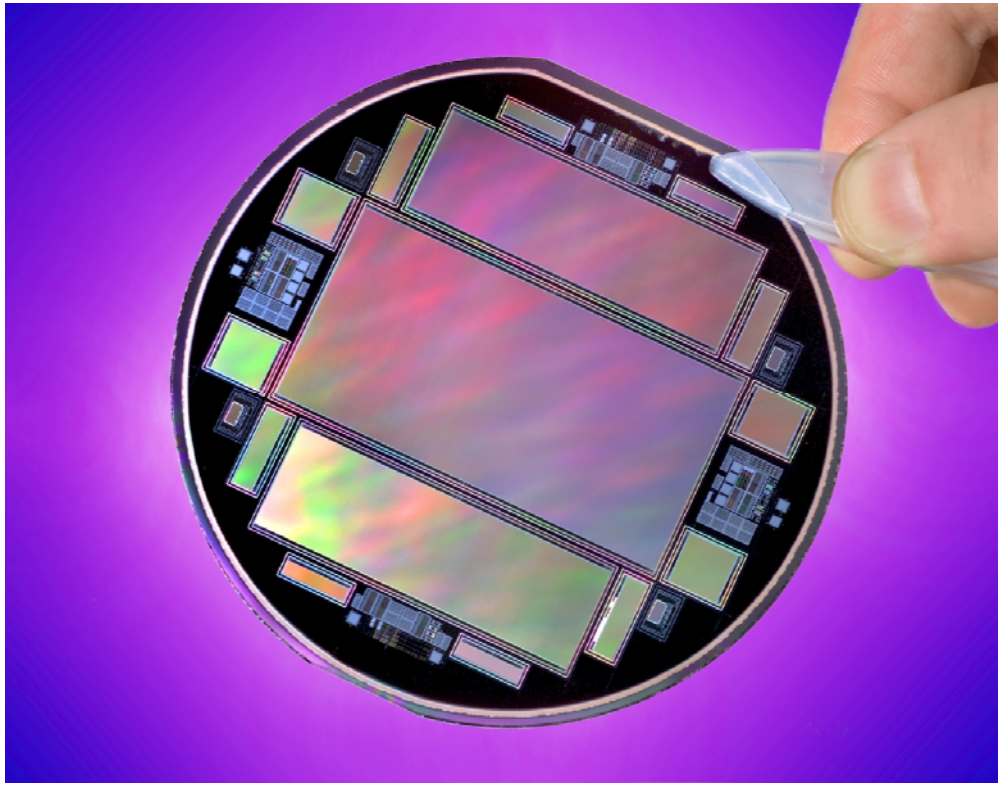
includes

2K x 4K (15 μm pixels),

1.5K x 4.8K (10.5 μm pixels)

1.3K x 4.2K (12 μm pixels)

+ test structures

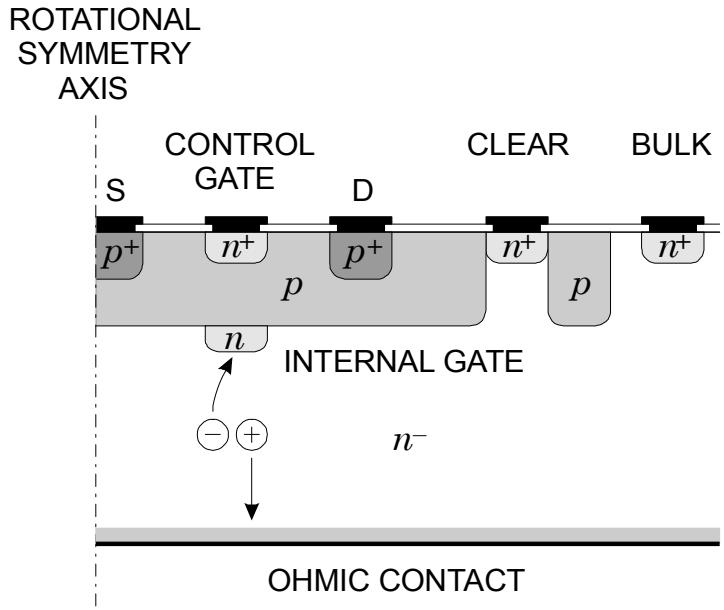


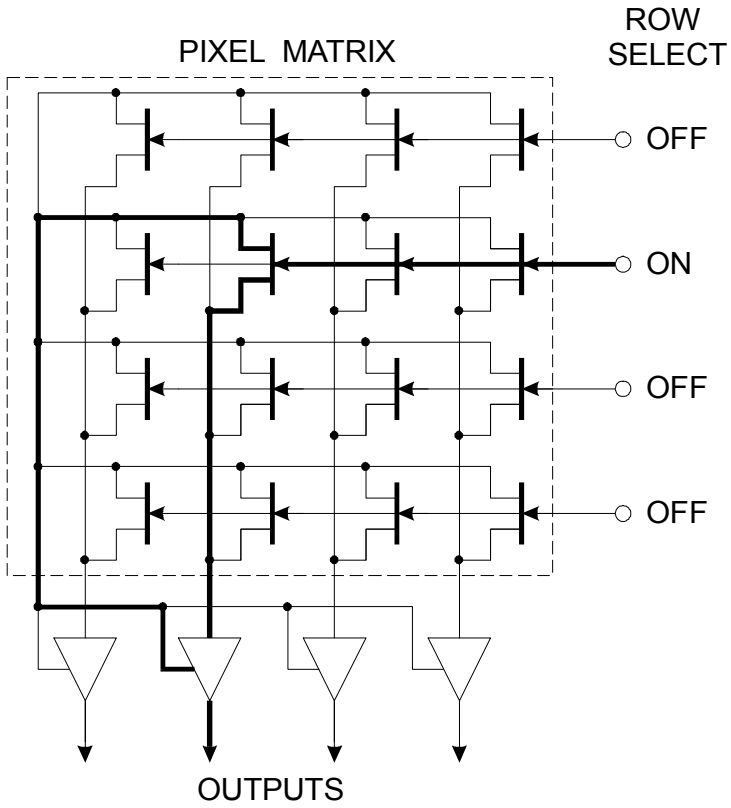
current fab runs on 150 mm wafers.

For more information see http://snap.lbl.gov

3. DEPFET Arrays

A variation on the CCD is the DEPFET array, which implements a transistor in each pixel.





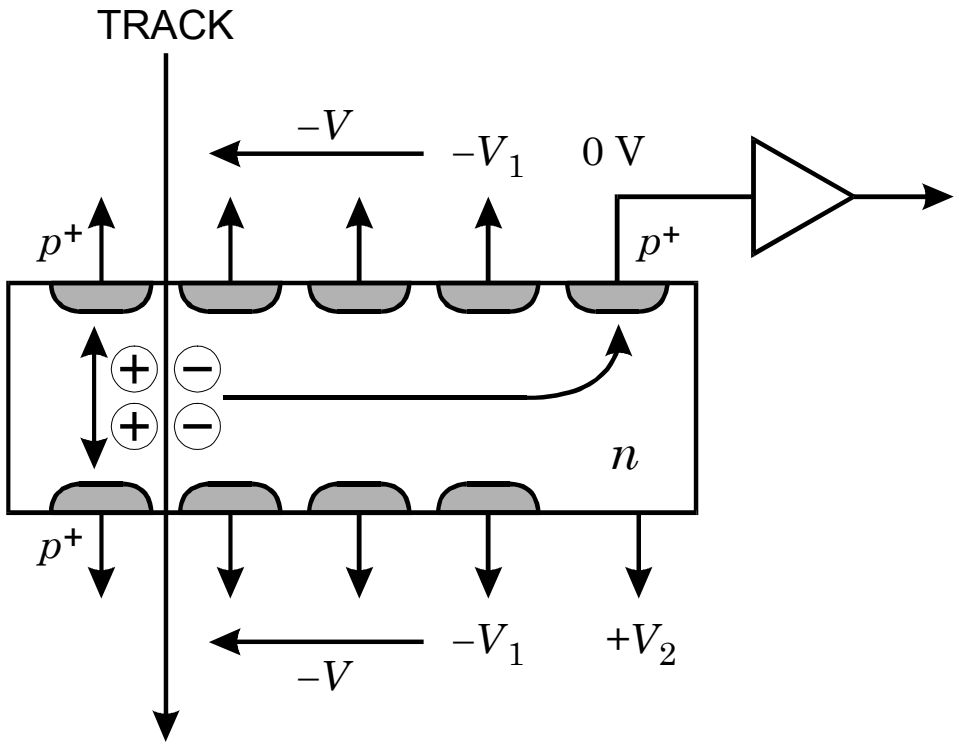
Charge is collected on the internal gate of the transistor. Reduced node capacitance is cited as an advantage, but the transistors are inferior to modern CMOS, so noise is about the same as in CCDs.

Sequential readout as in CCDs, but the selective readout of a portion of the array is possible.

See papers by G. Lutz *et al.* (MPI Munich) and N. Wermes *et al.* (Univ. Bonn) for more details

4. Silicon Drift Chamber

A TPC structure implemented in silicon:



Silicon is depleted from both surfaces to form a potential well in the middle.

A longitudinal field draws the electrons to the readout electrode at the far end.

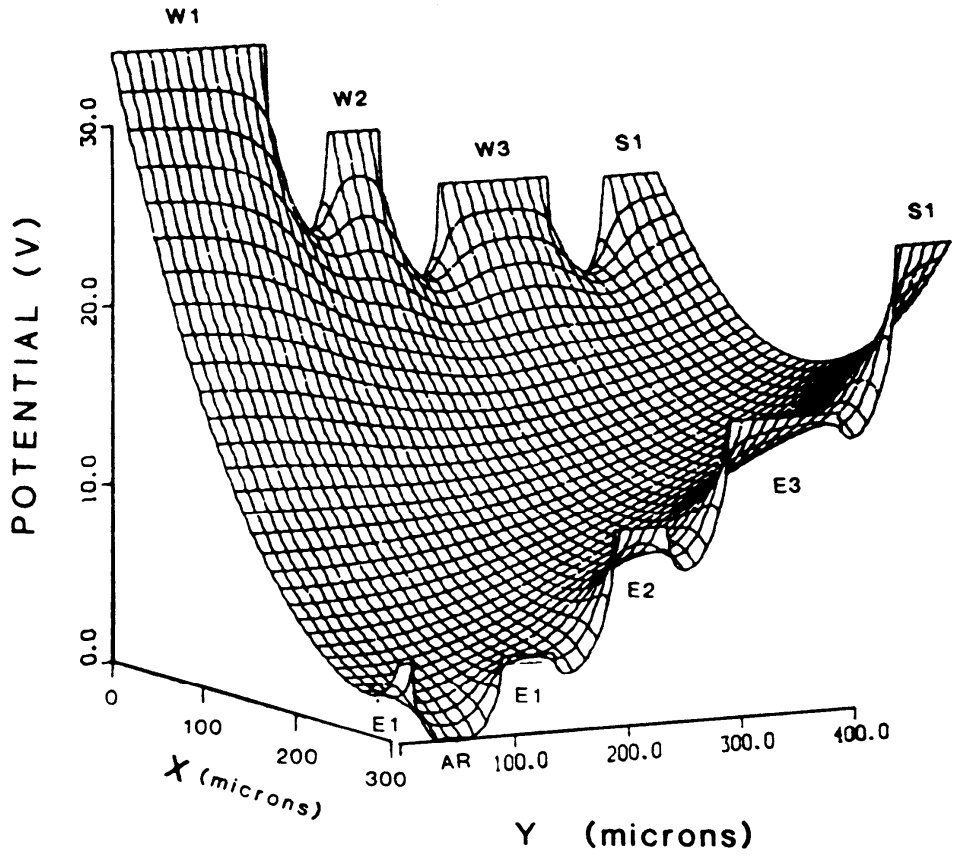
(see papers by Gatti and Rehak, e.g. Nucl. Instr. and Meth. 225 (1984) 608-614)

The potential trough is skewed to direct charge to a readout electrode on the surface.

Silicon drift chamber has advantage that the collection electrode is decoupled from the large acceptance area.

⇒ capacitance can be very small, even on a large area detector
(C~ 50 – 100 fF for A= 10 cm^2)

⇒ ~ 10 μm resolution over 5 – 10 cm drift distance



(from Gatti et al. IEEE Trans. Nucl. Sci. **NS-32** (1985) 1204)

Drift velocity must be predictable.
Trapping must be low for long drift distances (~ cm) ⇒ problem with radiation damage.

Although originally proposed as a position sensing device, an important application is in a low-noise x-ray detector or photodiode.

Next-Generation Pixel Devices

5. Monolithic Active Pixel Sensors (MAPS)

Utilize epi layer of "standard" CMOS as sensor

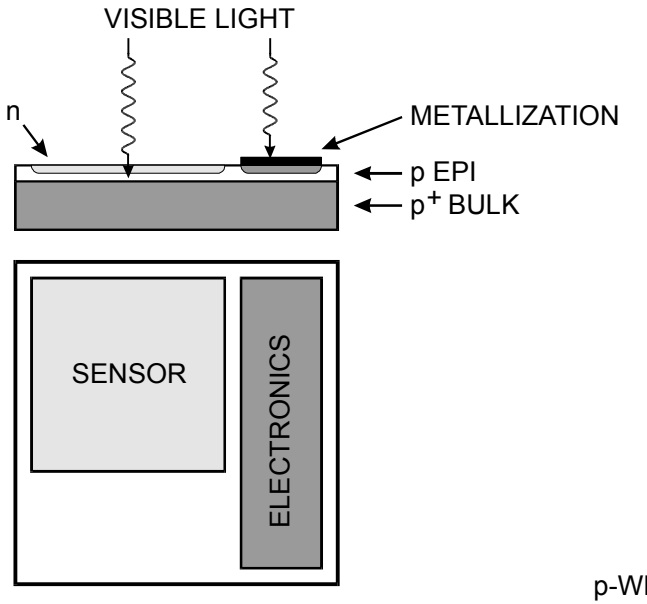
Charge collection by diffusion ⇒

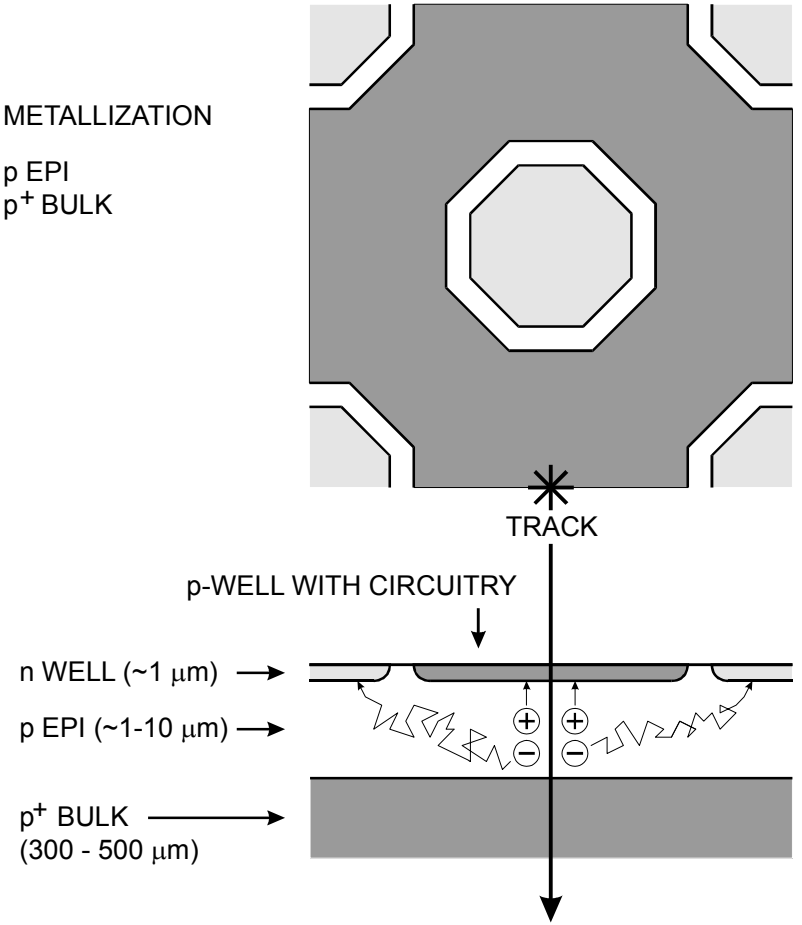
limits speed, radiation resistance

OK for ILC

Designs with ~90% active area per IC

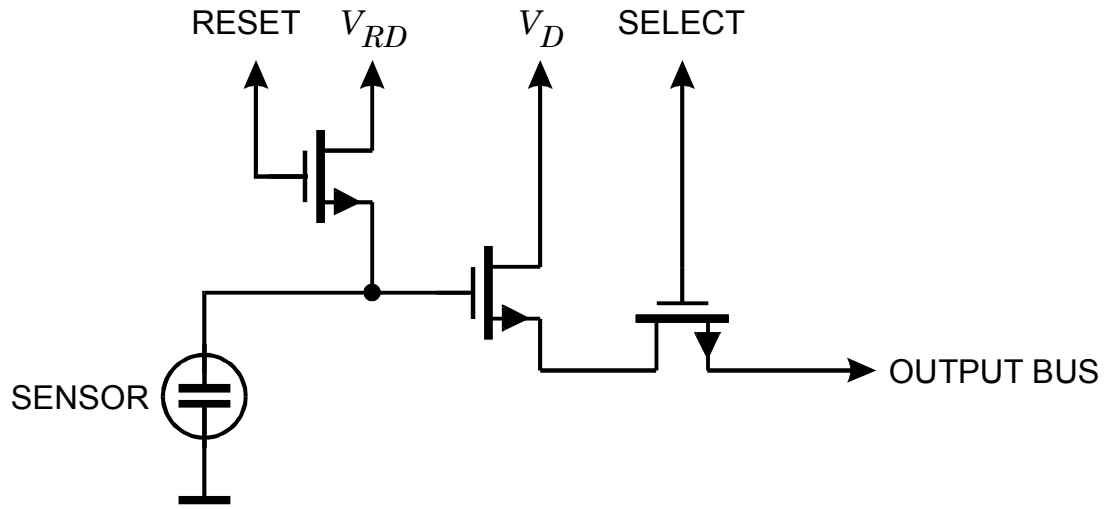
Chips can be thinned to ~50 μm to reduce material. (Battaglia et al.)





Chips limited to 10 – 20 mm size, so many required to cover large area.

Simple MAPS Output Circuit



Some designs implement correlated double sampling on each pixel.

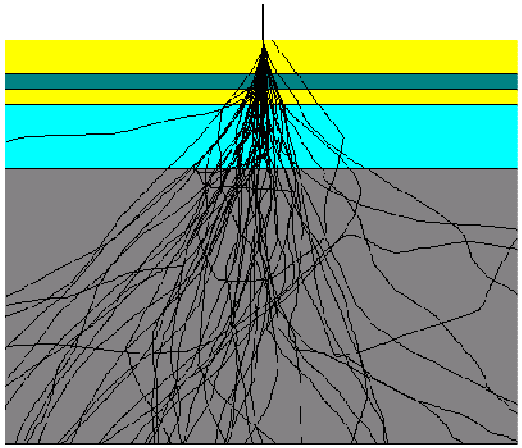
Requires that all pixels be read out, so readout time extends over many beam crossings. Frame rate determines shot noise contribution to Q_n.

Reduce readout time: Full processing chain (preamp, shaper, comparator) required to implement on-chip sparsification.

Some new designs include threshold discrimination per pixel:
0.13 μm CMOS, 25 μm pixel, but threshold dispersion ≈ elec. noise.

Monolithic Pixels

Electron Detection



- Essentially all charge collected from thin region
- Detector can be thinned
- Higher energy $\Rightarrow$ better PSF, lower S/N
- Pixels are small (so there can be more of them, but they are less intelligent than hybrid pixels)

But ...

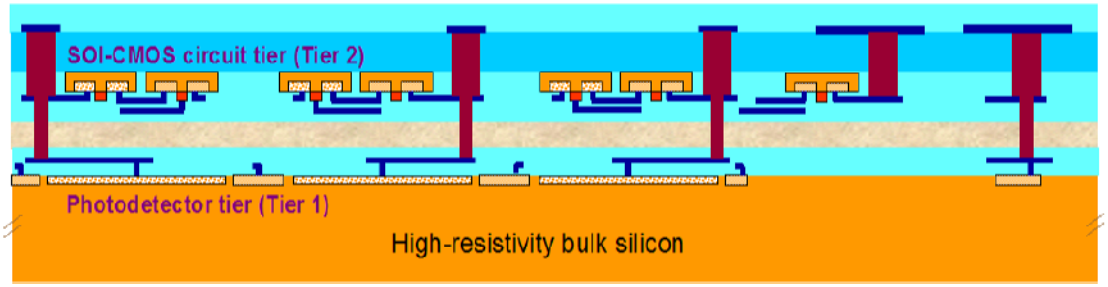
- Radiation damage (electric field in the detection region is not well controlled)
- Diffusion (because collection region is not depleted)

6. Multi-Tier Electronics (aka “SOI” or “3D”)

CMOS Circuitry

Isolation Oxide

Sensor Layer

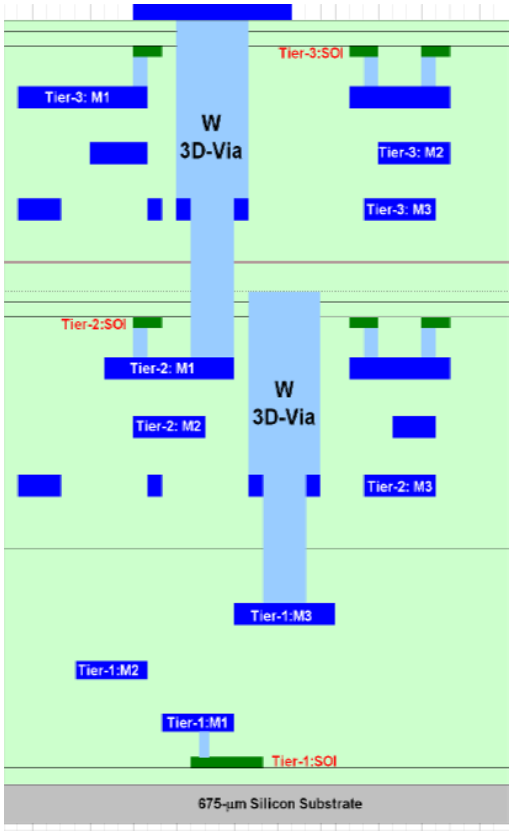


MIT Lincoln Lab

3-Tier Design (FNAL)

3 transistor levels
11 metal layers

Accommodate additional circuitry for given pixel size.



(R. Lipton, STD6)

Test Chips designed at KEK (Arai et al.)

Fabricated by OKI

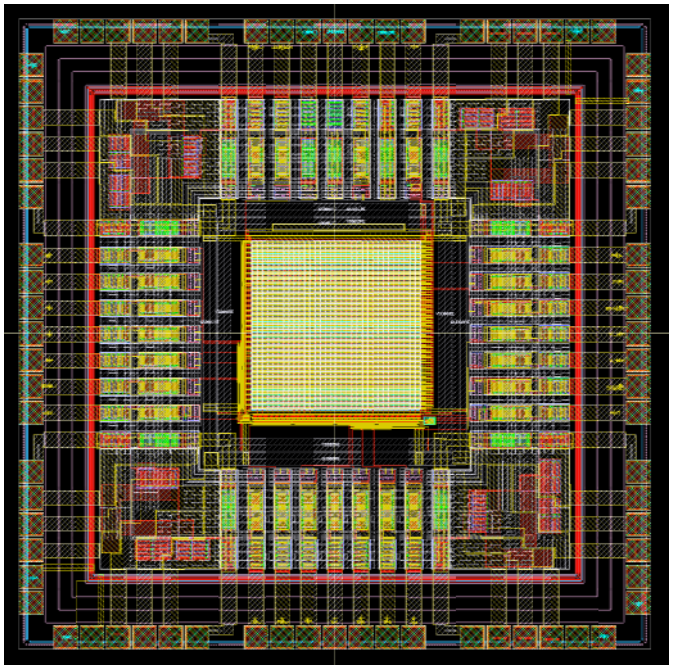
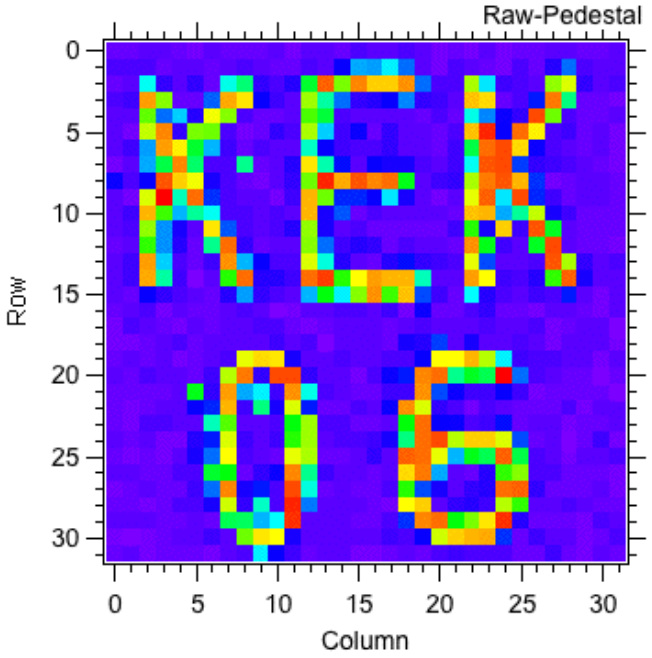


Image (20 μm pixels)



High resistivity substrate (1 kΩ cm CZ) thinned to 350 μm.
(see talk T6.9 by Tsuboyama et al.)

Radiation resistance of sensor layer in industrial processes inadequate for SLHC, but suitable for ILC.

Summary

Both ILC and SLHC drive developments towards higher levels of segmentation.

ILC: Micron-resolution pixel detectors for vertexing.
Material even more critical than at LHC

Candidates: CCDs, MAPS, DEPFETs

CCDs and DEPFETs fabricated as large area devices
- CCDs available commercially
- DEPFETS local MPI Munich development

MAPS require integration of many small devices
- additional mass in mounting + cooling

Multi-Tier structures offer better controlled charge collection, but much R&D necessary.

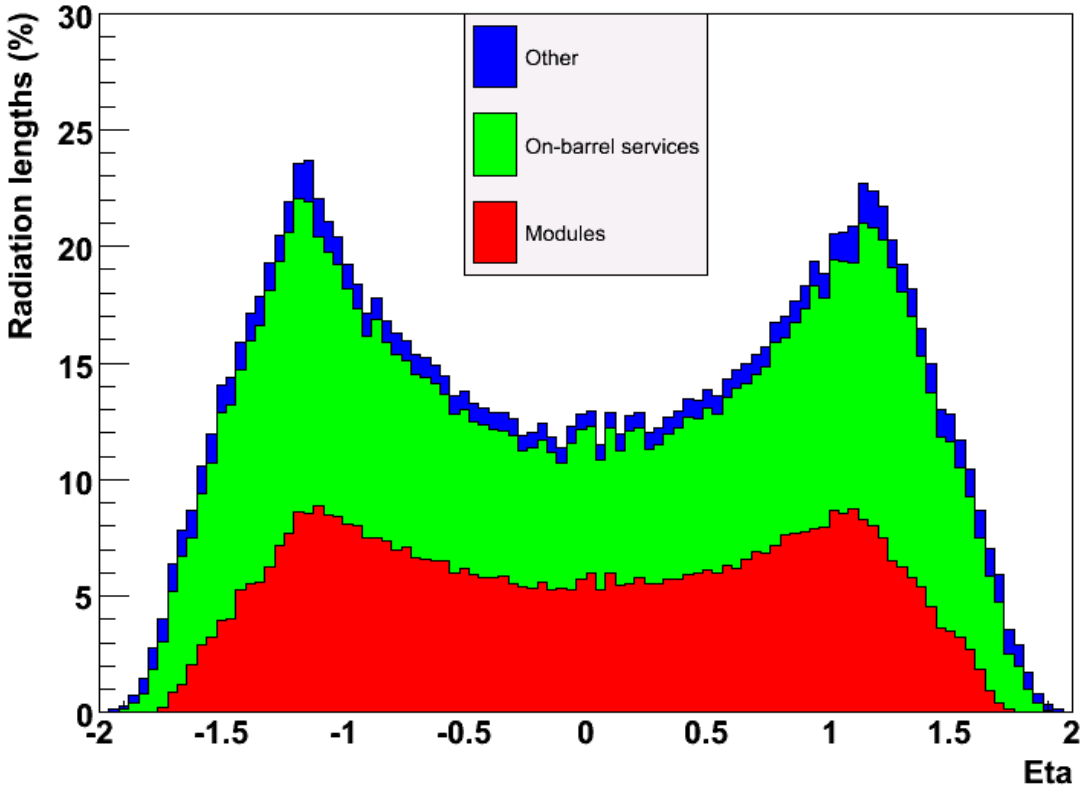
sLHC: Increased radiation resistance required:
$\Rightarrow$ short strips and hybrid pixel detectors

Challenge: reduce power dissipation and material

Sobering Reminder: Material in ATLAS Silicon Tracker Barrel

Total material per layer:
3% X_0.

Half is services:
cooling
cabling
carbon fiber support



(see http://www.hep.phy.cam.ac.uk/~cpw1/atlas.html)

ATLAS Pixel Detector:	Total (3 layers)	10.7% X_0
	Hybrids + Cables	1.3% X_0
	Support + Cooling	6.9% X_0

Can we do better?

Challenges

- No “silver bullets”!
- Systems design is crucial in advanced detectors.
- Many details interact, even in conceptually simple designs.
- It is essential to understand key aspects and their interactions.
- Key front-end issues don’t require detailed electronics knowledge of circuits, but understanding of basic underlying physics is essential.
- Broad physics education required.

  U.S. physics departments commonly do not recognize the scientific aspects of instrumentation R&D.

  Many developments are essentially made as technician efforts, so the simplistic perspective doesn’t accept that novel developments require a scientific approach.

  Emphasis on theory and mathematical techniques neglects understanding of physics and how to apply it to undefined multidimensional problems.