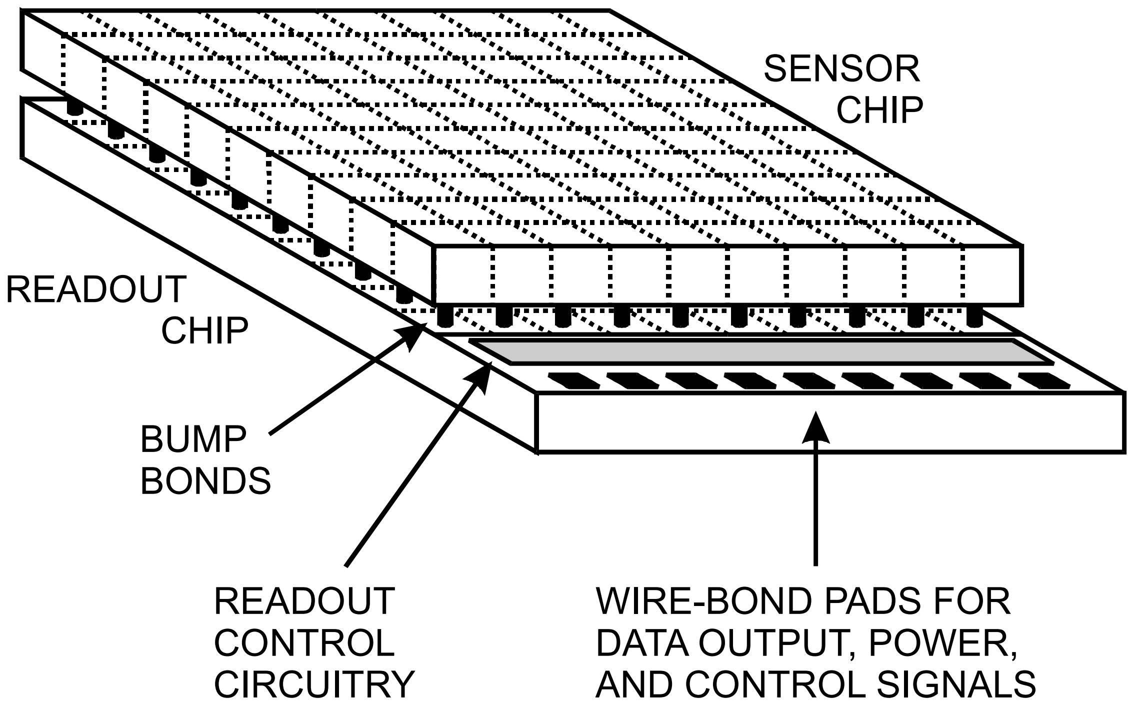
Detector Structures II – Pixel Devices

1. Hybrid Pixel Devices
   Example: ATLAS Pixel System
2. Charge Coupled Devices (CCDs)
   HEP
   Astronomical Imaging
3. DEPFET Arrays
4. Silicon Drift Chamber
5. Monolithic Active Pixel Sensors (MAPS)
6. Multi-Tier Electronics (aka “SOI” or “3D”)

1. Hybrid Pixel Devices

Join separate sensor and readout.



Electronic design for low power crucial!

Hybrid pixels allow independent optimization of sensor and readout,
e.g. allows non-Si sensor,
but at the expense of material and cost.

Advantages of pixels at LHC

Hit rate at $r_\perp = 14$ cm: ~ 10^7 cm^{-2}s^{-1} $\Rightarrow$ Small pixels yield low rate per channel

Unambiguous position sensing

Essential for pattern recognition

Radiation damage:

Fluence per year at r ~ 10 cm:	typ. $5\cdot 10^{13}$ cm^{-2}	(equivalent 1 MeV neutrons)
Ionizing Dose per year at r ~ 10 cm:	30 kGy (3 Mrad)	

Small pixels:

- detector bias current per element still small after radiation damage
- ~100 fF capacitance allows low noise, so system tolerates degradation of both detector signal and electronic noise due to radiation damage

Drawback: Engineering complexity order of magnitude greater than previous chips

Question: What is the ultimate limit of radiation resistance?

Current design could survive 5 – 10 years at nominal LHC luminosity.

Luminosity upgrade? Much R&D necessary.

Requires significant circuit complexity per pixel:

Each pixel cell includes

- charge-sensitive-amplifier + shaper per pixel
- threshold comparator per pixel
- trim-DAC per pixel for fine adjustment of threshold
- time-over-threshold analog digitization
- test pulse circuitry per pixel (dual range)
- buffer memory to accommodate trigger latency
- circuitry to mask bad pixels

ATLAS Pixel Detector

Pixel size: 50 μm x 400 μm

size historical:
could be 50 μm x 200 μm

Power per pixel: < 40 μW

Each chip: 18 columns x 160 pixels (2880 pixels)

Module size: 16.4 x 60.4 mm^2

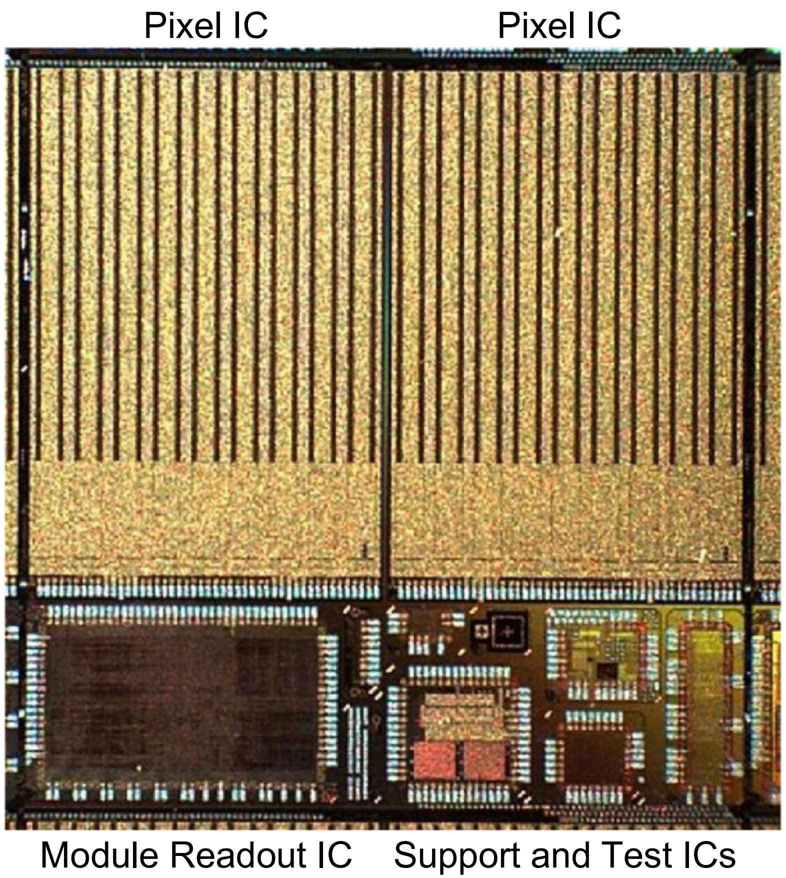
16 front-end chips per module

46080 pixels per module

fabricated in 0.25 μm CMOS

~ $3.5 \cdot 10^6$ transistors per chip

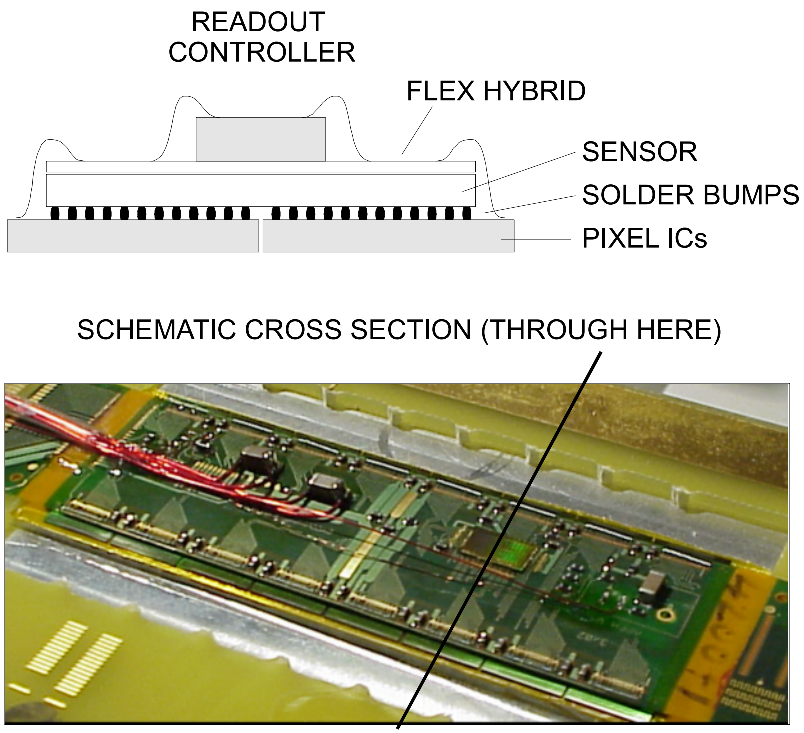
Functional to > 100 Mrad

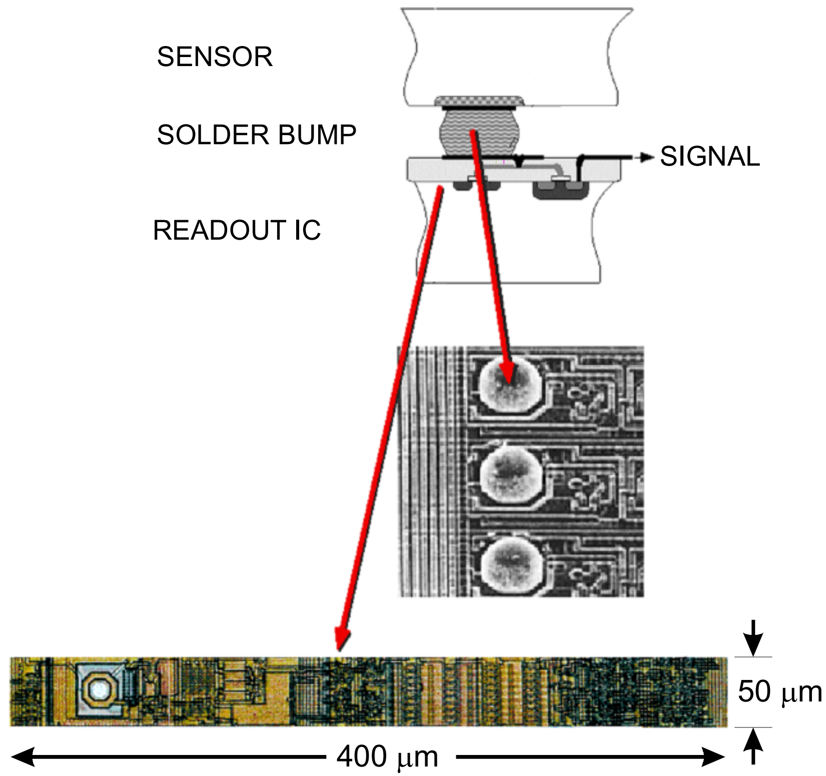


Radiation resistant to high fluences than strips because low noise provides large performance reserves.

ATLAS Pixel Module

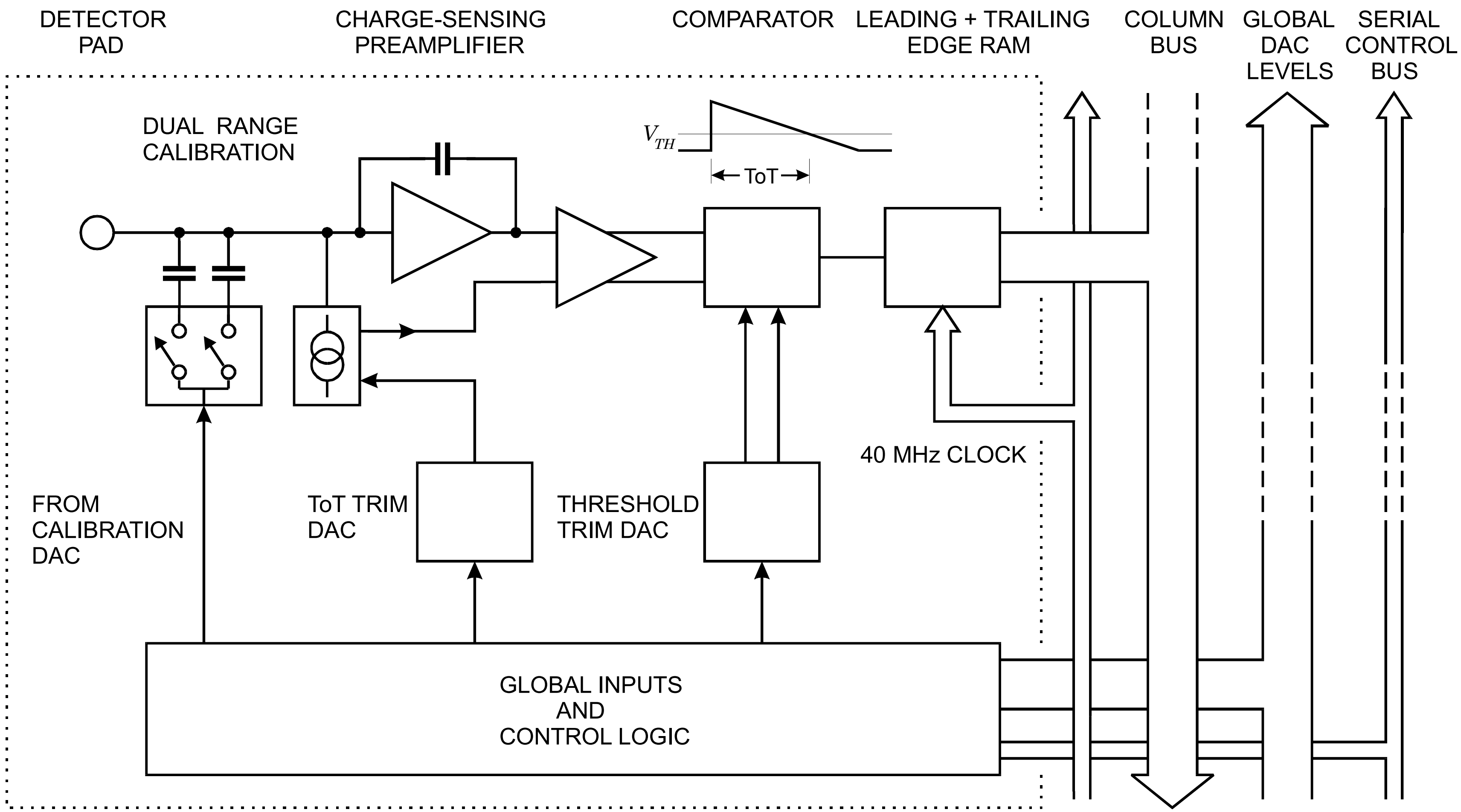
Sensor used as substrate to mount 16 readout ICs





Two-dimensional arrays of solder bump bonds connect ICs to sensor.
Bump bonding at small pitches not industry standard – requires large production quantities
Complicates prototyping relative to bump bonding, which can be done in lab.

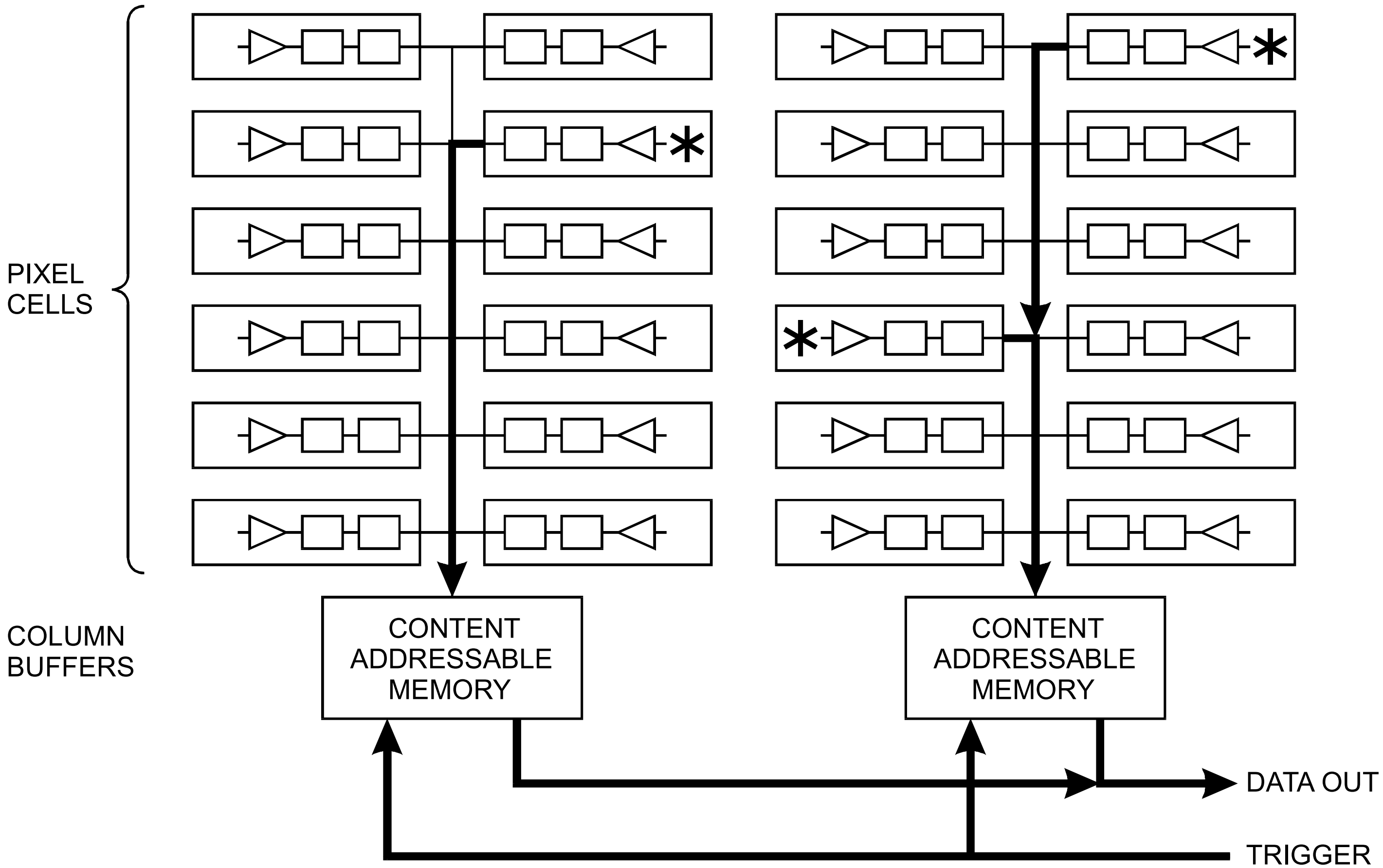
ATLAS Pixel Cell



0.25 μm CMOS, $Q_n \approx 170$ e

40 μW per cell; total power for 2880 pixels: 200 mW (incl. peripheral circuitry)

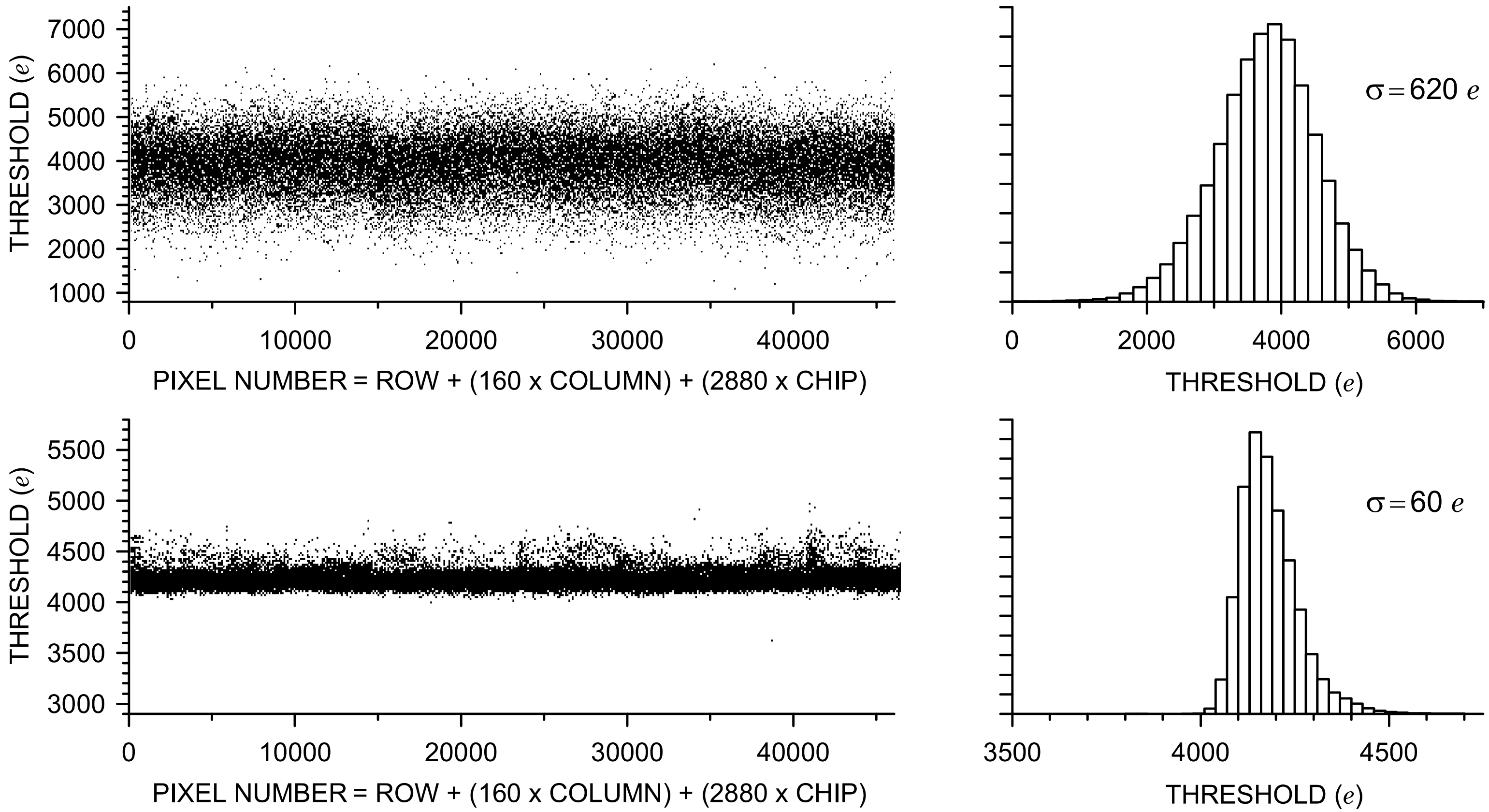
Readout Scheme



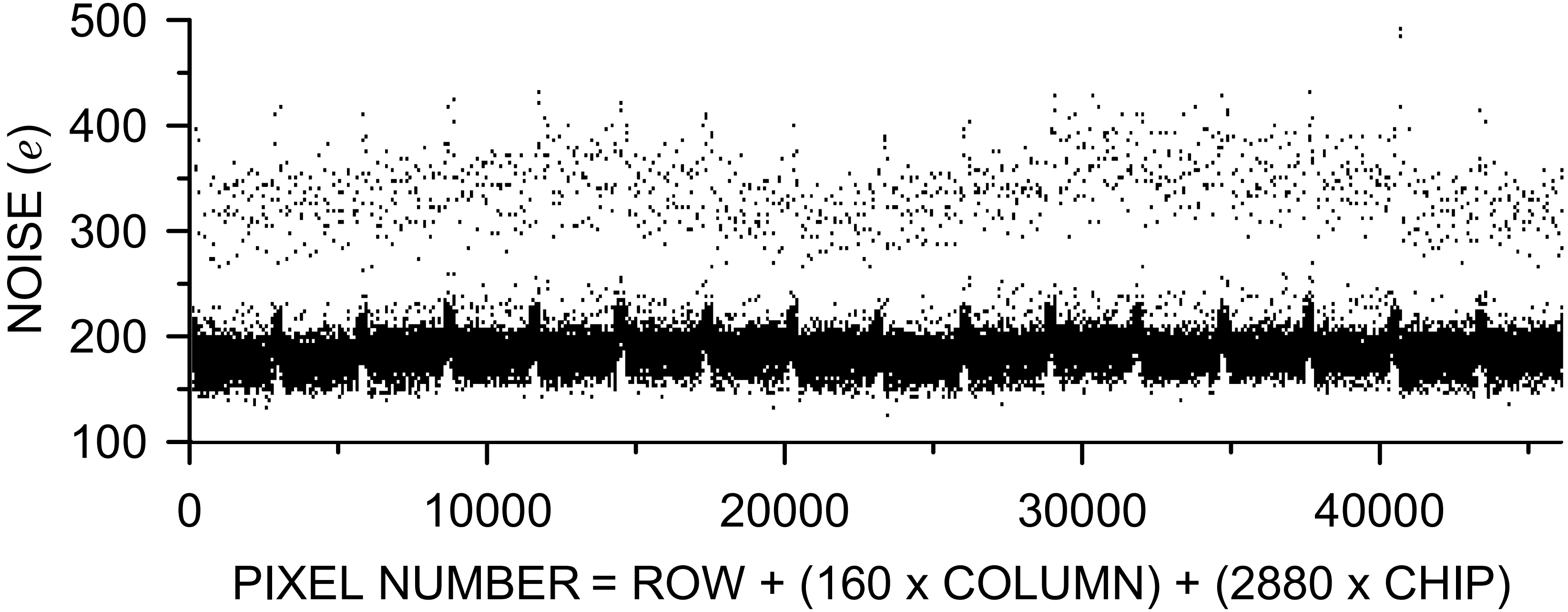
Pixels continuously active, but don't send signals until struck (self-triggered).
Time stamp for struck pixels stored immediately in Content Addressable Memory
Data stored in pixel until Level 1 trigger received for stored time stamp.

Threshold dispersion must be smaller than noise.
Small feature sizes $\Rightarrow$ large threshold dispersion $\Rightarrow$ correct with trim DAC

Threshold dispersion before and after trimming



Noise Distribution



Three groups visible: 1. nominal pixels

2. Extended pixels that bridge columns between ICs (spikes every 2880 pixels)

3. Ganged pixels to bridge rows between ICs

Where are we Going?

ILC: μm position resolution in vertex detector (1 – 5 μm)

$\Rightarrow$ ~20 μm pixels

Jet (multi-track) resolution

Minimal mass

$\Rightarrow$ monolithic pixel devices

(CCDs, MAPs, DEPFETs, multi-tier ICs?)

$\Rightarrow$ low-mass power distribution, cooling

sLHC: 10-fold luminosity

$\Rightarrow$ radiation hardness limited primarily by sensor

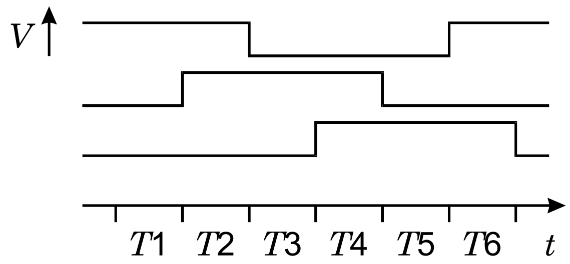
Charge trapping in the sensor $\Rightarrow$ reduced signal

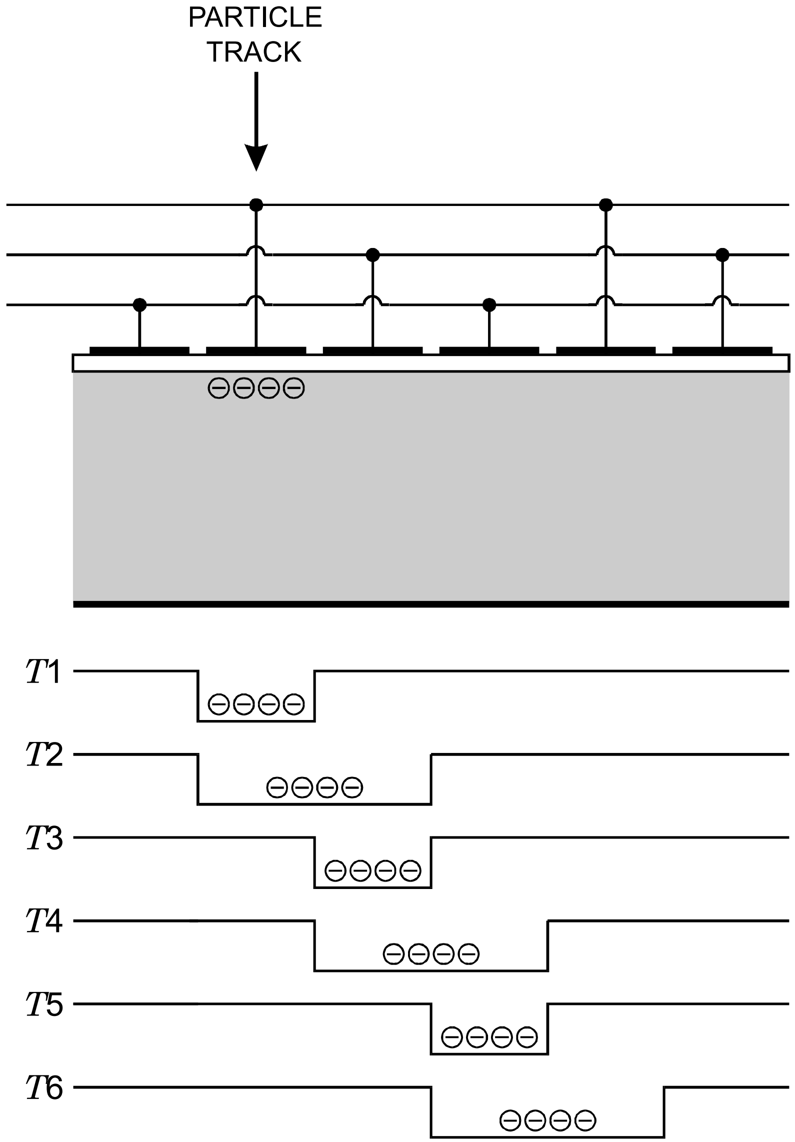
Hybrid pixels allow separate optimization of sensor material and readout,

but at the expense material and cost.

2. Charge Coupled Devices (CCDs)

CCD Principle

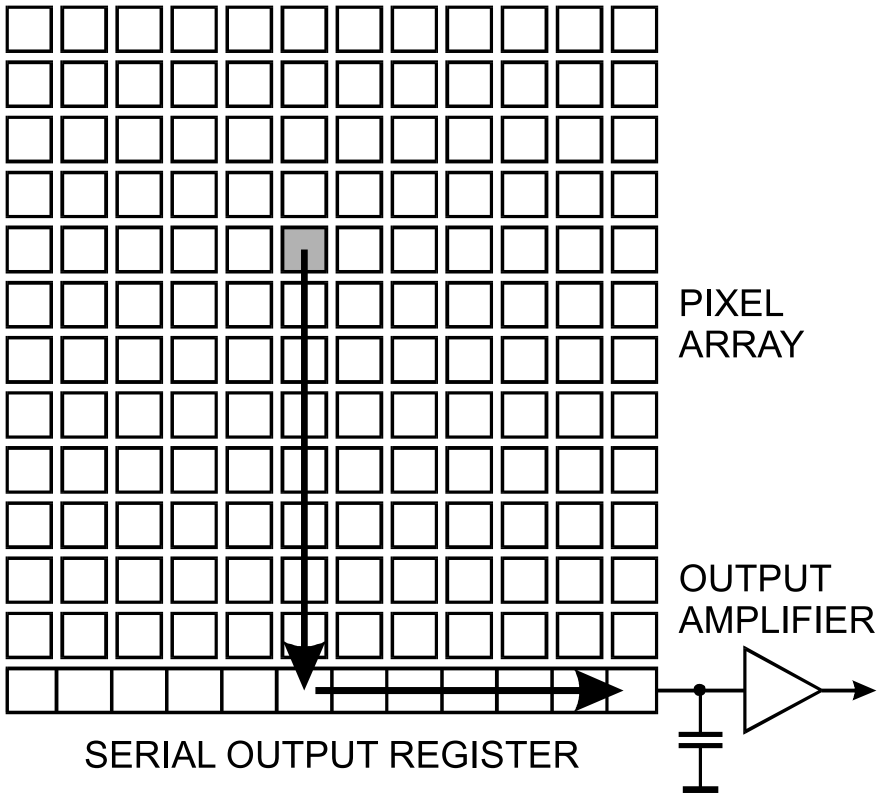




Voltage applied to individual electrodes forms potential wells that collect electrons.

Sequentially applying pulses transports electron buckets from one pixel to the next.

CCD Readout



Sequential readout requires that some charge buckets have to traverse complete array.

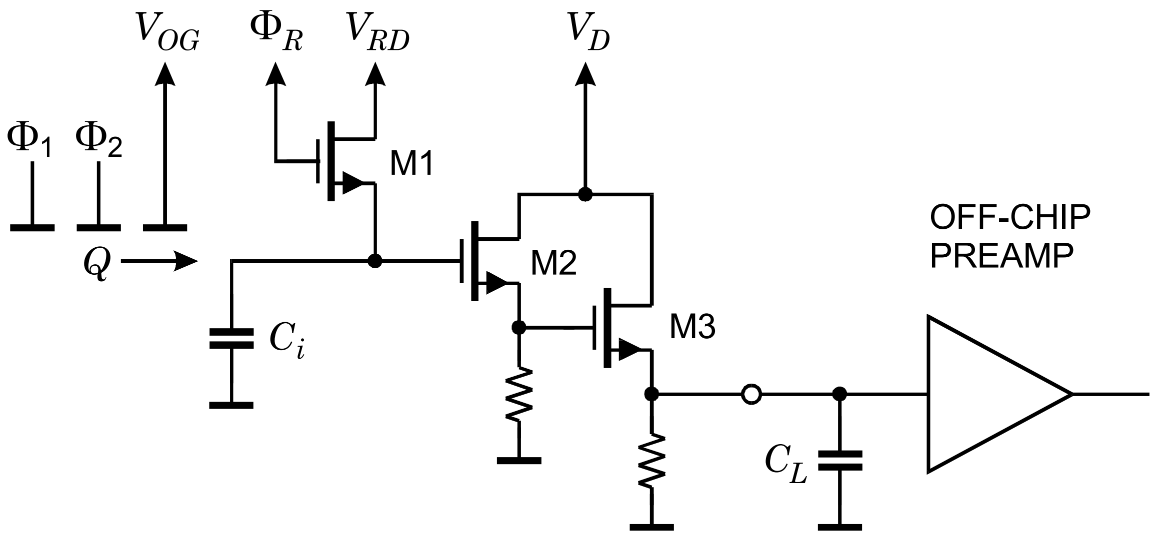
Requires extremely high transfer efficiency – achieved in practice!

Long readout times: $T = N_{col} N_{row} T_{clock}$ (e.g. 200 ms in VXD3)

Clock rates typ. 5 – 10 MHz, but 50 MHz in ILC prototype designs

Advanced designs have one readout amplifier per column to speed up readout.

Typical on-chip readout amplifier



Circuit in VXD3 vertex detector in SLD – Equivalent Noise Charge ~100 e.

Utilize correlated double sampling

CCDs cooled to achieve low noise and high transfer efficiency: VXD3 operated at 200K

Charge collected from 20 μm depth, so 20 μm pixels yield 20 $(\mu m)^3$ space points

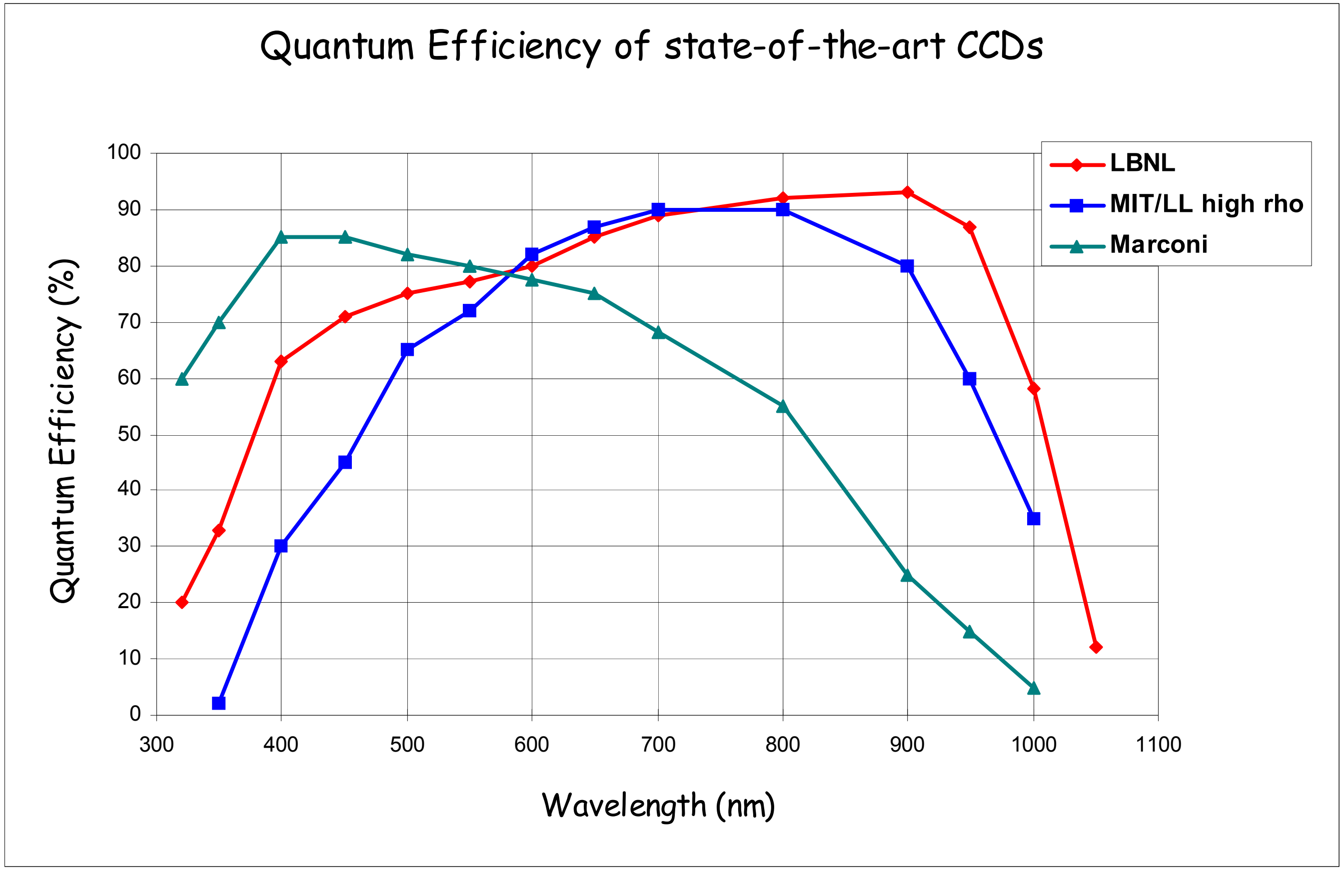
Large arrays: e.g. 80 x 16 mm^2 in VXD3. Larger arrays now available.

CCDs for Astronomical Imaging

Astronomy requires long exposure times (up to 100s of s)

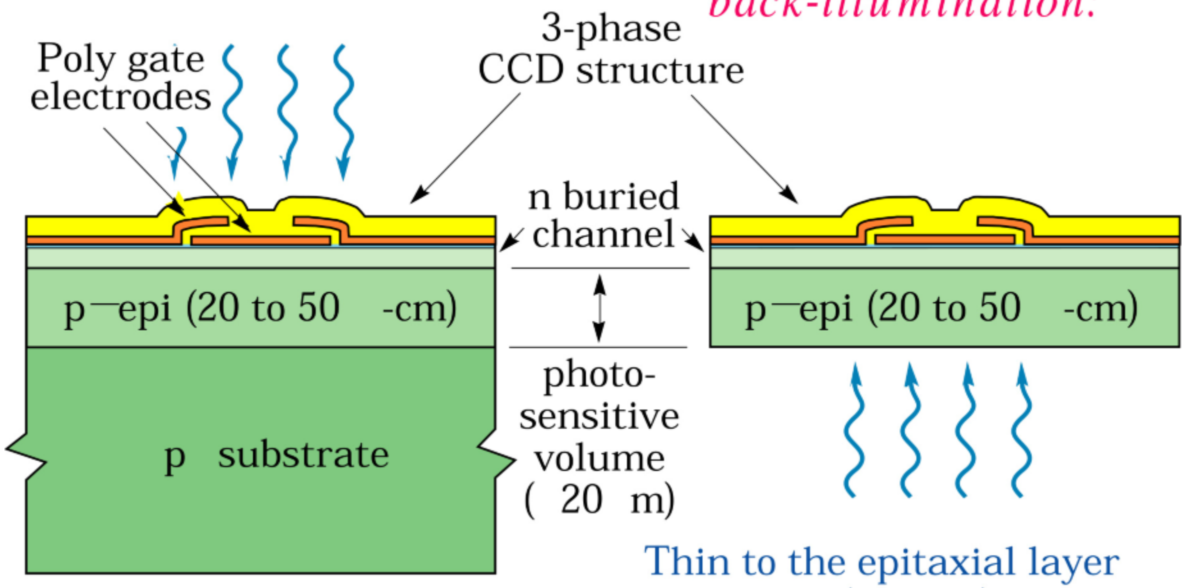
Single photon sensitivity requires extremely high transfer efficiency

Much larger signals in HEP or conventional imaging (digital cameras) fill traps.



Conventional CCD Structure

Front-illuminated CCD: *Thinned CCD with back-illumination:*



Thin to the epitaxial layer thickness (20 m)

Drawbacks:

1) Poor blue response due to absorption in polysilicon gate electrodes
2) Poor near-IR response due to thinness of the epitaxial layer
3) Interference patterns due to gate structure

Drawbacks:

1) Thinning is difficult and expensive
2) Poor near-IR response
3) Interference (fringing)
4) Lateral diffusion in field-free region (degraded PSF)

Fully Depleted CCD
(S.E. Holland, LBNL)

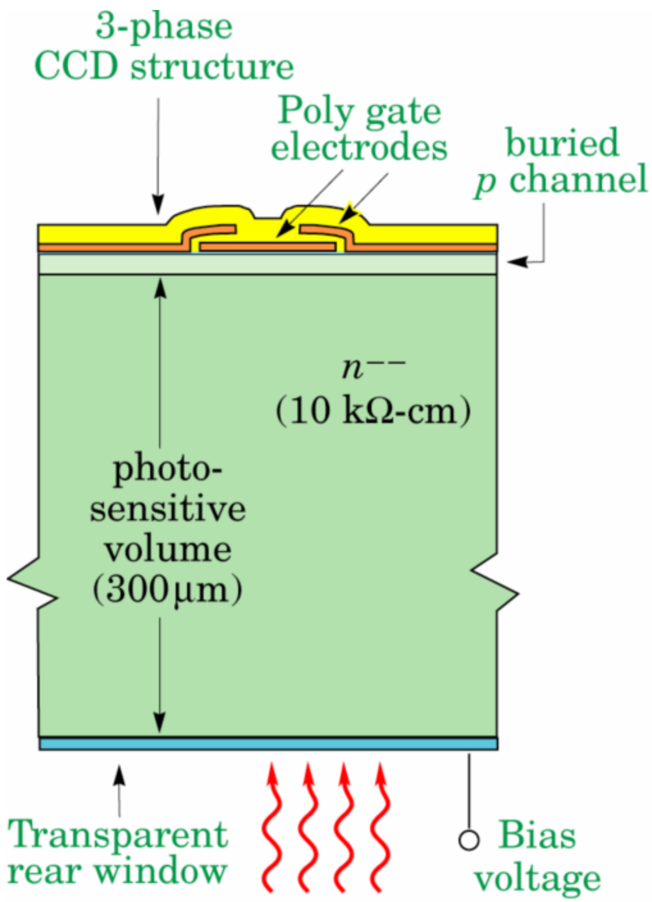
- high resistivity n-type substrate,
  fully depleted

- backside illumination

- transparent window with
  antireflection coating
  thin for good blue response

- 300 μm active thickness
  $\Rightarrow$ good QE up to λ= 1 μm

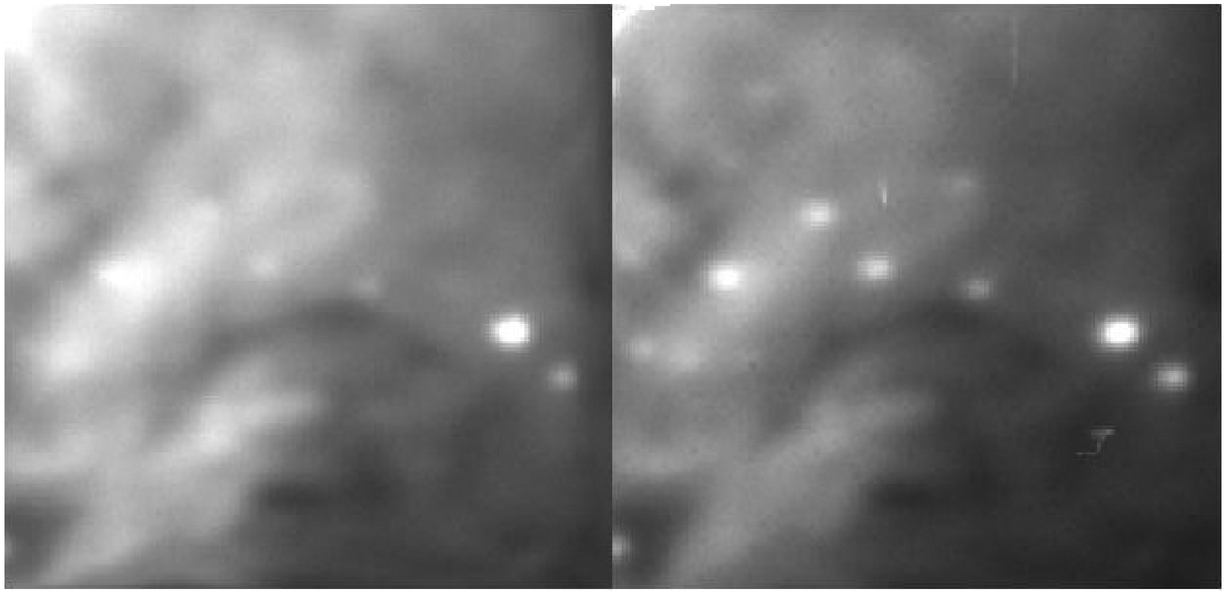
- no costly thinning of devices



Comparison between thinned CCD (bottom) and deep depletion device.

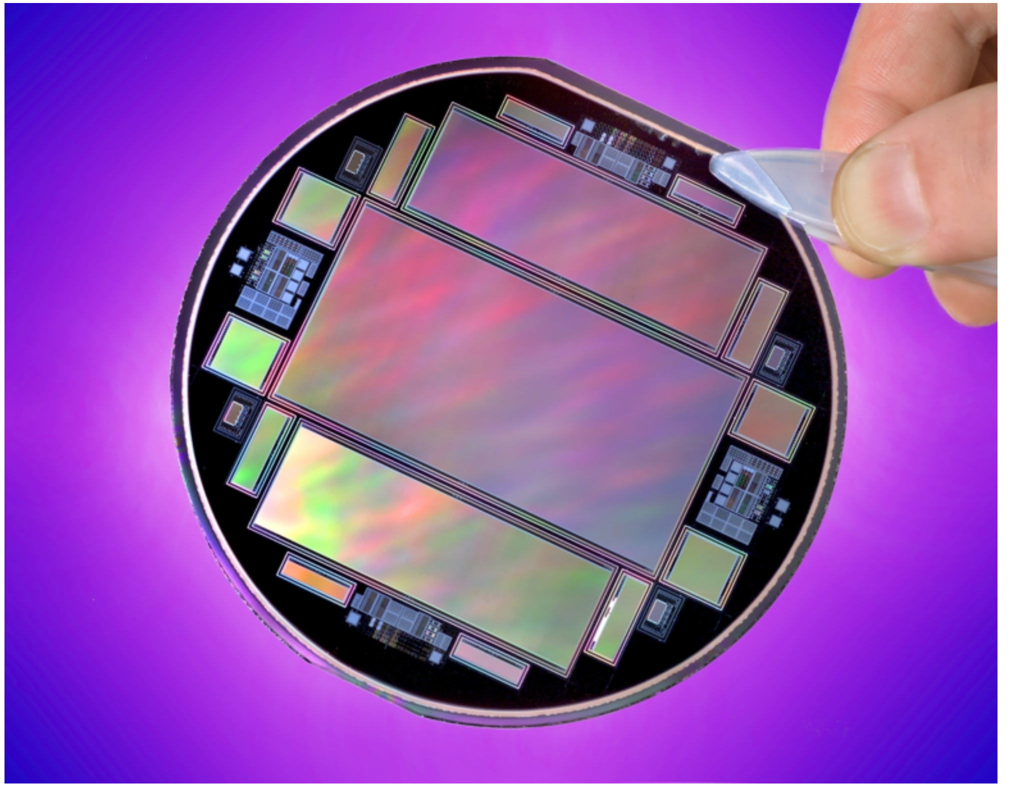
Interstellar dust tends to absorb in the blue, so extended red response of LBNL CCD shows features obscured in thinned CCDs.

“Conventional” thinned CCD Deep Depletion CCD



Lick 1m telescope, 4-Dec-1996

100 mm diameter wafer
fabricated at LBNL



includes

2K x 4K (15 μm pixels),

1.5K x 4.8K (10.5 μm pixels)

1.3K x 4.2K (12 μm pixels)

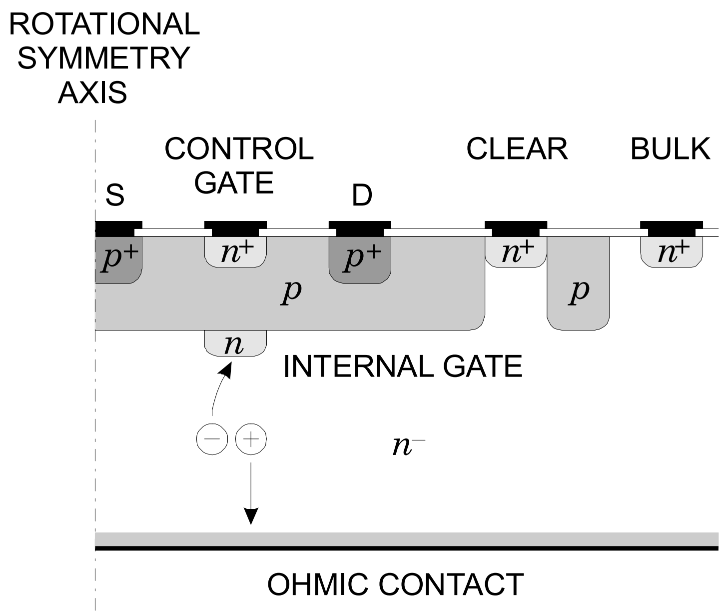
+ test structures

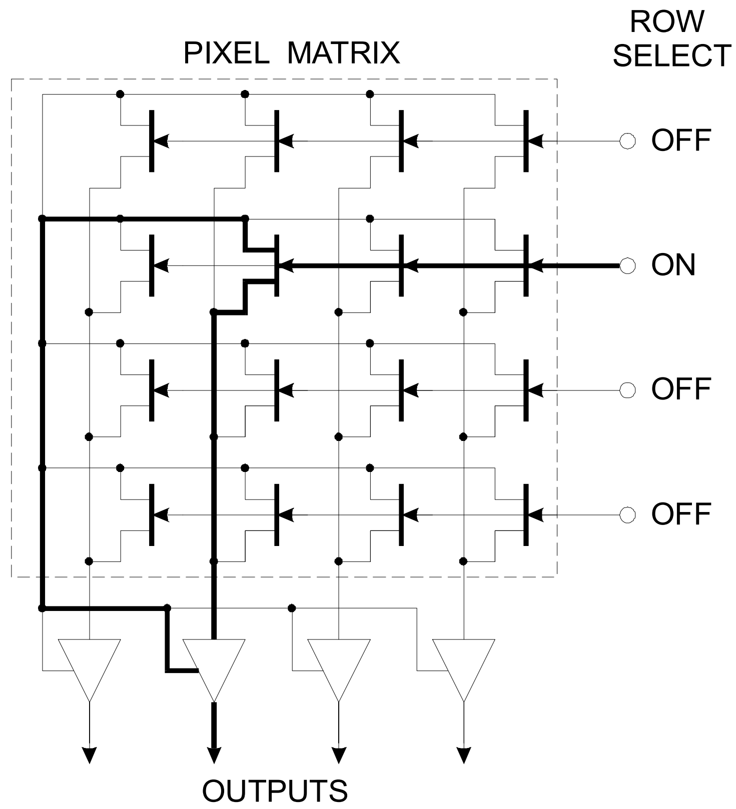
current fab runs on 150 mm wafers.

For more information see http://snap.lbl.gov

3. DEPFET Arrays

A variation on the CCD is the DEPFET array, which implements a transistor in each pixel.





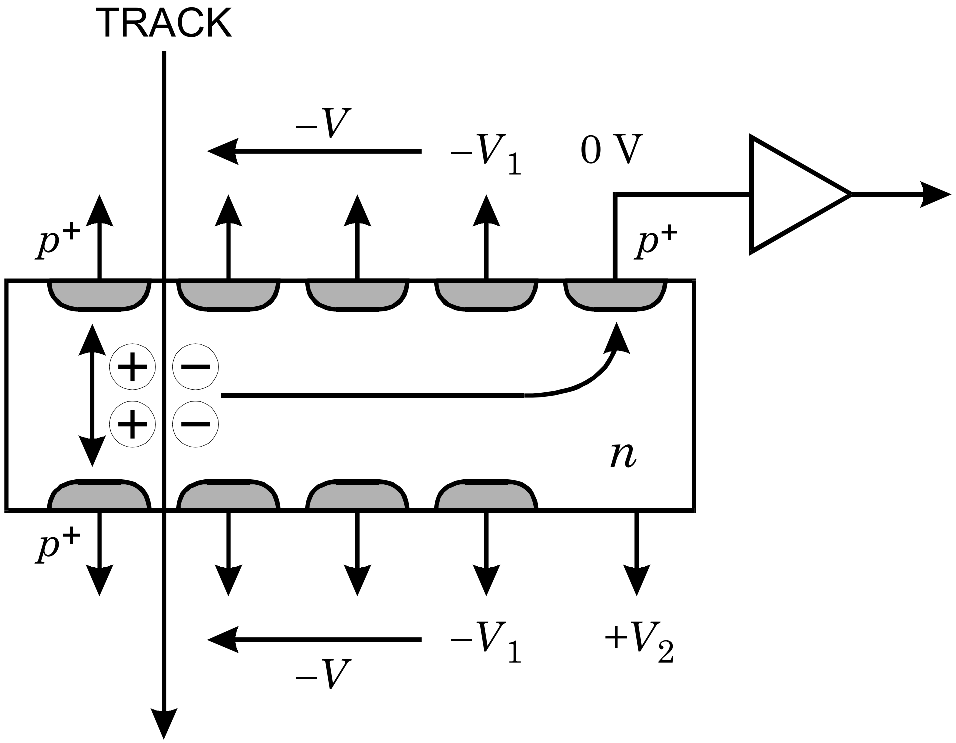
Charge is collected on the internal gate of the transistor. Reduced node capacitance is cited as an advantage, but the transistors are inferior to modern CMOS, so noise is about the same as in CCDs.

Sequential readout as in CCDs, but the selective readout of a portion of the array is possible.

See papers by G. Lutz *et al.* (MPI Munich) and N. Wermes *et al.* (Univ. Bonn) for more details

4. Silicon Drift Chamber

A TPC structure implemented in silicon:



Silicon is depleted from both surfaces to form a potential well in the middle.

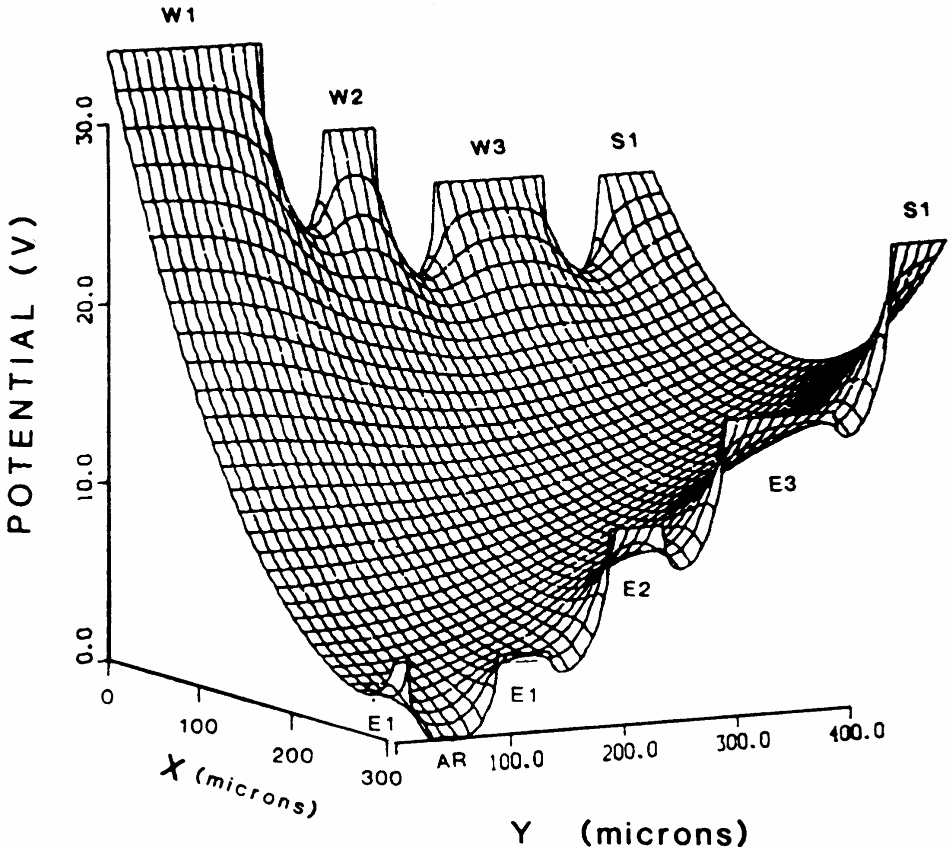
A longitudinal field draws the electrons to the readout electrode at the far end.

The potential trough is skewed to direct charge to a readout electrode on the surface.

Silicon drift chamber has advantage that the collection electrode is decoupled from the large acceptance area.

⇒ capacitance can be very small, even on a large area detector
(C~ 50 – 100 fF for A= 10 cm^2)

⇒ ~ 10 μm resolution over 5 – 10 cm drift distance



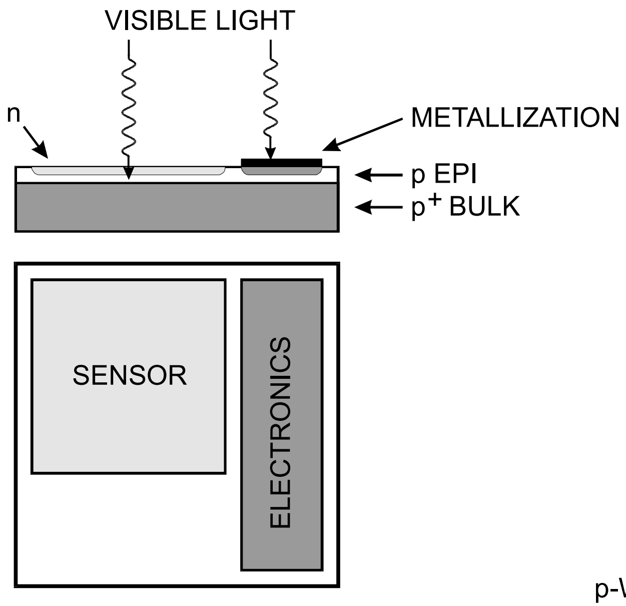
(from Gatti et al. IEEE Trans. Nucl. Sci. **NS-32** (1985) 1204)

Drift velocity must be predictable.
Trapping must be low for long drift distances (~ cm) ⇒ problem with radiation damage.

Although originally proposed as a position sensing device, an important application is in a low-noise x-ray detector or photodiode.

Next-Generation Pixel Devices

5. Monolithic Active Pixel Sensors (MAPS)

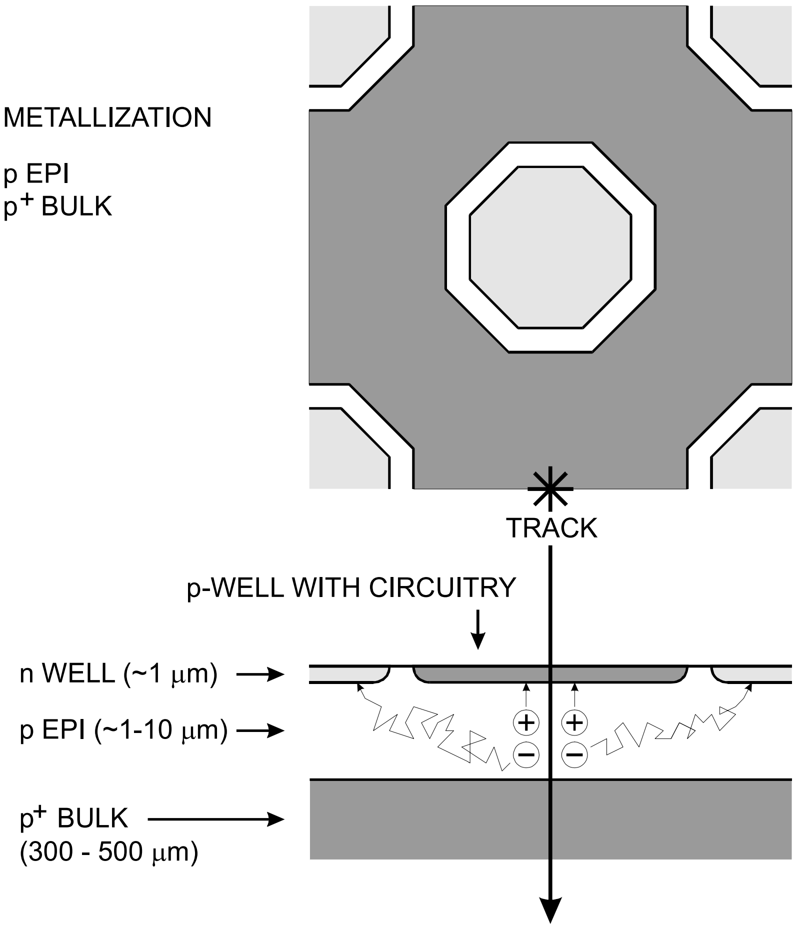


Utilize epi layer of “standard” CMOS as sensor

Charge collection by diffusion ⇒

limits speed, radiation resistance

OK for ILC

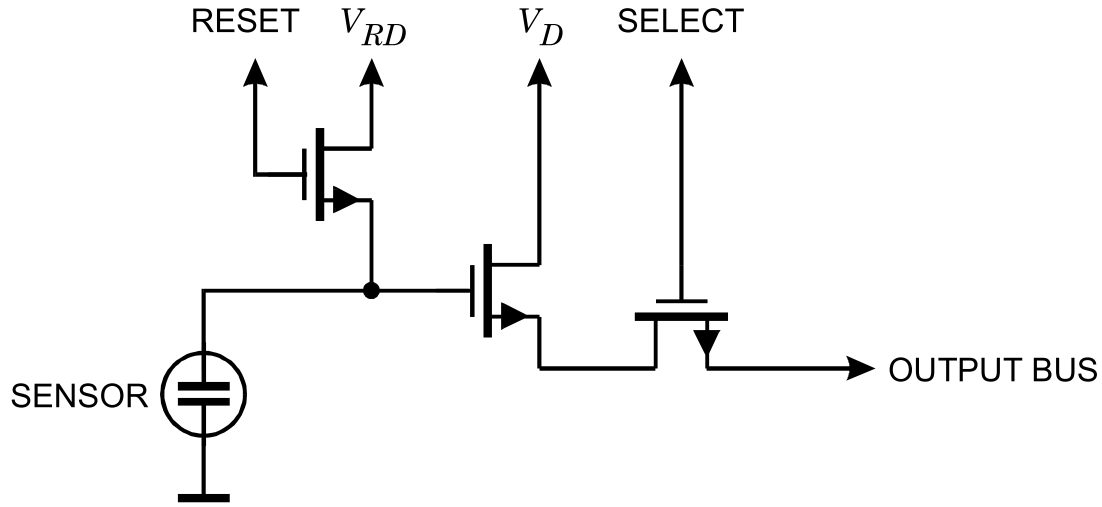


Designs with ~90% active area per IC

Chips can be thinned to ~50 µm to reduce material. (Battaglia et al.)

Chips limited to 10 – 20 mm size, so many required to cover large area.

Simple MAPS Output Circuit



Some designs implement correlated double sampling on each pixel.

Requires that all pixels be read out, so readout time extends over many beam crossings. Frame rate determines shot noise contribution to Q_n.

Reduce readout time: Full processing chain (preamp, shaper, comparator) required to implement on-chip sparsification.

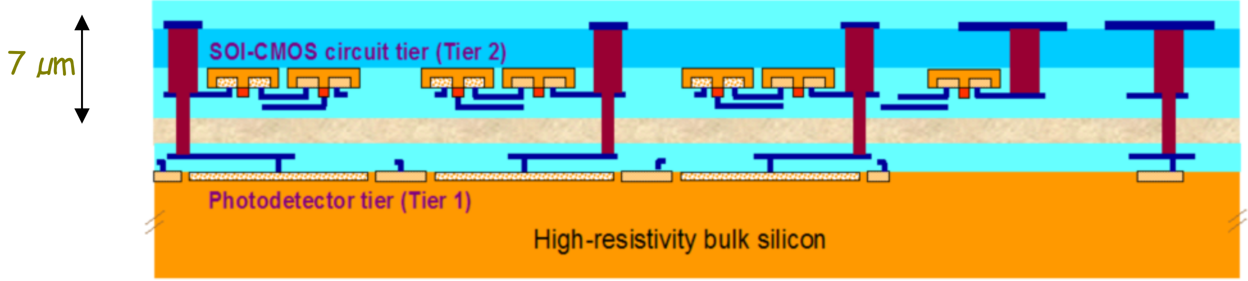
Some new designs include threshold discrimination per pixel:
0.13 μm CMOS, 25 μm pixel, but threshold dispersion ≈ elec. noise.

6. Multi-Tier Electronics (aka “SOI” or “3D”)

CMOS Circuitry

Isolation Oxide

Sensor Layer

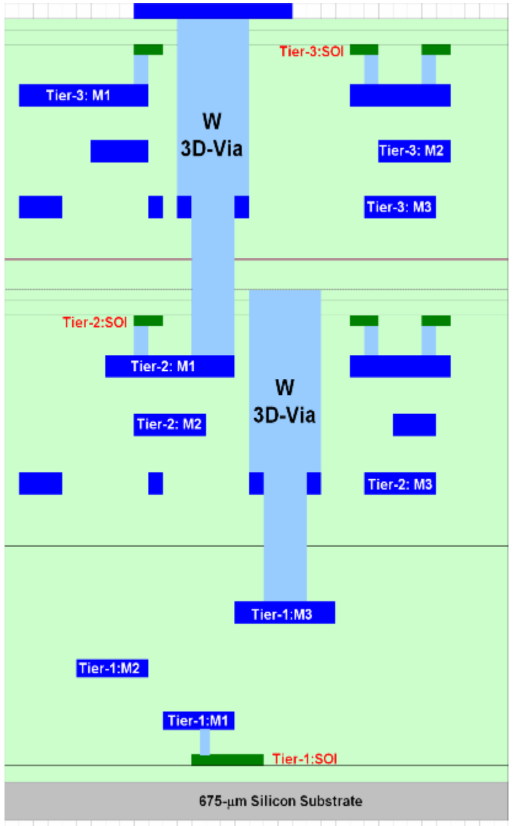


MIT Lincoln Lab

3-Tier Design (FNAL)

3 transistor levels
11 metal layers

Accommodate additional circuitry for given pixel size.



(R. Lipton, STD6)

Test Chips designed at KEK (Arai et al.)

Fabricated by OKI

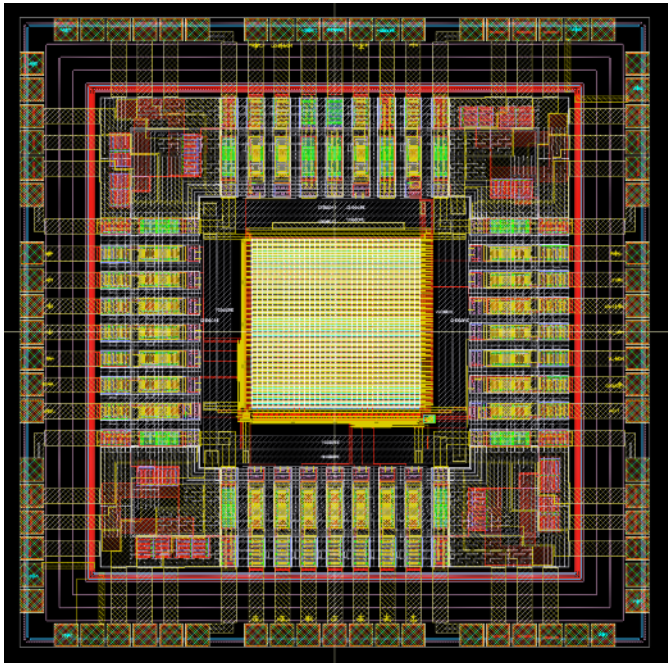
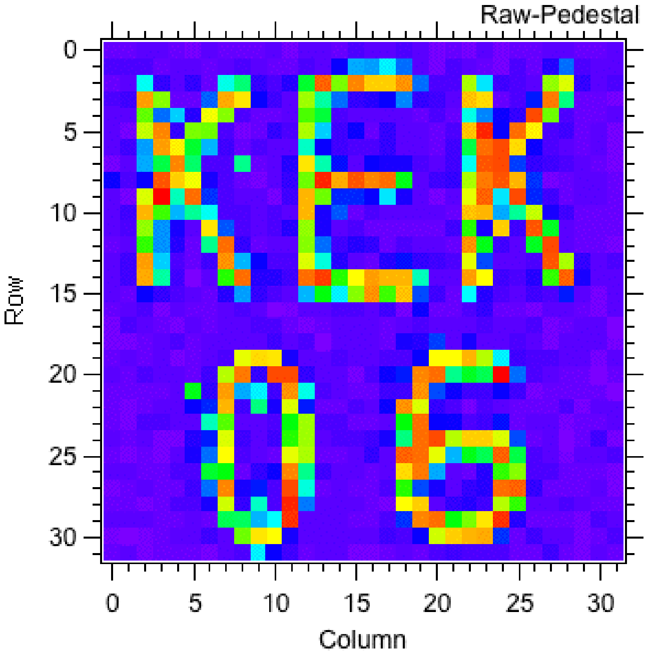


Image (20 μm pixels)



High resistivity substrate (1 kΩ cm CZ) thinned to 350 μm.
(see talk T6.9 by Tsuboyama et al.)

Radiation resistance of sensor layer in industrial processes inadequate for SLHC, but suitable for ILC.

Summary

Both ILC and SLHC drive developments towards higher levels of segmentation.

ILC: Micron-resolution pixel detectors for vertexing.
Material even more critical than at LHC

Candidates: CCDs, MAPS, DEPFETs

CCDs and DEPFETs fabricated as large area devices
CCDs available commercially
DEPFETS local MPI Munich development

MAPS require integration of many small devices
additional mass in mounting + cooling

Multi-Tier structures offer better controlled charge collection, but much R&D necessary.

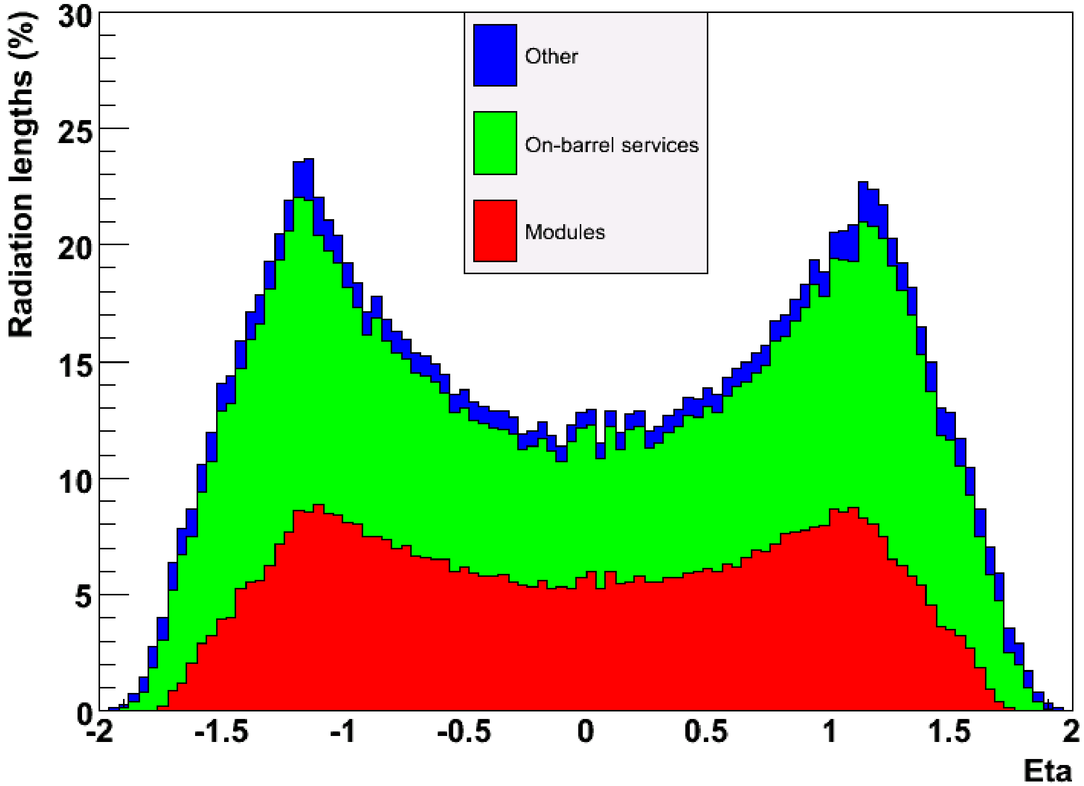
sLHC: Increased radiation resistance required:
$\Rightarrow$ short strips and hybrid pixel detectors

Challenge: reduce power dissipation and material

Sobering Reminder: Material in ATLAS Silicon Tracker Barrel

Total material per layer:
 3% X_0.

Half is services:
 cooling
 cabling
 carbon fiber support



(see http://www.hep.phy.cam.ac.uk/~cpw1/atlas.html)

ATLAS Pixel Detector:	Total (3 layers)	10.7% X_0
	Hybrids + Cables	1.3% X_0
	Support + Cooling	6.9% X_0

Can we do better?