IV. Detector Systems – Conflicts and Compromises

Conflicts

Custom integrated circuits essential for vertex detectors in HEP.

Requirements

1. low mass to reduce scattering
2. low noise
3. fast response
4. low power
5. radiation tolerance

reduction in mass ⇒ thin detector

radiation tolerance ⇒ thin detector

thin detector ⇒ less signal ⇒ lower noise required

lower noise ⇒ increased power

fast response ⇒ increased power

increased power ⇒ more mass in cabling + cooling

immunity to external pickup ⇒ shielding ⇒ mass

+ contain costs

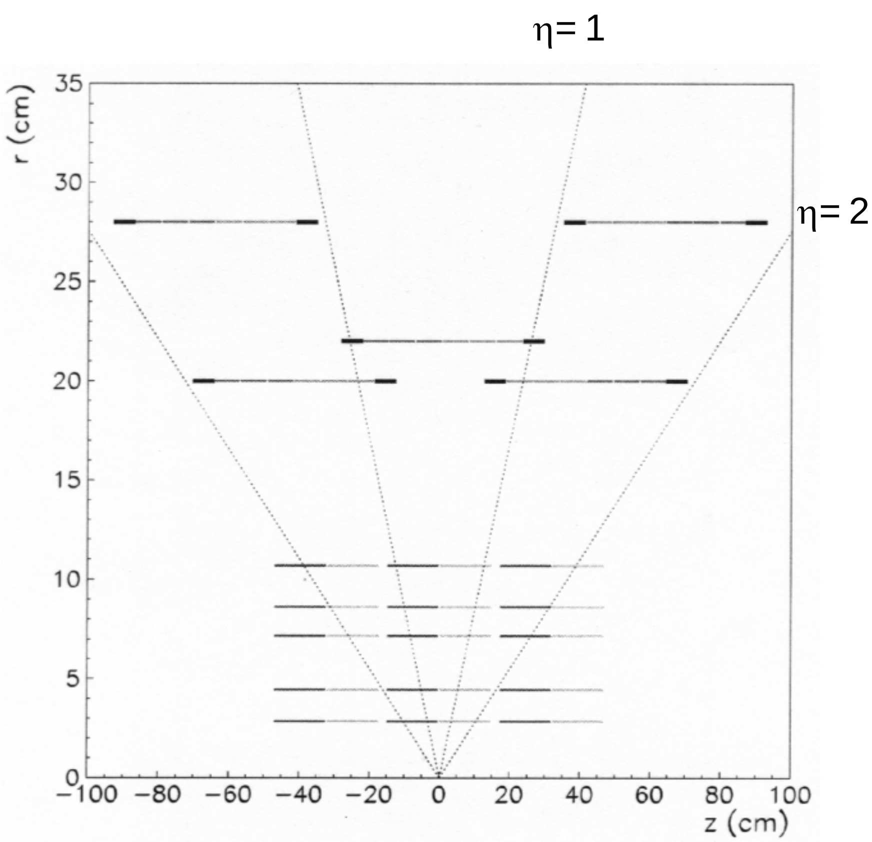
How to deal with these conflicting requirements?

Some examples ...

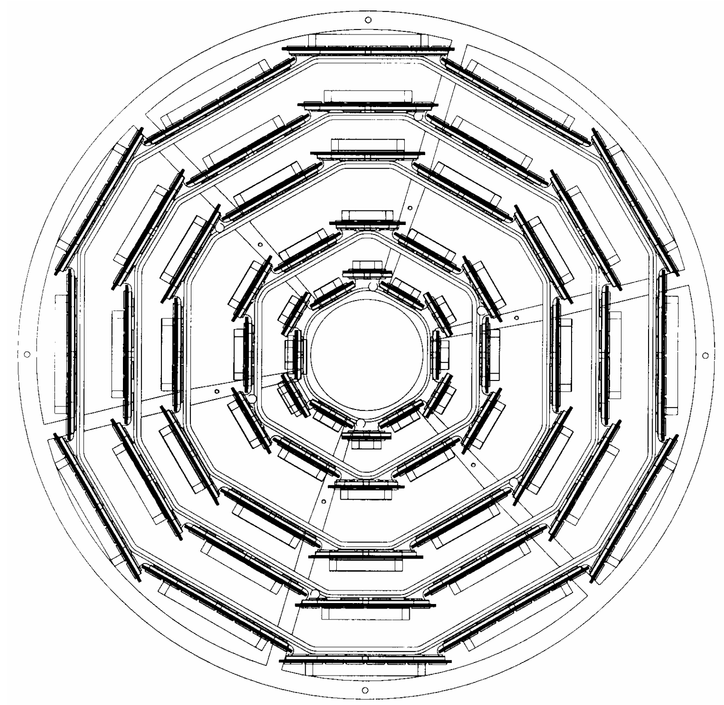
2. CDF Vertex Detector Upgrade: SVX2

Expand coverage of existing vertex detector

a) side view (z = beam axis)



b) axial view of vertex detector



Property	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4
Radial distance (cm)	2.45	4.67	7.02	8.72	10.6
Stereo angle (degrees)	90	90	+1.2	90	-1.2
$r\phi/z$ readout channels	256/512	384/576	640/640	768/512	896/896
$r\phi/z$ readout chips	2/2	3/3	5/5	6/4	7/7
$r\phi/z$ strip pitch (μm)	60/141	62/125.5	60/60	60/141	65/65
Total width (mm)	17.14	25.59	40.30	47.86	60.17
Total length (mm)	74.3	74.3	74.3	74.3	74.3

Layers 0, 1 and 3 use 90° stereo angle, whereas layers 4 and 5 use 1.2° stereo angle to reduce ghosting.

Electronic Readout

SVX2 uses the SVX3 chip, which is a further development of the SVX2 chip used by D∅.

Include on-chip digitization of analog signal

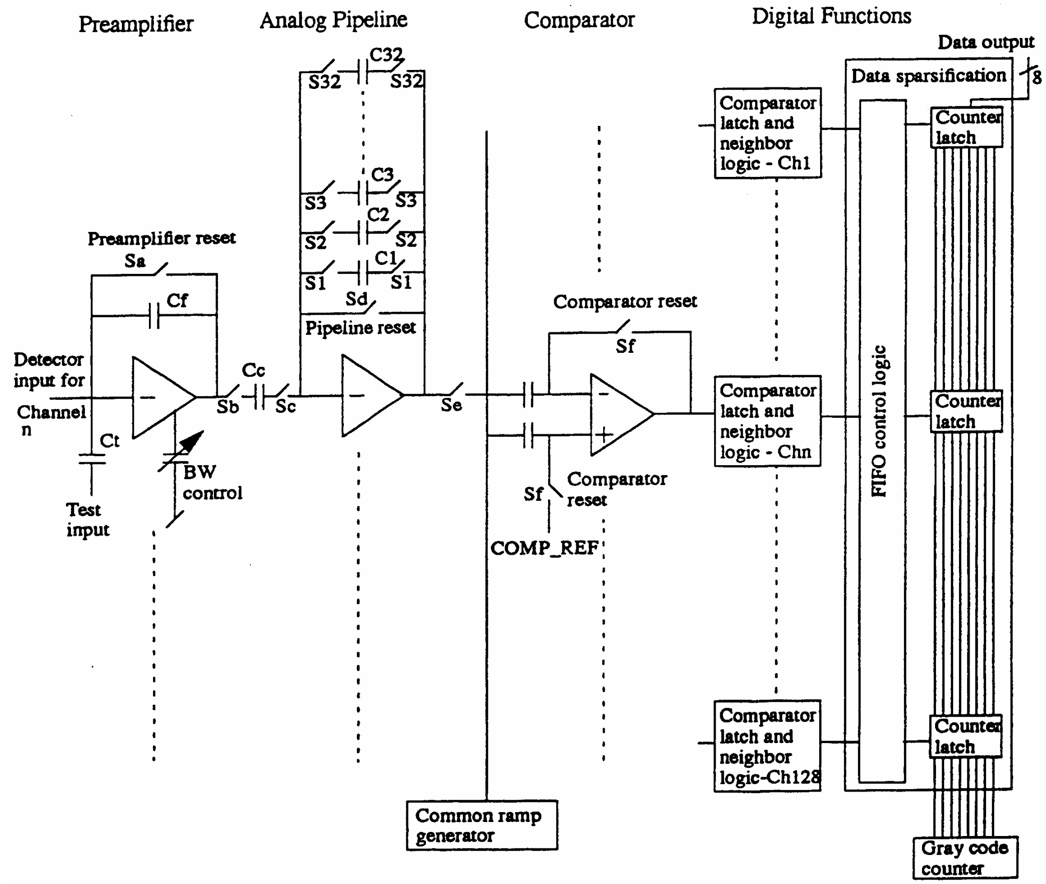
Threshold, calibration via on-chip DACs

All communication to and from chip via digital bus

Wilkinson ADC integrated with pipeline + comparator, which is also used for sparsification. Adds 100 µm to length and 300 µW/ch power.

ADC clock runs at 106 MHz in experiment, tested to 400 MHz

Total power: 3 mW/ch



SVX2 die layout

Dimensions: 6.3 x 8.7 mm 0.8 µm, triple-metal rad-hard CMOS

Input Pads

Preamplifiers

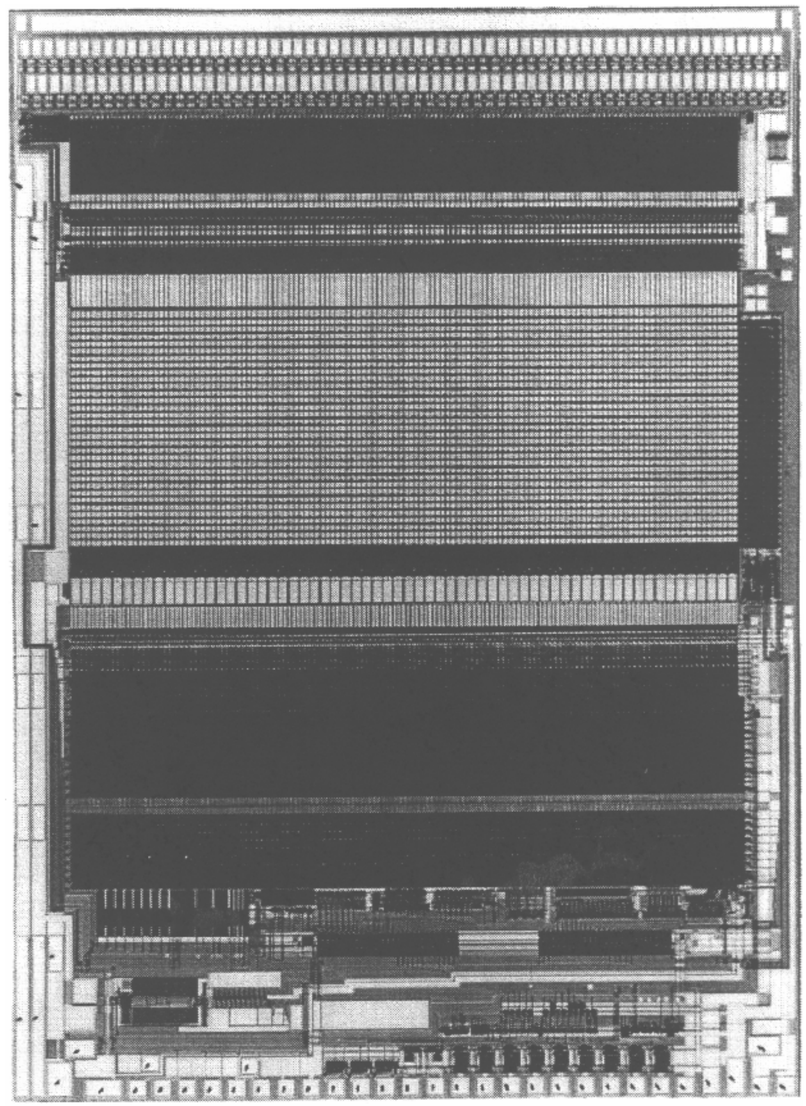
Analog Pipeline

ADC Comparator

Neighbor Logic

Sparsification +
Readout

ADC Ramp +
Counter, I/O



SVX2 (used by D∅) is designed for sequential signal acquisition and readout.

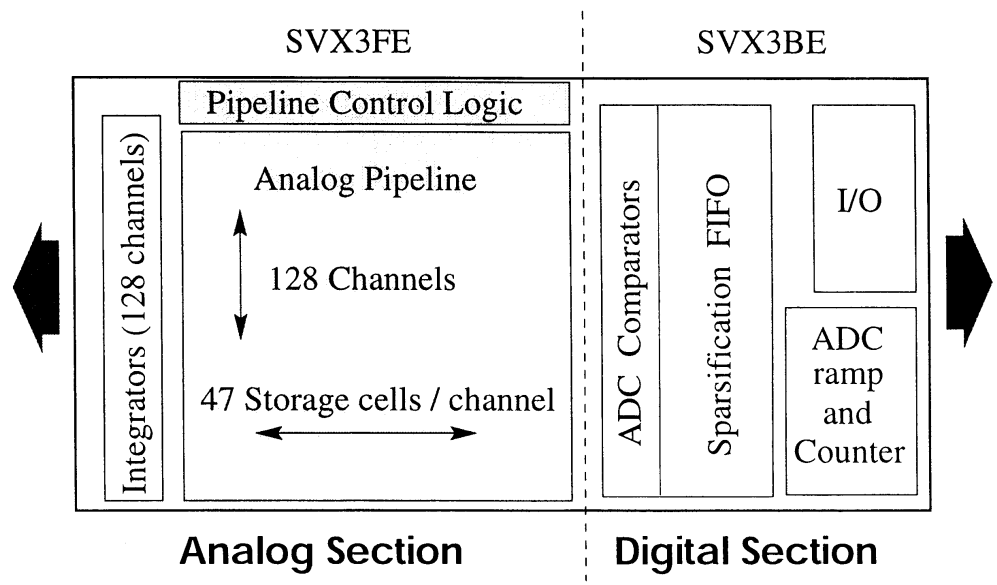
SVX3 (used by CDF) allows concurrent read-write, i.e. signal acquisition and readout can proceed concurrently.

SVX3 Floor Plan

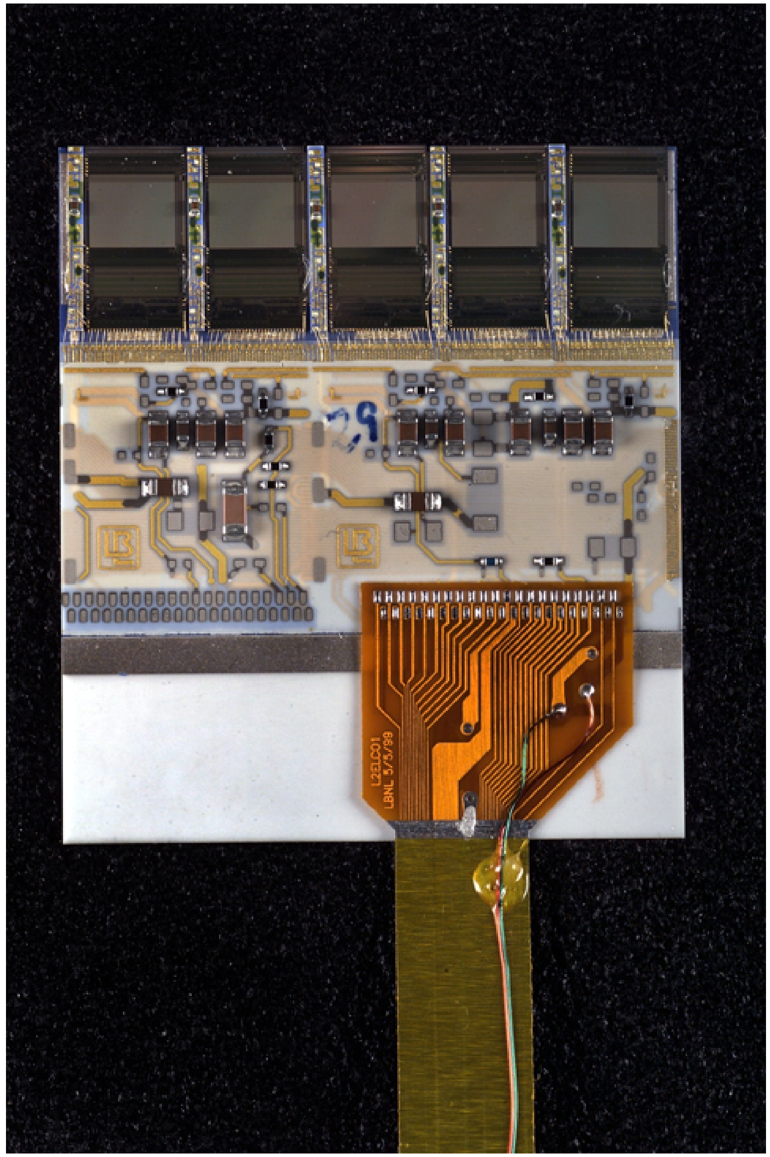
Measured Noise:

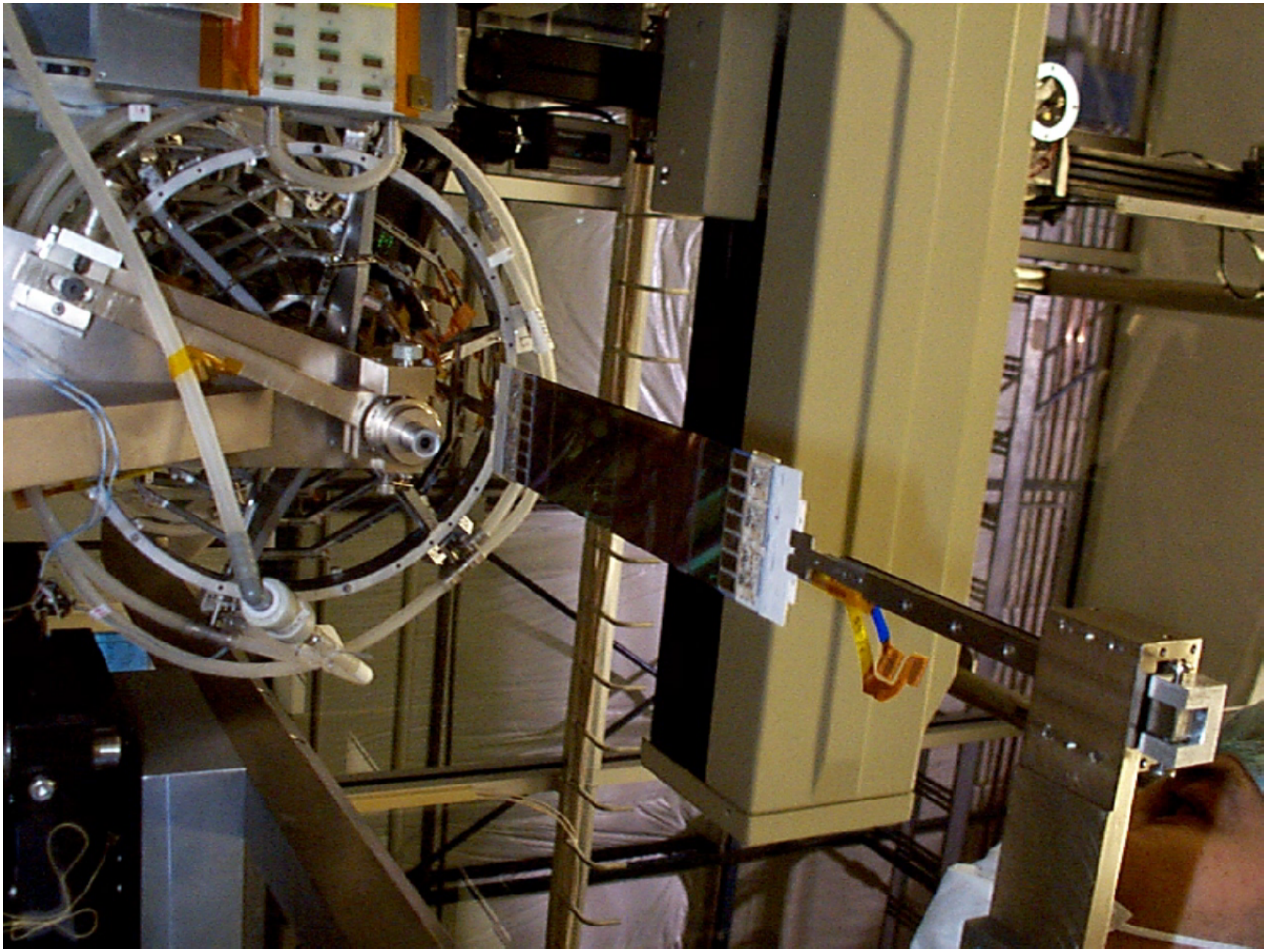
Q_n= 500 el + 60 el/pF rms

Both chips fabricated in rad-hard CMOS.



Analog section: 6.26 x 8.06 mm^2 Digital section: 6.26 x 4.97 mm^2
Combined in 1 chip: 6.26 x 12 mm^2





SVX2 and SVX3 utilize correlated double sampling for pulse shaping

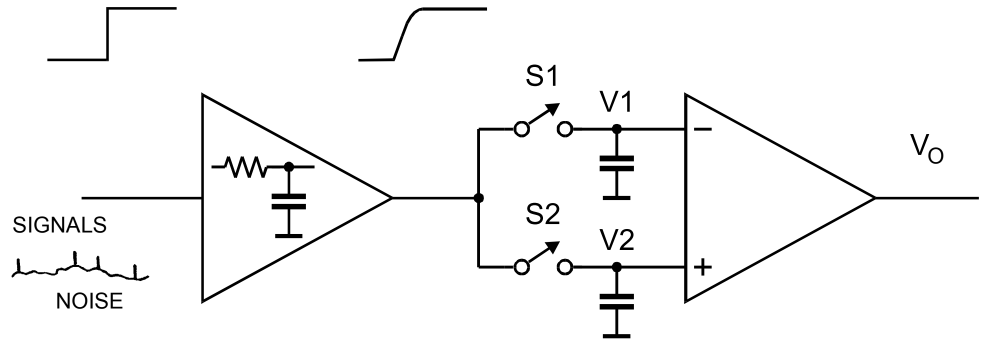
(see Signal Processing 1)

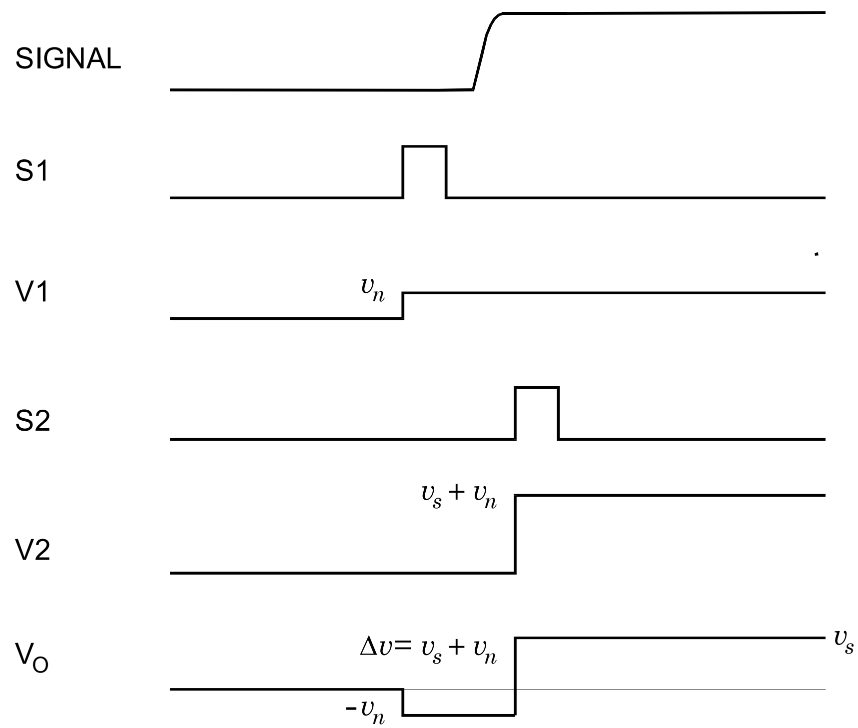
Correlated double sampling requires prior knowledge of signal arrival.

OK for colliders if $\Delta T_{beam} > T_{shaper}$, but not for random signals.

High luminosity colliders (B Factories, LHC) have much shorter beam crossing intervals

$\Rightarrow$ continuous shaping required





3. BaBar Silicon Vertex Tracker

B mesons from Υ(4S) production have low momentum.

Asymmetry in beam energies (9 GeV e^- on 3.1 GeV e^+) used to provide boost ($\beta\gamma$ = 0.56) that allows conventional vertex detectors to cope with short B meson lifetime.

Vertex detector must provide resolution in boost direction, i.e. parallel to beam axis, rather than in $r\varphi$.

Resolution requirement not stringent:

> Less than 10% loss in precision in the asymmetry measurement if the separation of the B vertices is measured with a resolution of ½ the mean separation (250 μm at PEPII)

⇒ 80 μm vertex resolution required for both CP eigenstates and tagging final states.

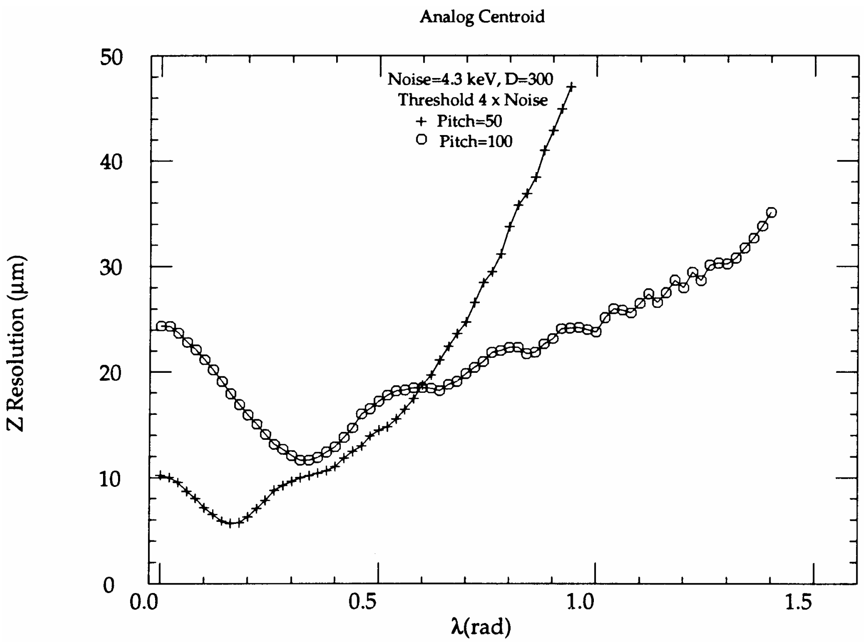
Resolution is multiple-scattering limited: beam pipe: 0.6% X_0

Use crossed strips: z-strips for vertex resolution
$r\varphi$ strips for pattern recognition

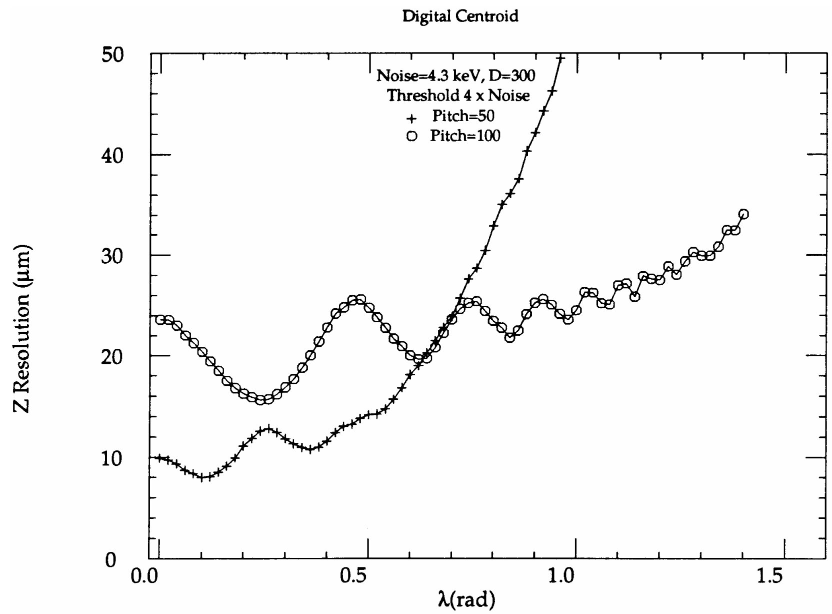
Measurement does not require utmost position resolution ⇒ use binary readout

Position resolution for analog and binary readout vs dip angle λ.

Analog readout (50 and 100 µm pitch)



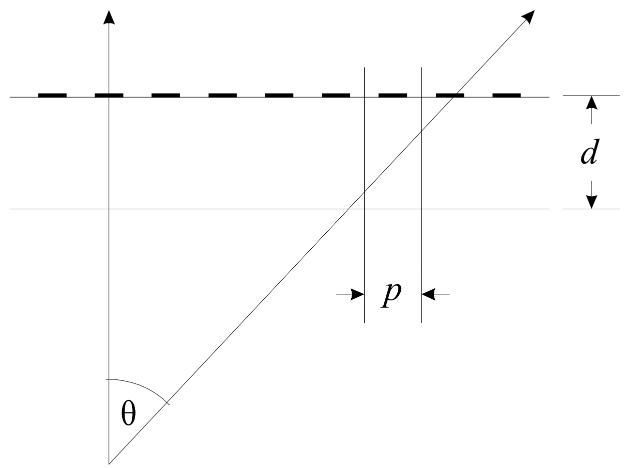
Binary readout (50 and 100 µm pitch)



Why does 100 µm pitch yield better resolution at large dip angles?

Signal in z-strips degrades at large dip angles

$$Q_s = d\,\frac{dE}{dx} \qquad\qquad Q_s = p\cos\Theta \cdot \frac{dE}{dx}$$



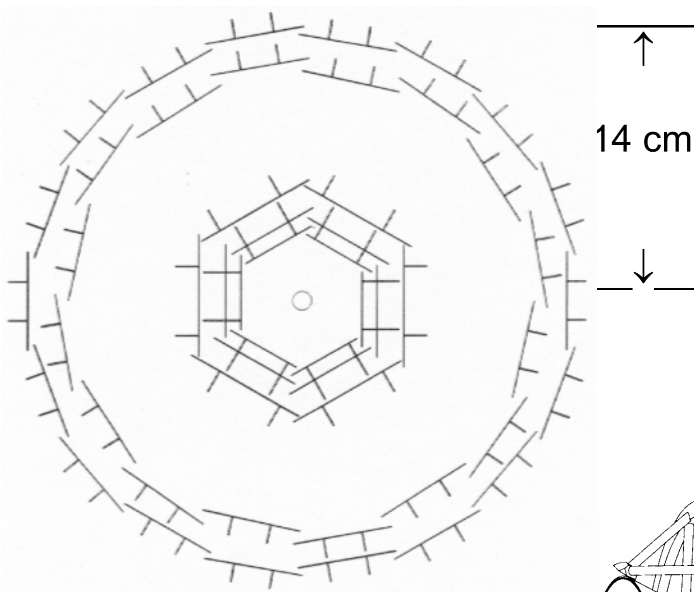
Change strip pitch at $\lambda > 0.7$ radians

Furthermore ….

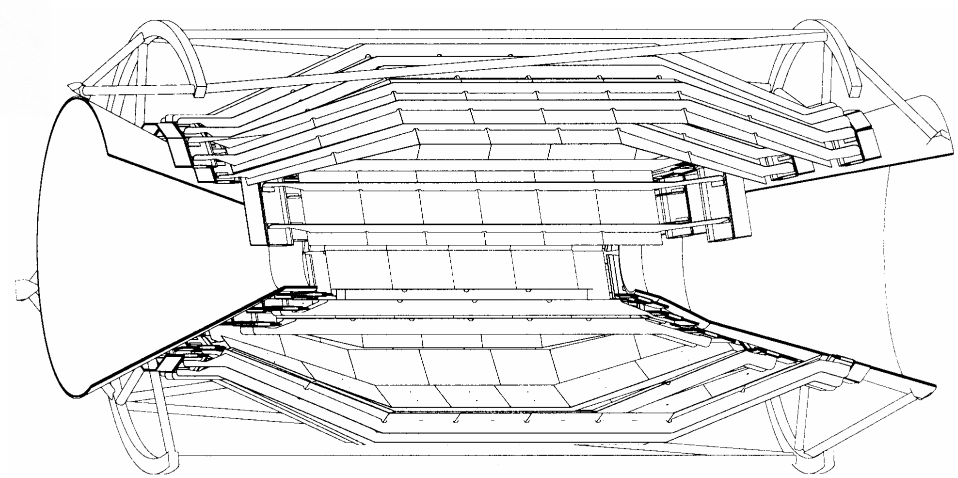
add coarse analog information (3 – 4 bits adequate)

Mechanical arrangement of detector

Axial view

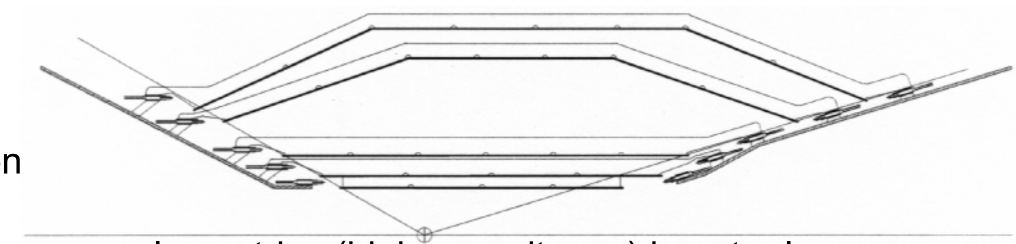


Side view



Outer layers use “lampshade” geometry instead of disks

Electronics mounted outside of active region (connected to detectors by kapton cables)



⇒ long strips (high capacitance) in outer layers

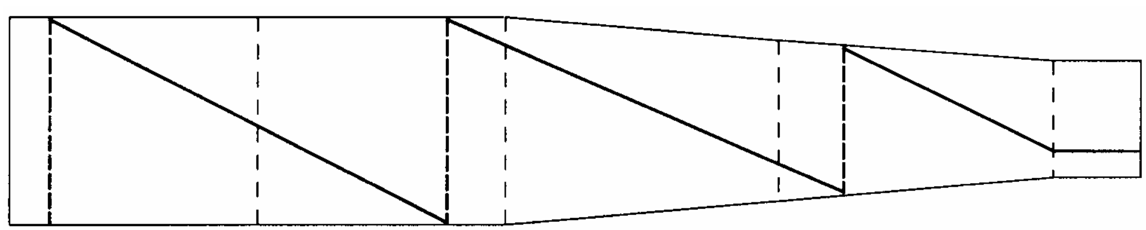
Layer	Fanout Type	Length (cm)	Number of Readout Strips	Number of Readout Channels	Typical Pitch at Input(μm)	Typical Pitch at Output (μm)	Number of Circuits
1	z, F+B	12.5	950	768	100	50	12
	ϕ, F+B	3.0	768	768	50	50	12
2	z, F+B	14.5	1150	1024	100	50	12
	ϕ, F+B	3.0	960	1024	50	50	12
3	z, F+B	15.6	1360	1280	100	50	12
	ϕ, F+B	2.0	1280	1280	50	50	12
4a	z, F	19.7	885	512	200	50	8
	z, B	24.3	1115	512	200	50	8
	ϕ, F+B	2.0	512	512	65	50	16
4b	z,F	20.6	930	512	200	50	8
	z,B	24.2	1160	512	200	50	8
	ϕ, F+B	2.0	512	512	65	50	16
5a	z, F	25.2	1160	512	200	50	9
	z, B	25.1	1205	512	200	50	9
	ϕ, F+B	2.0	512	512	65	50	18
5b	z, F+B	26.1	1205	512	200	50	18
	ϕ, F+B	2.0	512	512	65	50	18

z-strips are connected at ends, to avoid cables in middle of detector.

Kapton connecting cables that connect multiple detector segments
(use $r\varphi$ resolution to disentangle ambiguities)

Kapton rather than “double metal” to reduce capacitance (+ cost)

Connections made along diagonals:



AToM – Readout IC for BaBar Vertex Detector
(LBNL, Pavia, UCSC)

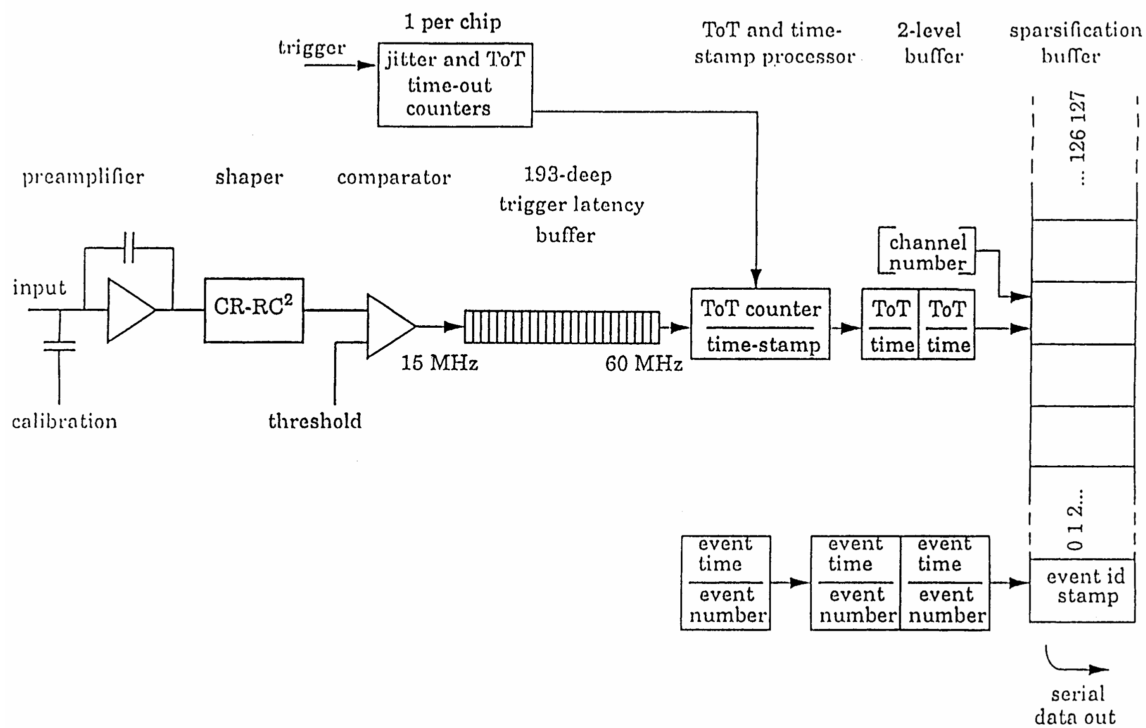
Preamplifier with continuous reset

CR-RC^2 shaper with selectable shaping times (100, 200 and 400 ns)

> Outer layers of tracker have longer strips (higher capacitance) than inner layers. Lower occupancy allows use of longer shaping time to maintain electronic noise.

Coarse digitization via Time-Over-Threshold
(analog information for position interpolation only requires 3 – 4 bit resolution)

AToM Block Diagram



Measured noise (pre-production run) for 3 shaping times

100 ns: Q_n= 350 el + 42 el/pF
200 ns: Q_n= 333 el + 35 el/pF
400 ns: Q_n= 306 el + 28 el/pF

4. Development of a Tracker Concept at the LHC

ATLAS Tracking detector for the LHC:

Colliding proton beams

7 TeV on 7 TeV (14 TeV center of mass)

Luminosity: 10^{34} cm^{-2}s^{-1}

Bunch crossing frequency: 40 MHz

Interactions per bunch crossing: 23

Charged particles per unit of rapidity: 150

$\Rightarrow$ hit rate $n' = \dfrac{2\cdot 10^9}{r_\perp^2}\ \left[\mathrm{cm}^{-2}\mathrm{s}^{-1}\right]$, where $r_\perp$= distance from beam axis

If the detector subtends ±2.5 units of rapidity, the total hit rate in the detector is $3\cdot 10^{10}$ s^{-1}

Hit rate at $r_\perp$= 14 cm: ~ 10^7 cm^{-2}s^{-1}

Overall detector to include

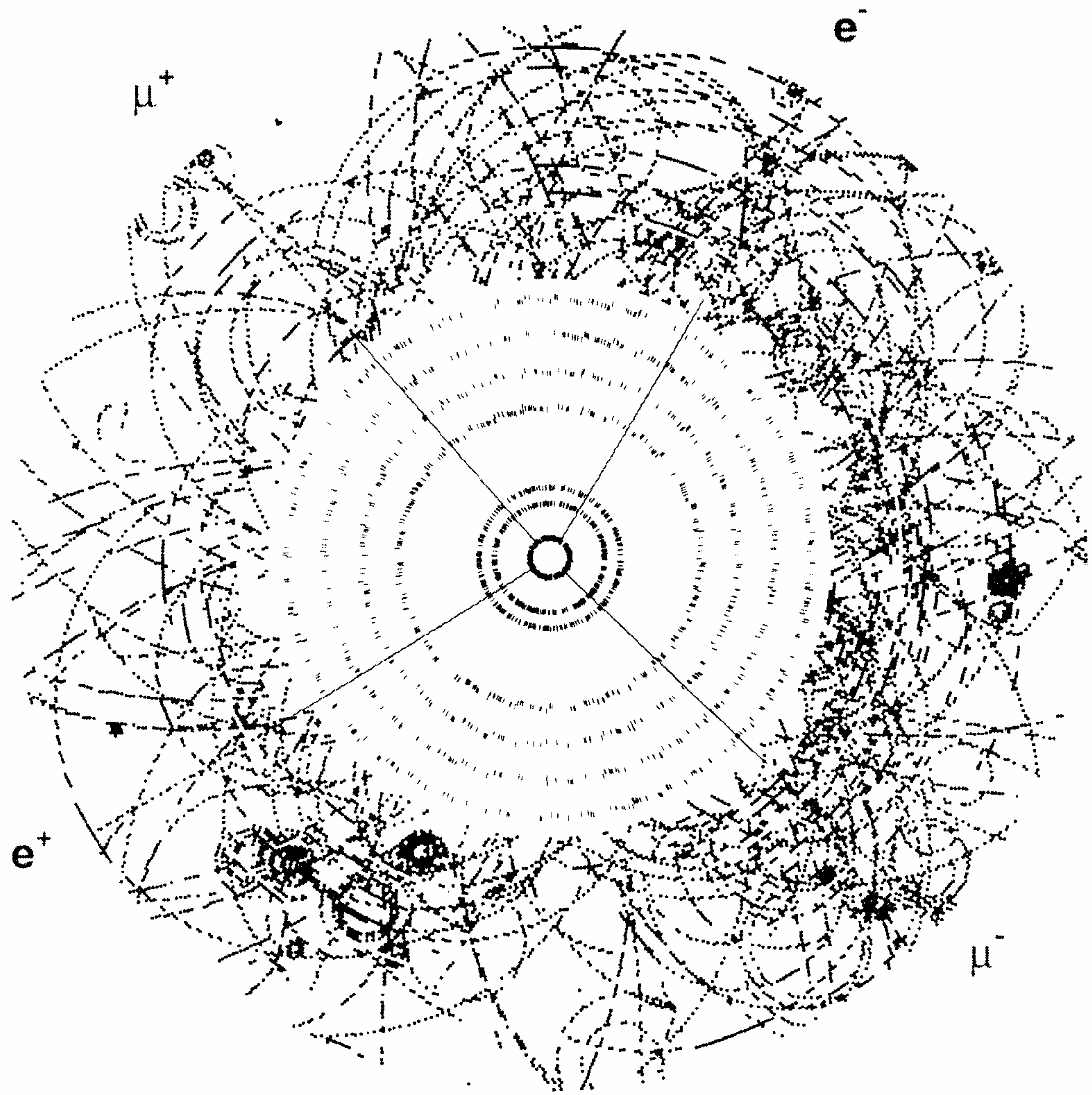
1. Vertexing for B-tagging
2. Precision tracking in 2T magnetic field
3. Calorimetry (EM + hadronic)
4. Muon detection

"Typical Event" – Axial View

H $\rightarrow$ ZZ* $\rightarrow$ $\mu^+\mu^-e^+e^-$
(m_H= 130 GeV)

Appears worse than it is

– tracks spread azimuthally, but high track density at forward angles.



Radiation Damage

Two sources of particles

a) beam collisions

b) neutron albedo from calorimeter

Fluences per year (equivalent 1 MeV neutrons)

r ~ 10 cm typ. $5 \cdot 10^{13}$ cm^{-2}

r ~ 30 cm typ. $2 \cdot 10^{13}$ cm^{-2}

Ionizing Dose per year

r ~ 10 cm 30 kGy (3 Mrad)

r ~ 30 cm 4 kGy (400 krad)

In reality, complex maps are required of the radiation flux, which is dependent on local material distribution.

How to cope with ...

- High total event rate

  a) fast electronics
  high power required for both noise and speed

  b) segmentation
  reduce rate per detector element
  for example, at r= 30 cm the hit rate in an area of $5 \cdot 10^{-2}$ cm^2 is about 10^5 s^{-1}, corresponding to an average time between hits of 10 µs.

  ⇒ longer shaping time allowable

  ⇒ lower power for given noise level

- Large number of events per crossing

  a) fast electronics (high power)

  b) segmentation
  if a detector element is sufficiently small, the probability of two tracks passing through is negligible

  c) single-bunch timing
  reduce confusion by assigning hits to specific crossing times

⇒ Segmentation is an efficient tool to cope with high rates.

With careful design, power requirements don’t increase.

⇒ Fine segmentation feasible with semiconductor detectors

- “μm-scale” patterning of detectors
- monolithically integrated electronics mounted locally

Large number of front-end channels requires simple circuitry

Single bunch timing ⇒ collection times <25 ns

Radiation damage is a critical problem in semiconductor detectors:

a) detector leakage current $I_R = I_{R0} + \alpha \Phi A d$

$\Rightarrow$ shot noise $Q_{ni}^2 = 2 q_e I_R F_i T_S$

$\Rightarrow$ self-heating of detector $I_R(T) \propto T^2 e^{-E/2k_B T}$

reduce current by cooling

reduce shaping time

reduce area of detector element

b) Increase in depletion voltage

$\Rightarrow$ thin detector

$\Rightarrow$ allow for operation below full depletion

$\Rightarrow$ less signal

Requires lower noise to maintain minimum S/N

$\Rightarrow$ decrease area of detector element (capacitance)

Use of a highly-developed technology, i.e. Si rather than “exotic” materials, provides performance reserves and design flexibility to cope with radiation damage.

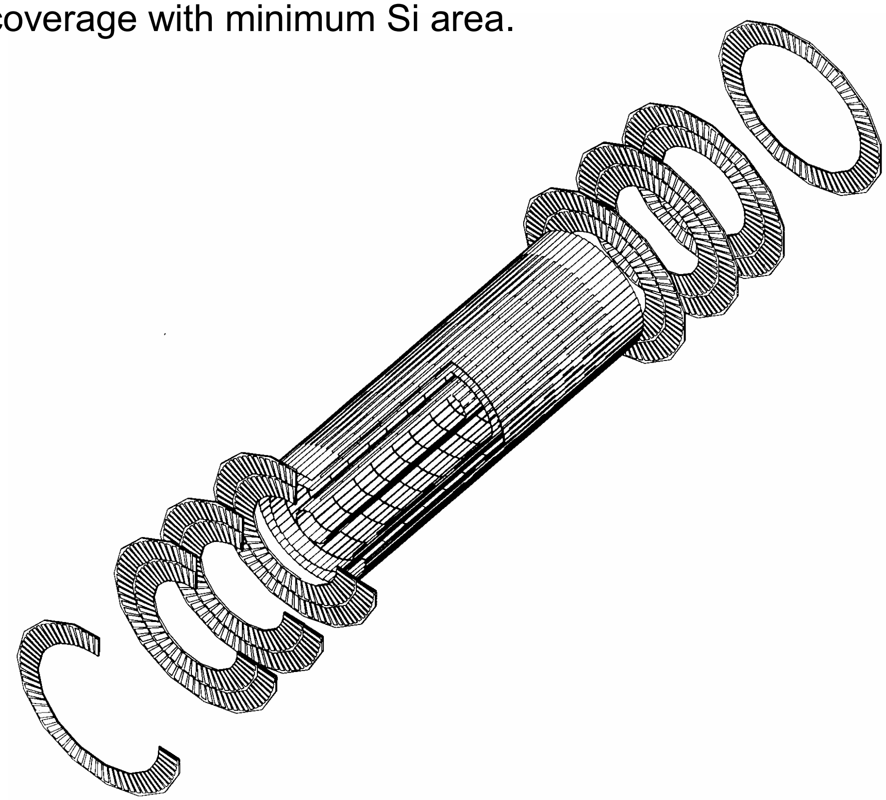
Layout

Full coverage provided by a combination of barrel and disk layers.

Coverage provided by a) barrel in central region

b) disks in forward regions

to provide maximum coverage with minimum Si area.



Pixels at small radii (4, 11, 14 cm) to cope with

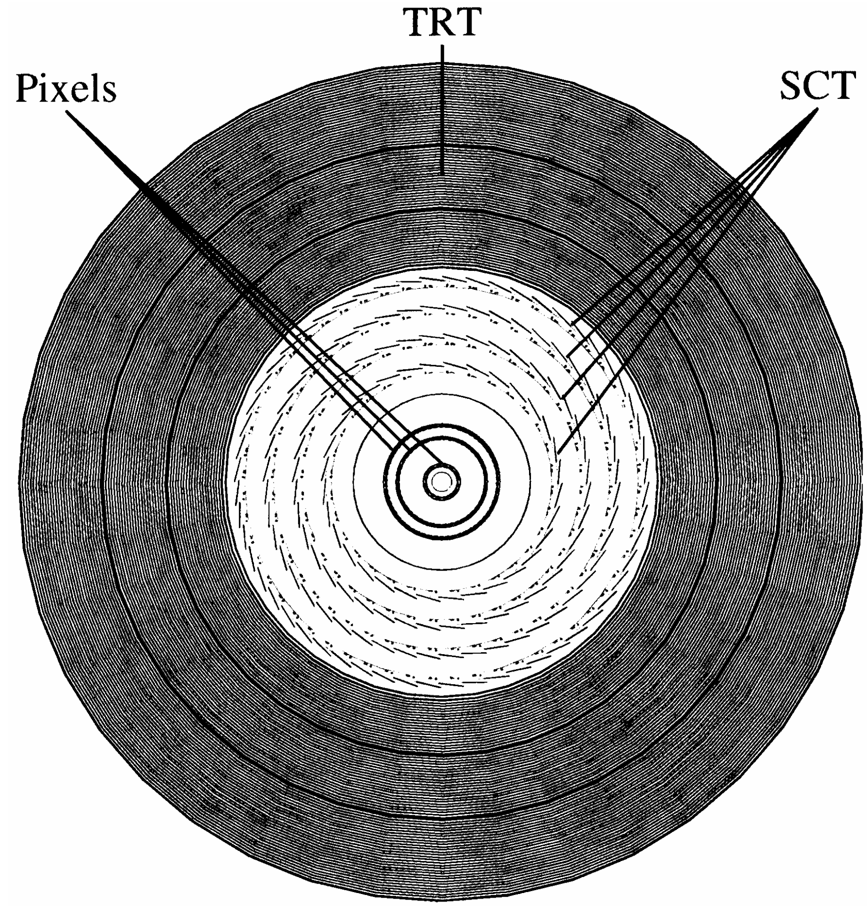
- high event rate (2D non-projective structure)
- radiation damage
  small capacitance ~ 100 fF
  $\Rightarrow$ low noise $Q_n \approx 100$ el

Strips at larger radii (30, 37, 45, 52 cm)
minimize material, cost

Pixels and strips provide primary pattern recognition capability

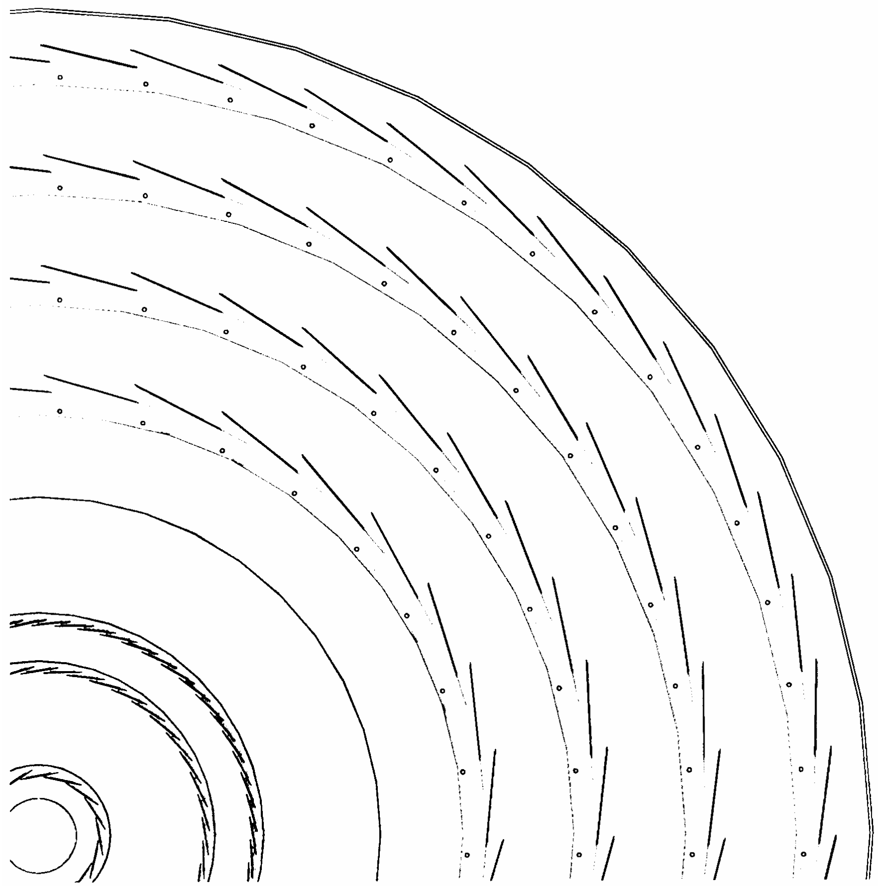
Straw drift chambers at outer radius (56 – 107 cm)

~70 layers yield 40 space points at large R and augment pattern recognition by continuous tracking (least expensive solution)

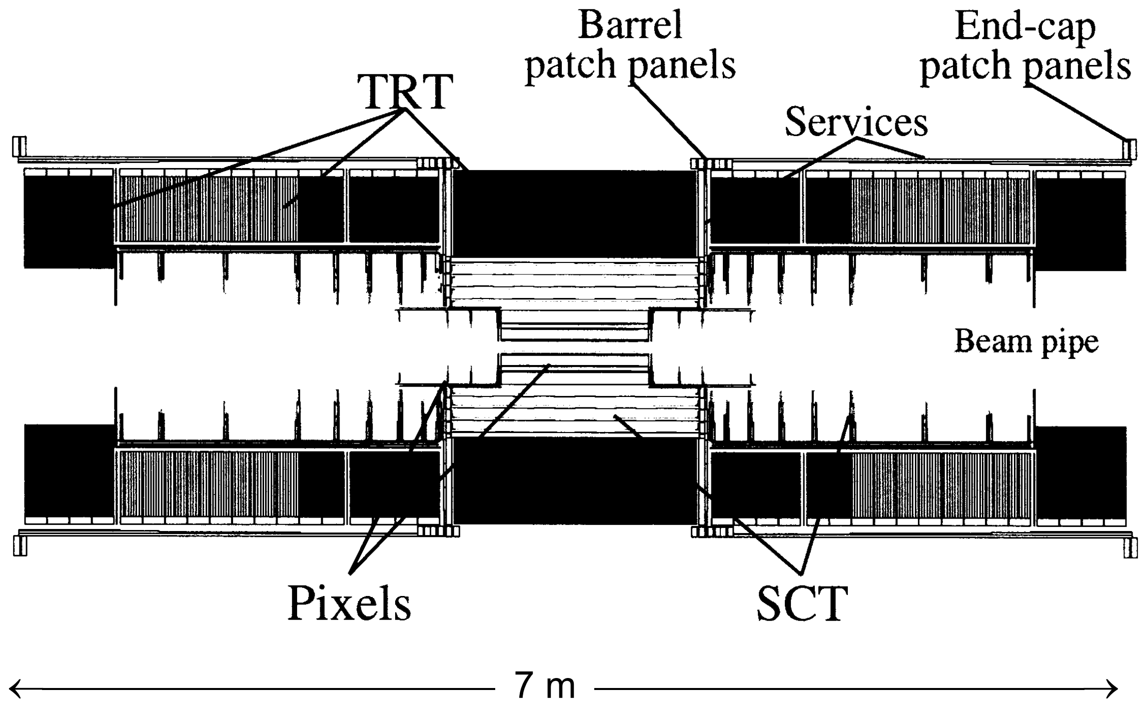


Detector modules arranged in cylindrical shells (barrels).

Modules are "shingled" to provide full coverage and overlap to facilitate relative position calibration.



Strip modules use back-to-back single-sided detectors with small-angle stereo (40 mr) to provide z-resolution with negligible "ghosting".



Resolution provided by 3 detector types in barrel

	$r\phi$	z
Pixels	12 µm	66 µm
Strips	16 µm	580 µm
Straws	170 µm	—

Segmentation ⇒ Large number of data channels

Total number of channels and area:

Pixels	1.4×10^{8} channels	$2.3\ m^2$
Strips	6.2×10^{6} channels	$61\ m^2$
Straws	4.2×10^{5} channels	

But, only a small fraction of these channels are struck in a given crossing

Occupancy for pixels, 50 µm x 300 µm:

4 cm Pixel Layer	4.4×10^{-4}
11 cm Pixel Layer	0.6×10^{-4}

Occupancy for strip electrodes with 80 µm pitch, 12 cm length:

30 cm Strip Layer	6.1×10^{-3}
52 cm Strip Layer	3.4×10^{-3}

Utilize local sparsification – i.e. on-chip circuitry that recognizes the presence of a hit and only reads out those channels that are struck.

⇒ data readout rate depends on hit rate, not on segmentation

First implemented in SVX chip

S.A. Kleinfelder, W.C. Carrithers, R.P. Ely, C. Haber, F. Kirsten, and H.G. Spieler, A Flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout, IEEE Trans. Nucl. Sci. **NS-35** (1988) 171

Readout

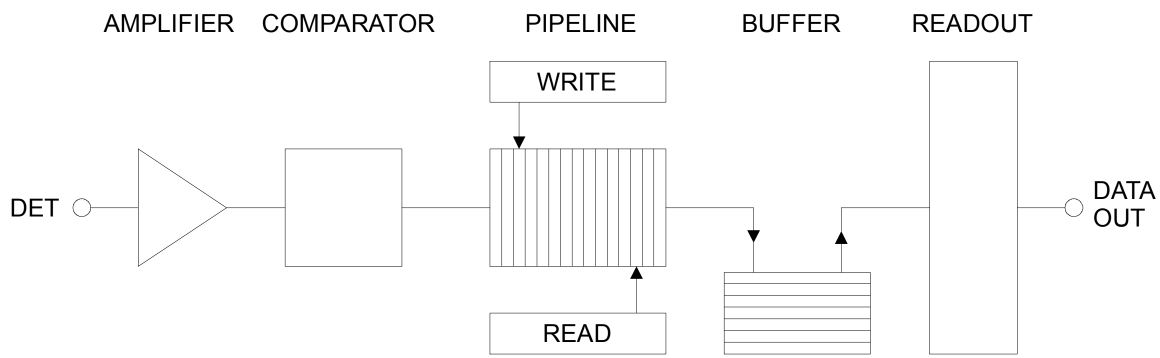
Strips + Pixels: many channels

Essential to minimize
- power
- material (chip size, power cables, readout lines)
- cost (chip size)
- failure rate (use simple, well controlled circuitry)

Goal is to obtain adequate position resolution, rather than the best possible

⇒ Binary Readout
- detect only presence of hits
- identify beam crossing

Architecture of ATLAS strip readout



Unlike LEP detectors …

Crossing frequency >> readout rate

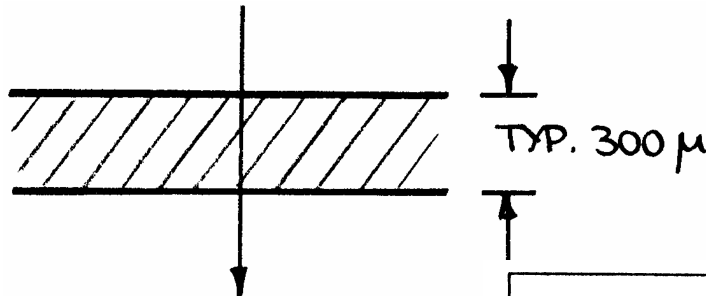
Data readout must proceed simultaneously with signal detection (equivalent to DC beam)

Single 128-channel BiCMOS chip (BJT + CMOS on same chip) in radiation-hard technology.

Required Signal-to-Noise Ratio

Acceptable noise level established by signal level and noise occupancy

1. Signal Level

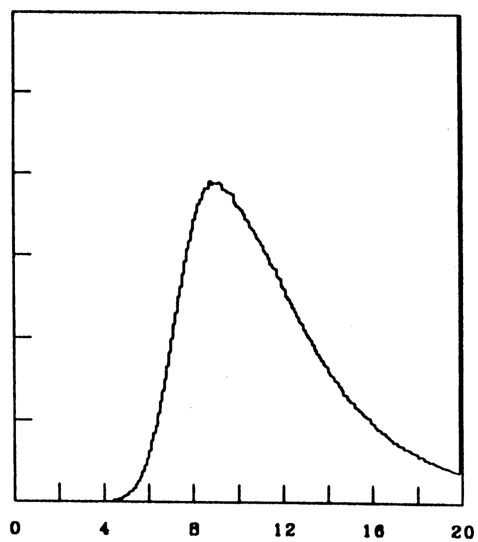


For minimum ionizing particles:

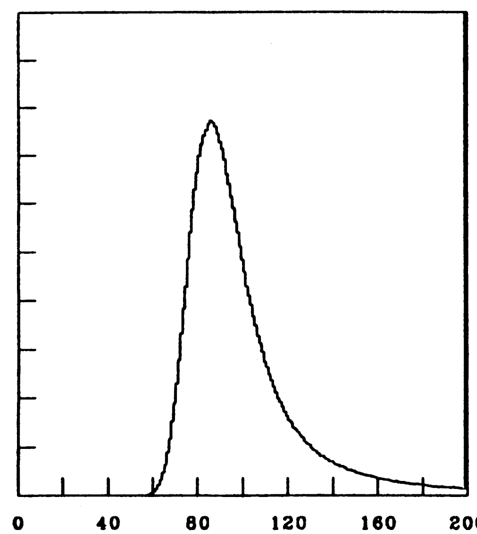
Q_s= 22000 *el* (3.5 fC)

Signals vary event-by-event according to Landau distribution

Relative width of distribution decreases with increasing energy loss.



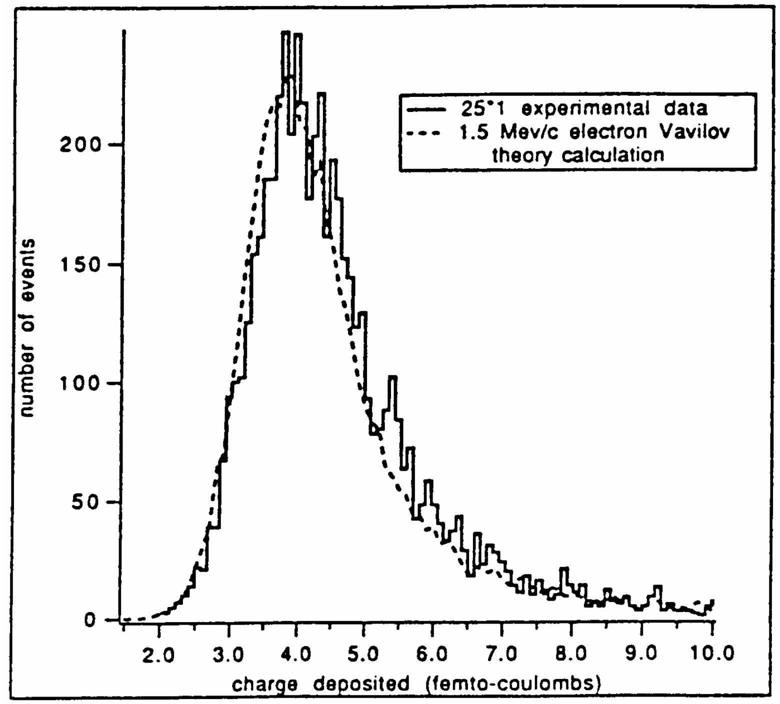
Si : 40 µm thick



Si : 300 µm thick

(calculation by G. Lynch)

Measured Landau distribution in a 300 µm thick Si detector
(Wood et al., Univ. Oklahoma)



The Landau distribution peaks at the most probable energy loss Q_0 and extends down to about 0.5 Q_0 for 99% efficiency.

Assume that the minimum energy is $f_L Q_0$.

Tracks passing between two strips will deposit charge on both strips.
If the fraction of the signal to be detected is f_{sh}, the circuit must be sensitive signal as low as

$$Q_{\min} = f_{sh} f_L Q_0$$

2. Threshold Setting

It would be desirable to set the threshold much lower than Q_{min}, to be insensitive to threshold variations across the chip.

A lower limit is set by the need to suppress the noise rate to an acceptable level that still allows efficient pattern recognition.

As discussed in an Appendix, the threshold-to-noise ratio required for a desired noise rate f_n in a system with shaping time T_S is

$$\frac{Q_T}{Q_n} = \sqrt{-2\log(4\sqrt{3}f_n T_S)}$$

Expressed in terms of occupancy P_n in a time interval Δt

$$\frac{Q_T}{Q_n} = \sqrt{-2\log\left(4\sqrt{3}_n T_S \frac{P_n}{\Delta t}\right)}$$

In the strip system the average hit occupancy is about 5 x 10^{-3} in a time interval of 25 ns. If we allow an occupancy of 10^{-3} at a shaping time of 20 ns, this corresponds to

$$\frac{Q_T}{Q_n} = 3.2$$

The threshold uniformity is not perfect. The relevant measure is the threshold uniformity referred to the noise level. For a threshold variation ΔQ_T, the required threshold-to-noise ratio becomes

$$\frac{Q_T}{Q_n} = \sqrt{-2\log\left(4\sqrt{3}_n T_S \frac{P_n}{\Delta t}\right)} + \frac{\Delta Q_T}{Q_n}$$

If $\Delta Q_T / Q_n = 0.5$, the required threshold-to-noise ratio becomes $Q_T / Q_n = 3.7$.

To maintain good timing, the signal must be above threshold by at least Q_n, so $Q_T / Q_n > 4.7$.

Combining the conditions for the threshold

$$\left(\frac{Q_T}{Q_n}\right)_{min} Q_n \le Q_{min} \quad \text{and signal} \quad Q_{min} = f_{sh} f_L Q_0$$

yields the required noise level

$$Q_n \le \frac{f_{sh} f_L Q_0}{(Q_T / Q_n)_{\min}}$$

If charge sharing is negligible $f_{sh} = 1$, so with $f_L = 0.5$, $Q_0 = 3.5$ fC and $(Q_T / Q_n)_{\min} = 4.7$

$$Q_n \le 0.37 \text{ fC} \quad \text{or} \quad Q_n \le 2300\ el$$

If the system is to operate with optimum position resolution, i.e. equal probability of 1- and 2-hit clusters, then $f_{sh} = 0.5$ and

$$Q_n \le 0.19 \text{ fC} \quad \text{or} \quad Q_n \le 1150\ el$$

ATLAS requires $Q_n \le 1500\ el$.

Prototype Results

ATLAS has adopted a single chip implementation (ABCD chip).

- 128 ch, bondable to 50 µm strip pitch
- bipolar transistor technology, rad-hard
  $\Rightarrow$ minimum noise independent of shaping time
- peaking time: ~20 ns (equivalent CR-RC^4)
- double-pulse resolution (4 fC – 4 fC): 50 ns
- noise, timing: following slides
- 1.3 to 1.8 mW/ch (current in input transistor adjustable)
- on-chip DACs to control threshold + operating point
- Trim DACs on each channel to reduce channel-to-channel gain and threshold non-uniformity
- Readout allows defective chips to be bypassed
- Optical fiber readout with redundancy
- die size: 6.4 x 4.5 mm^2

For illustration, the following slides show data from a previous prototype IC, the CAFE chip

This was part of an initial 2-chip implementation
(BJT analog chip and CMOS digital chip)

Production ICs are single chip BiCMOS with same architecture: similar results

CAFE Timing Performance

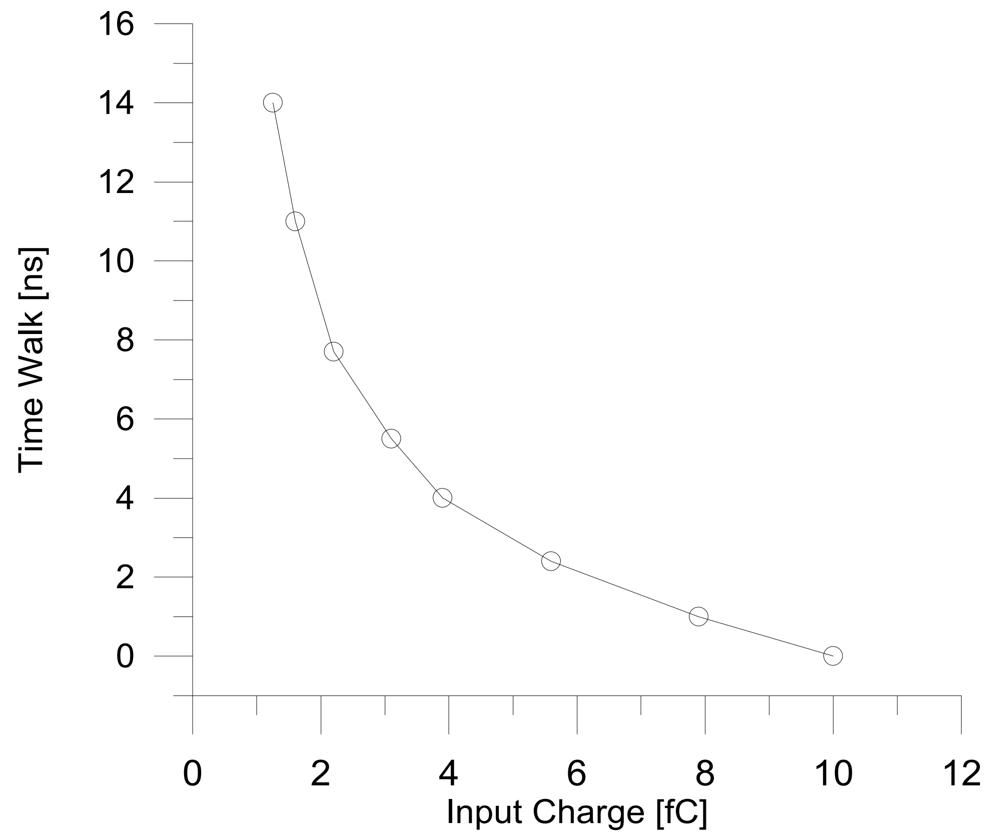
1. Chips from run 1 measured on test boards

- **irradiated to 10^{14} cm^{-2} (MIP equiv)**

Time Walk	1.25 - 10 fC:	16 ns
1 fC threshold	1.25 - 4 fC:	12 ns
	4 fC - 10 fC:	4 ns

Jitter at 1.25 fC ≈ 4 ns FWHM

Total time diistribution (99% efficiency) confined within about 18 ns.



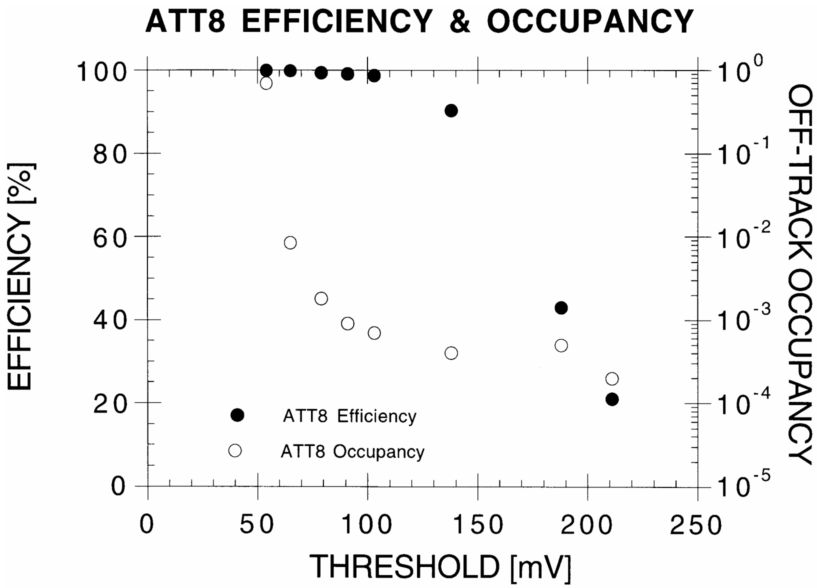
2. Chips from Run 2 measured on test boards (**pre-rad**)

C_{load}= 15 pF, 1 fC threshold, jitter as above

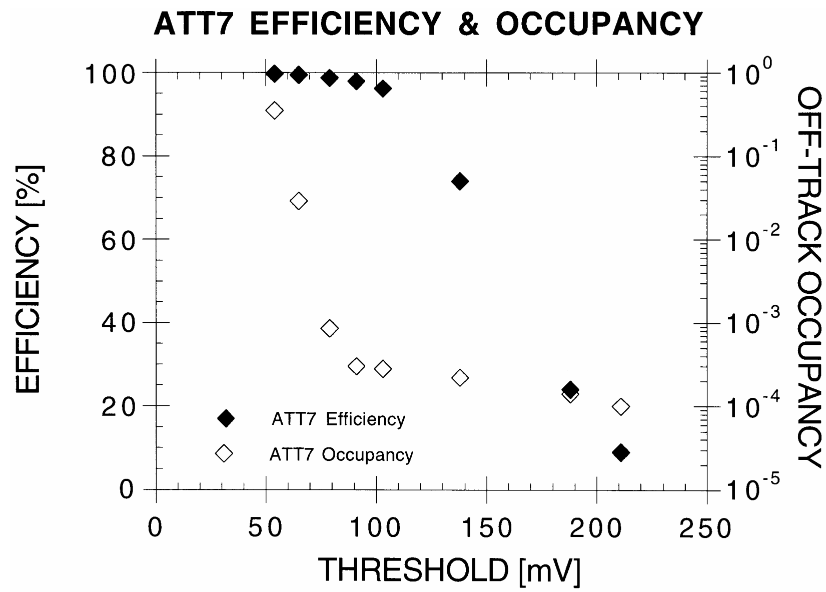
Test Beam Data

Tracking Efficiency vs. Occupancy for Full-Length Modules

non-irradiated module



irradiated module ($\Phi = 10^{14}$ cm^{-2})



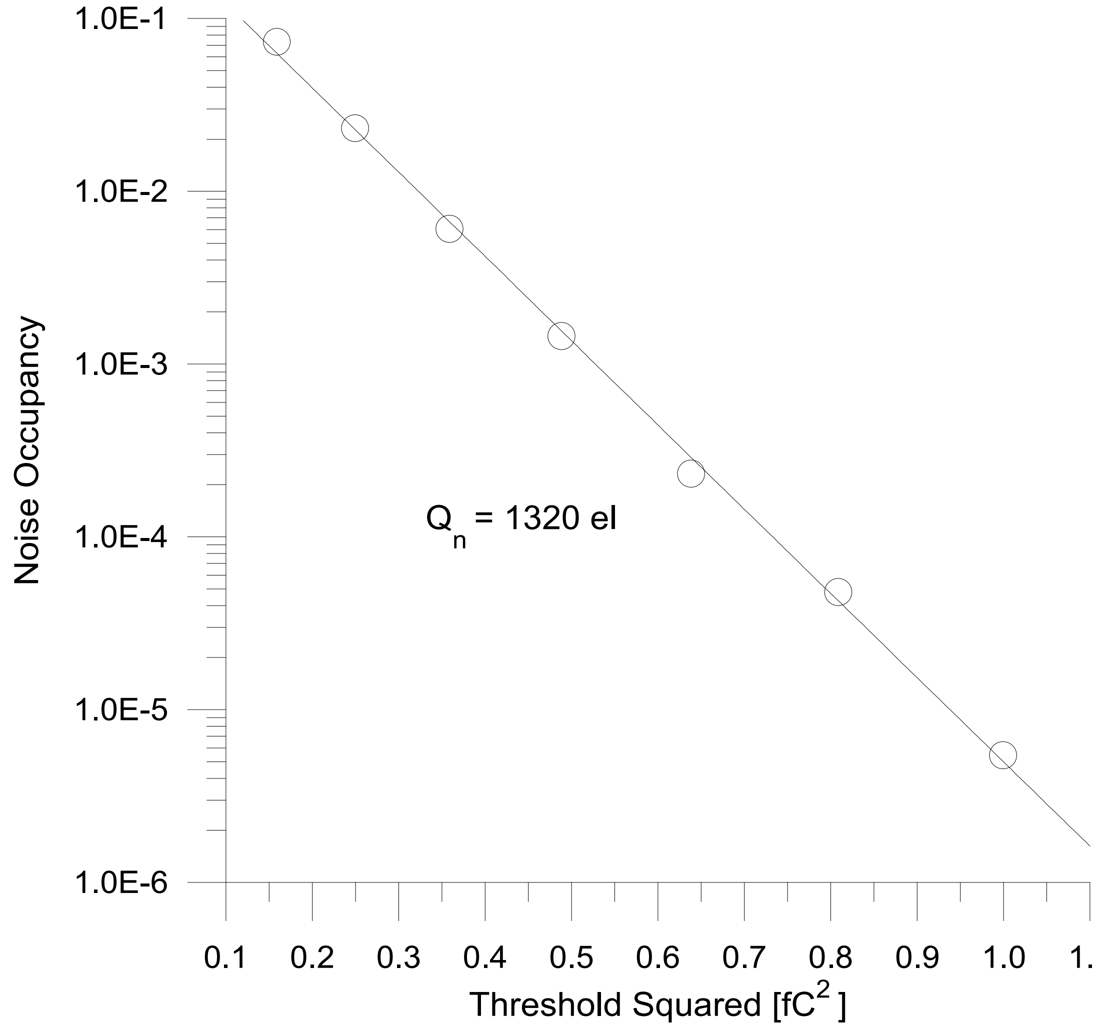
Noise Occupancy vs. Threshold

Module with CAFE chip in test beam position at KEK

Baseline fluctuations, digital cross-talk

⇒ deviations from straight line plot (gaussian noise)

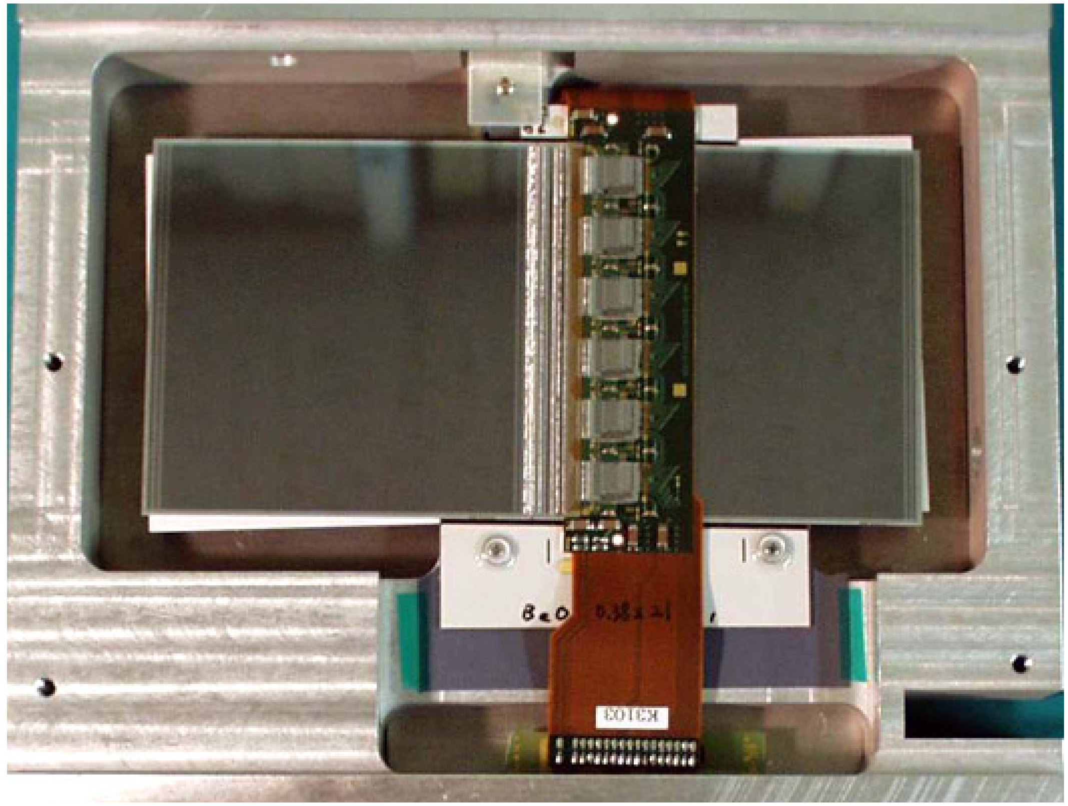
test beam noise same as measured in laboratory (within 5% simulation)



ATLAS Silicon Strip Detector Module

(mounted in fabrication fixture)

Two 6 x 6 cm^2 single-sided Si strip detectors butted edge-to-edge to form 12 cm long detector



Two 6 x 12 cm^2 detectors glued back-to-back and rotated to one another by 40 mrad to form small-angle stereo

Readout ICs – 128 channels each – mounted on detectors and connected at middle (reduce thermal noise of strip electrode resistance).

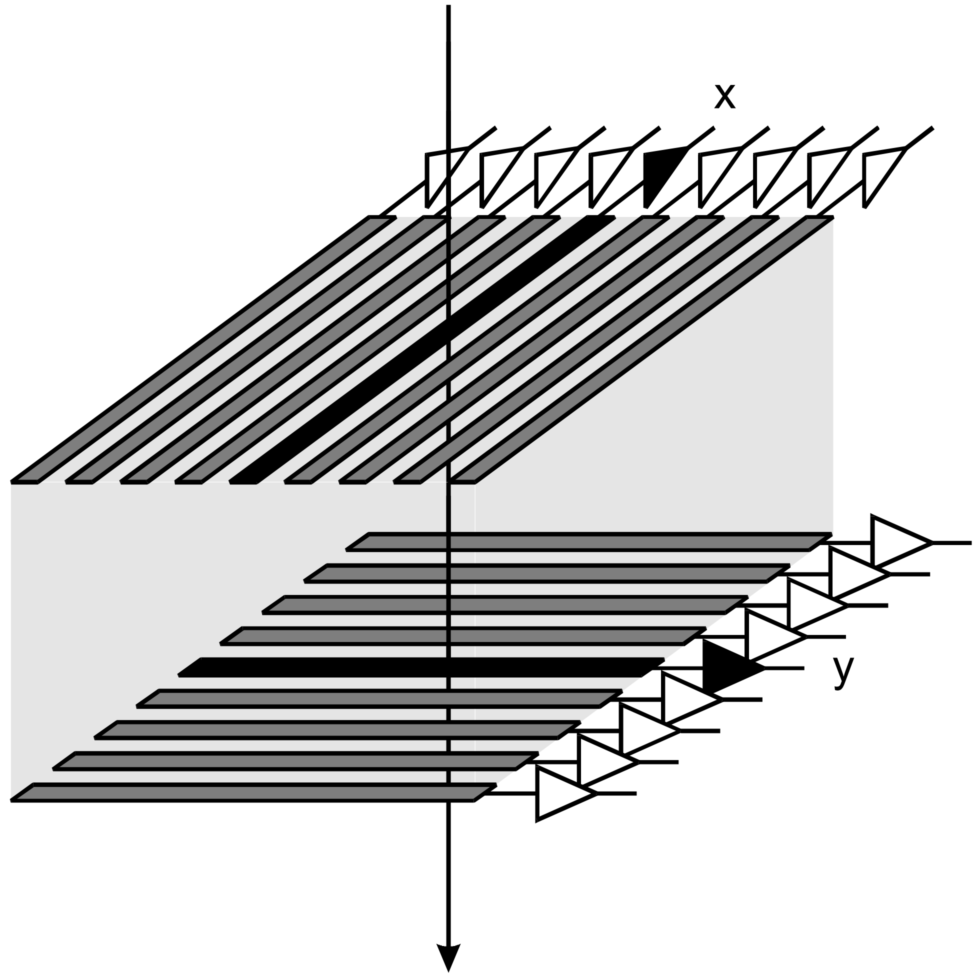
Strip pitch: 80 µm
no. of channels: 2 x 768

Binary readout with on-chip pipeline and readout sparsification

Kapton pigtail connects to local opto-module for clock, control, data transmission

Two-Dimensional Detectors

Example: Crossed strips on opposite sides of Si wafer



n readout channels $\Rightarrow$ n^2 resolution elements

Problem: ambiguities with multiple hits

n hits in acceptance field $\Rightarrow$

n x-coordinates and n y-coordinates

$\Rightarrow$ n^2 combinations

of which $n^2 - n$ are "ghosts"

ATLAS strips reduce ambiguities by using small angle stereo (40 mrad).

Not sufficient at small radii –

need non-projective 2D detector

Pixel Detectors with Random Access Readout
(K. Einsweiler et al.)

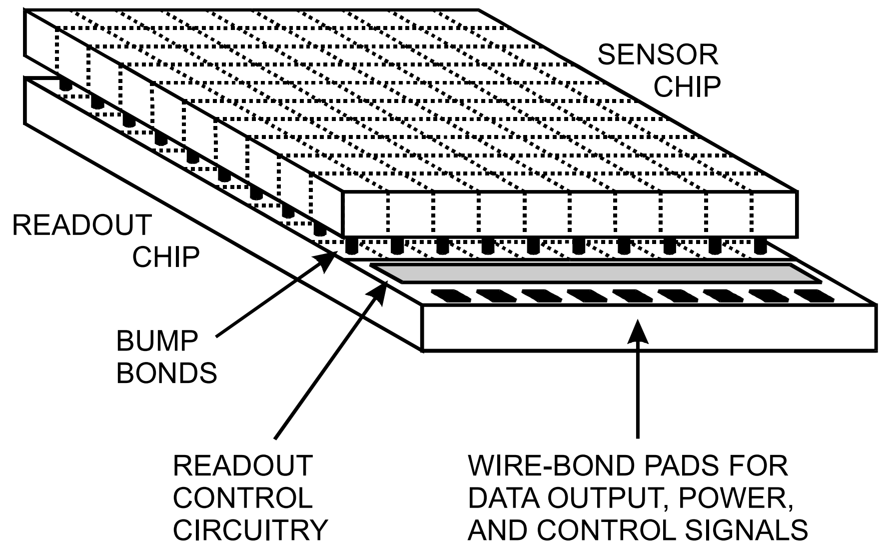
"Smart Pixels"

Quiescent state:
no clocks or switching in pixel array

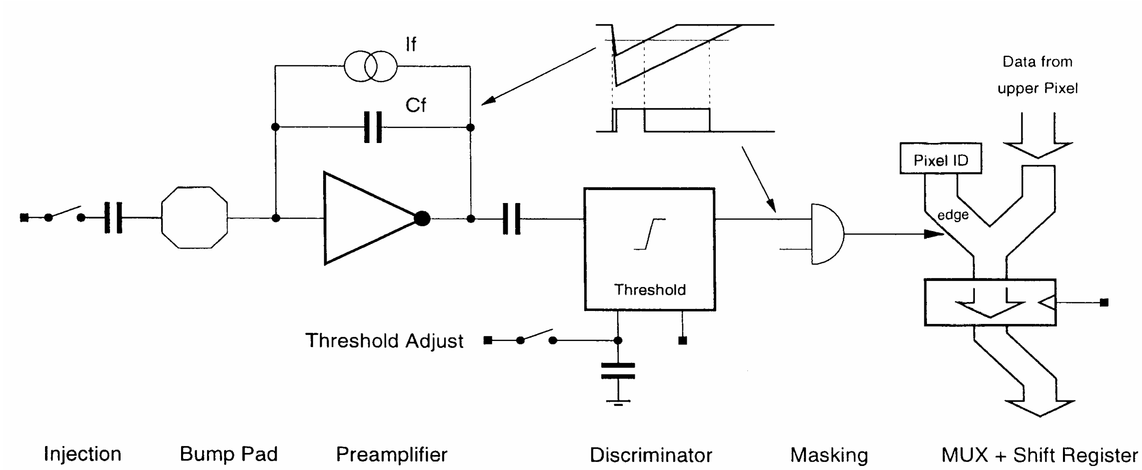
Pixel circuitry only issues signals when struck.

Struck pixels send address + time stamp
to peripheral register

On receipt of trigger selectively read out pixels.



Block Diagram of Pixel Cell



Q-amplifier + shaper per pixel

threshold comparator per pixel

trim-DAC per pixel for fine adjustment of threshold

time-over-threshold analog digitization

test pulse per pixel

bad pixels can be masked

Pixel size: 50 µm x 400 µm

size historical:
could be
50 µm x 200 µm

Power per pixel: < 40 µW

Final chip: 18 columns x 160 pixels (2880 pixels)

Module size: 16.4×60.4 mm^2

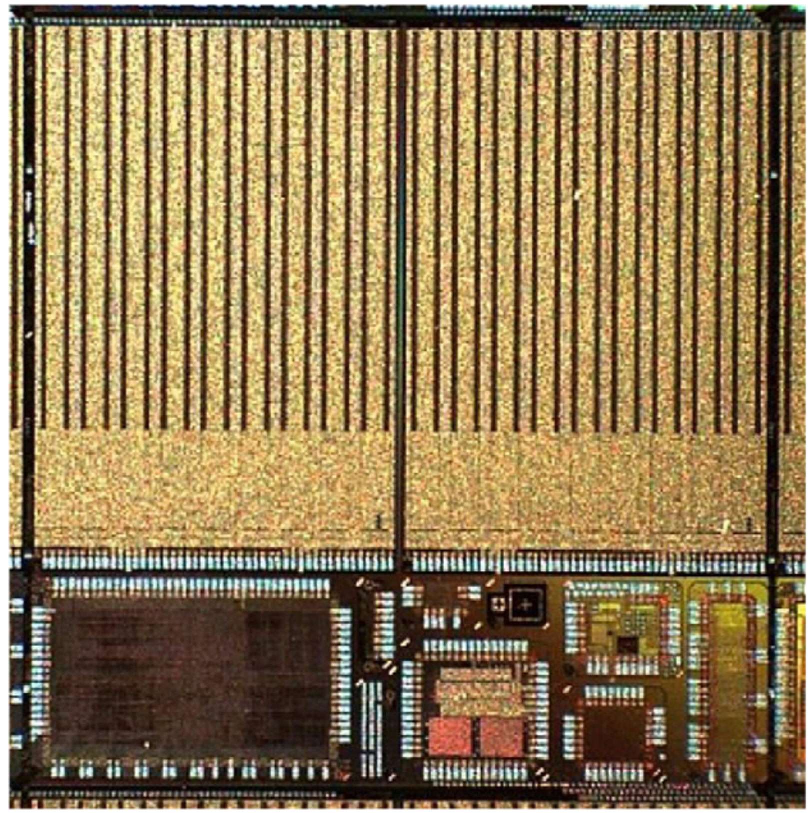
16 front-end chips per module

46080 pixels per module

fabricated in 0.25 µm CMOS

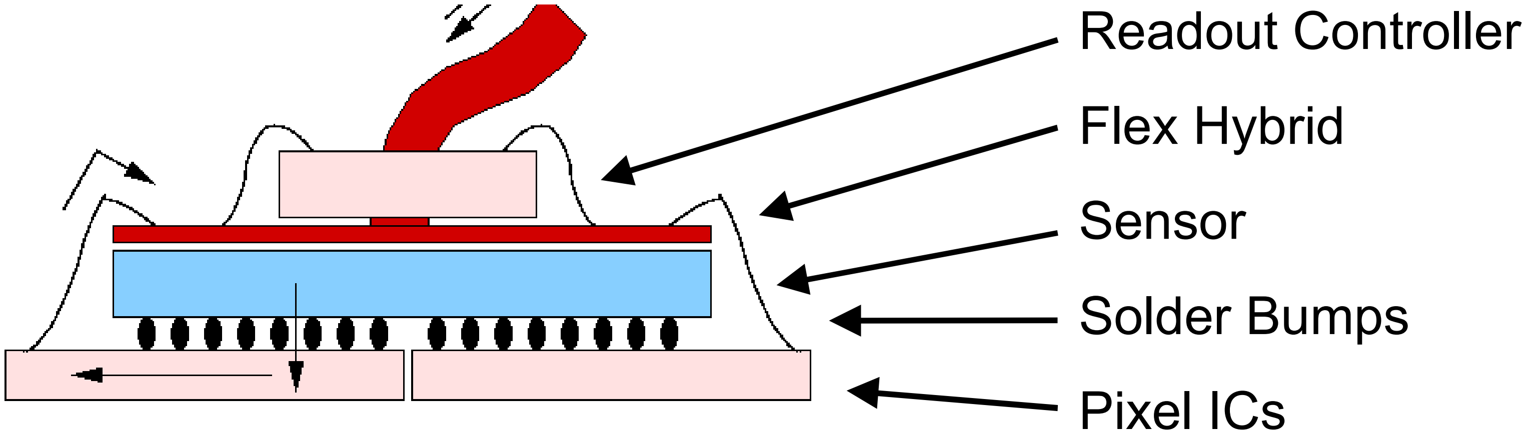
~ $3.5 \cdot 10^6$ transistors

functional to > 100 Mrad



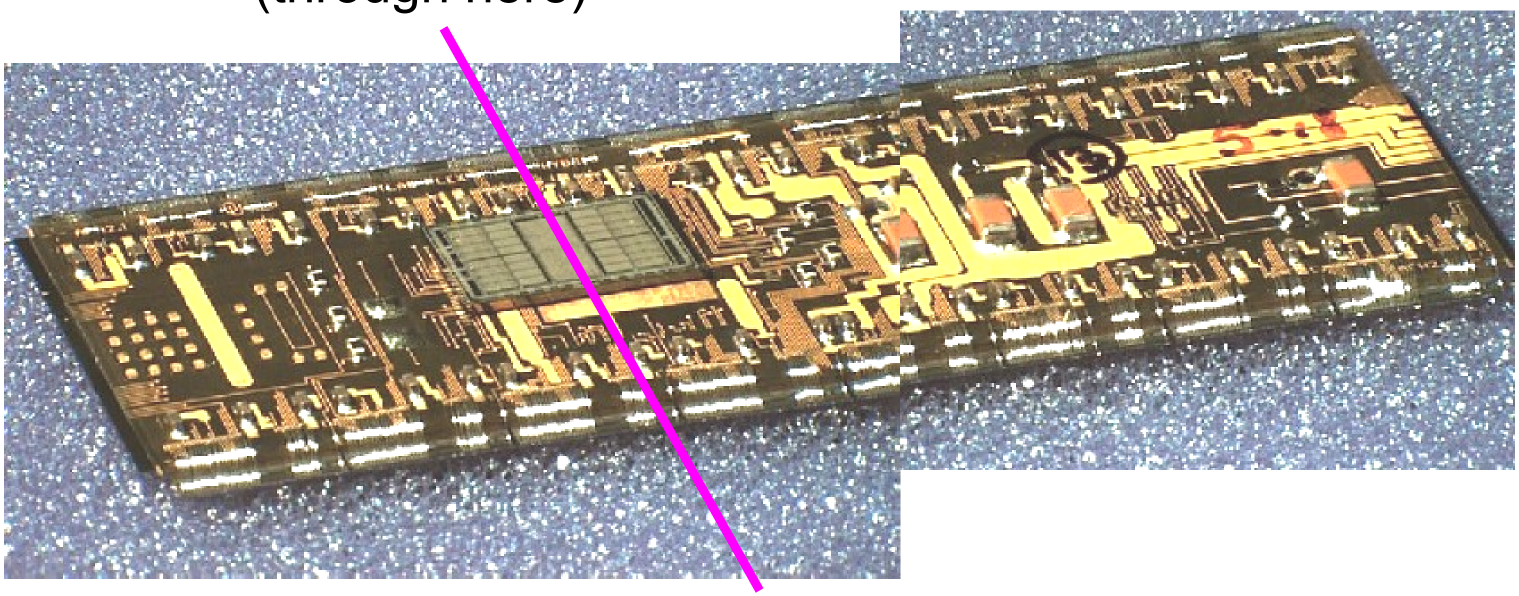
Measured noise level: ~100 e (threshold < noise)

Radiation resistant to higher fluences than strips because low noise provides large performance reserves.



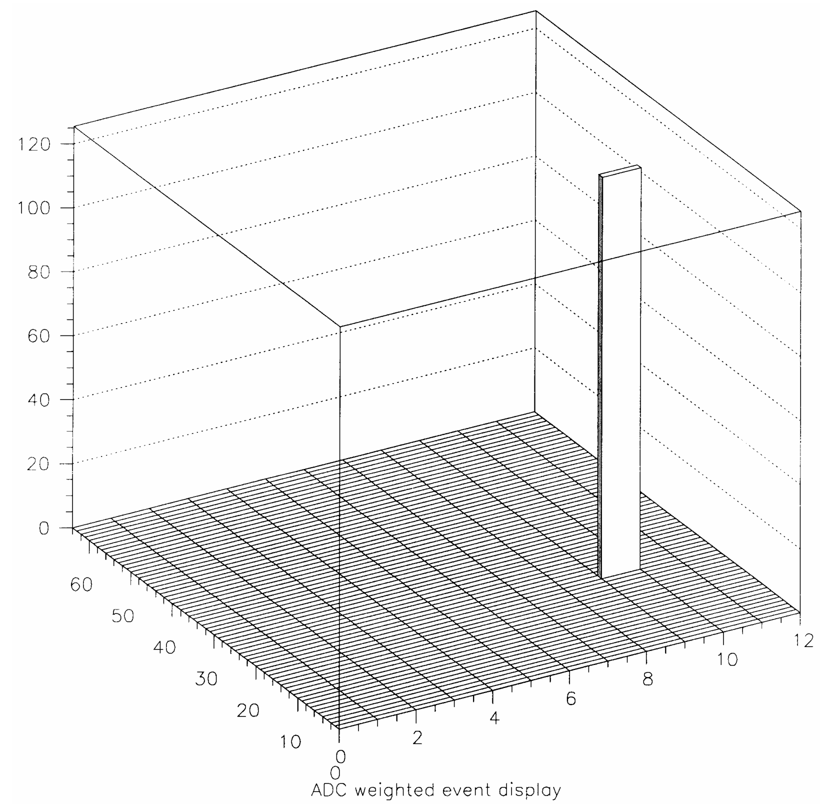
Schematic Cross Section

(through here)

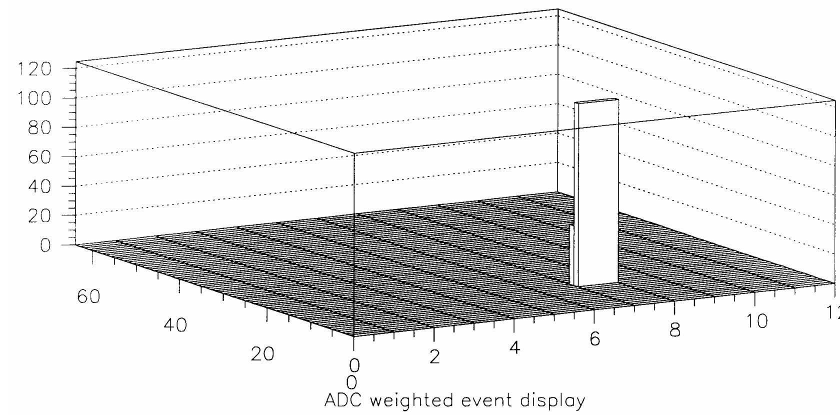


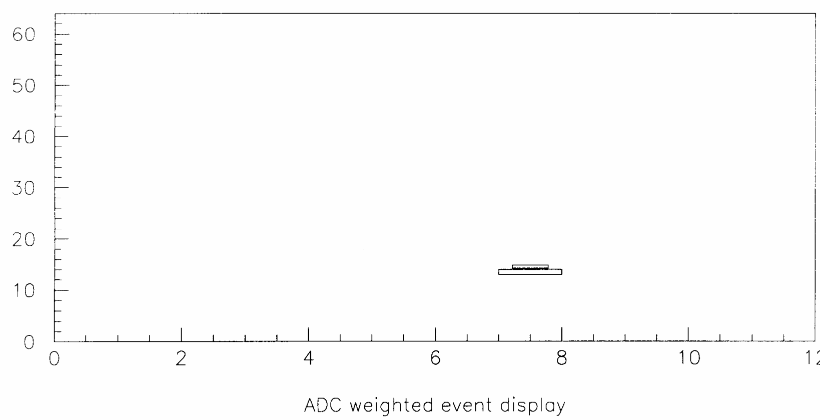
Test Beam Results

Track through single pixel



Charge sharing





Advantages of pixels at LHC

2D segmentation

⇒ Pattern recognition at small radii

Low capacitance

⇒ high S/N

⇒ allows degradation of both detector signal and electronic noise due to radiation damage

small detector elements

⇒ detector bias current per element still small after radiation damage

Drawback:

Engineering complexity order of magnitude greater than previous chips

Question: What is the ultimate limit of radiation resistance?

Current design could survive 5 – 10 years at nominal LHC luminosity.

Luminosity upgrade? Much R&D necessary.