V. Signal Processing – Part 2

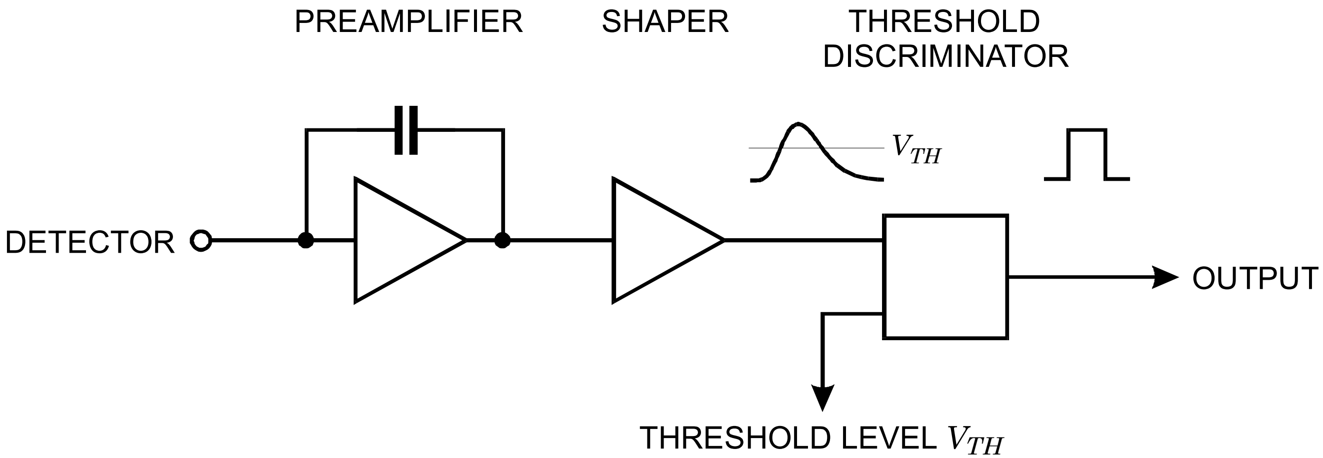
1. Threshold Discriminator Systems
2. Timing Measurements
3. Digitization
   - Elements of Digital Electronics
   - Analog-to-Digital Conversion
4. Digital Signal Processing

1. Threshold Discriminator Systems

The simplest form of a digitized readout is a threshold discriminator system, which produces a normalized (digital) output pulse when the input signal exceeds a certain level.

Noise affects not only the resolution of amplitude measurements, but also the determines the minimum detectable signal threshold.

Consider a system that only records the presence of a signal if it exceeds a fixed threshold.



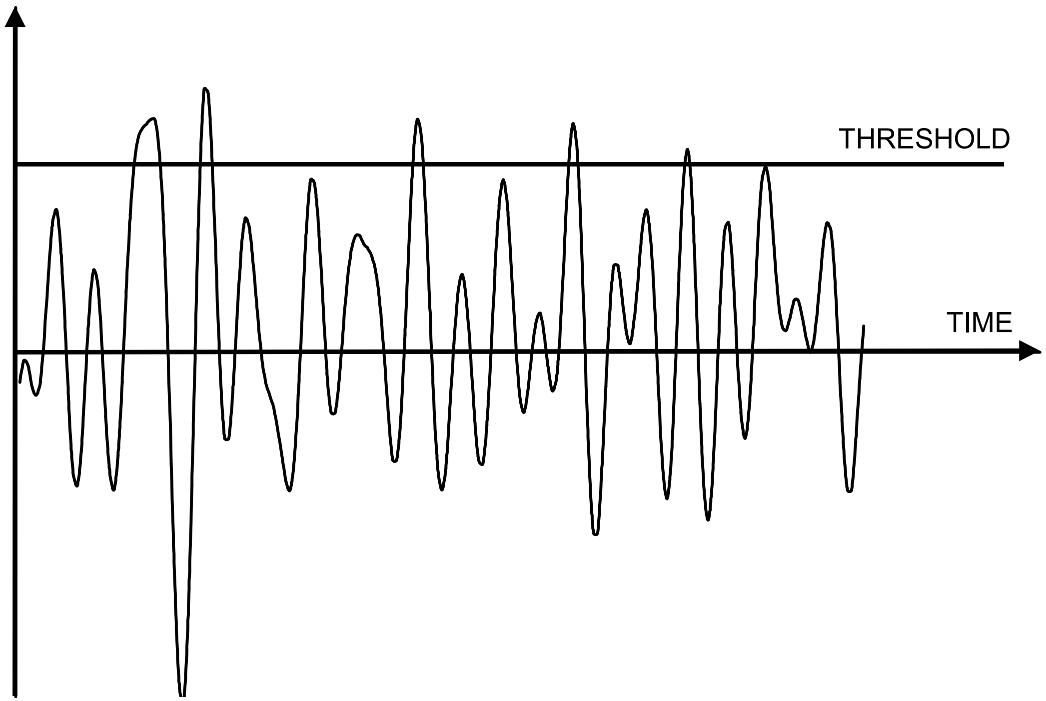
How small a detector pulse can still be detected reliably?

Consider the system at times when no detector signal is present.

Noise will be superimposed on the baseline.

Some noise pulses will exceed the threshold.

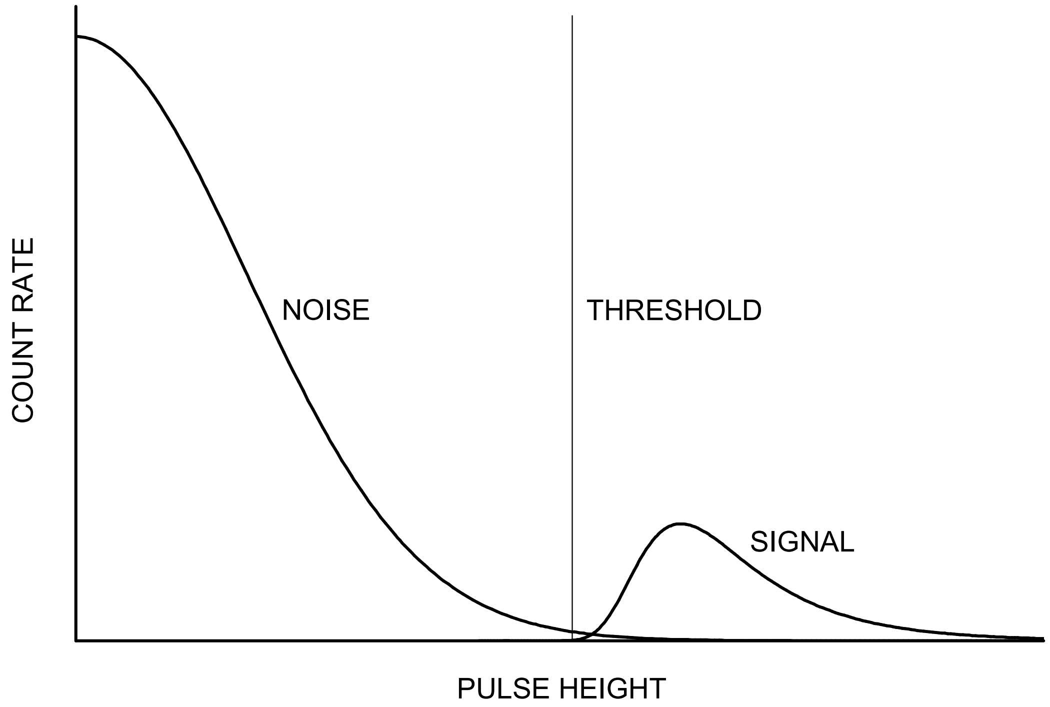
This is always true since the amplitude spectrum of Gaussian noise extends to infinity



The threshold must be set

1. high enough to suppress noise hits

2. low enough to capture the signal



With the threshold level set to 0 relative to the baseline, all of the positive excursions will be recorded.

Assume that the desired signals are occurring at a certain rate.

If the detection reliability is to be >99%, for example, then the rate of noise hits must be less than 1% of the signal rate.

The rate of noise hits can be reduced by increasing the threshold.

If the system were sensitive to pulse magnitude alone, the integral over the Gaussian distribution (the error function) would determine the factor by which the noise rate f_{n0} is reduced.

$$\frac{f_n}{f_{n0}} = \frac{1}{Q_n\sqrt{2\pi}} \int_{Q_T}^{\infty} e^{-(Q/2Q_n)^2} dQ \ ,$$

where Q is the equivalent signal charge,

Q_n the equivalent noise charge and

Q_T the threshold level.

However, since the pulse shaper broadens each noise impulse, **the time dependence is equally important**. For example, after a noise pulse has crossed the threshold, a subsequent pulse will not be recorded if it occurs before the trailing edge of the first pulse has dropped below threshold.

Combined probability function

Both the amplitude and time distribution are Gaussian.

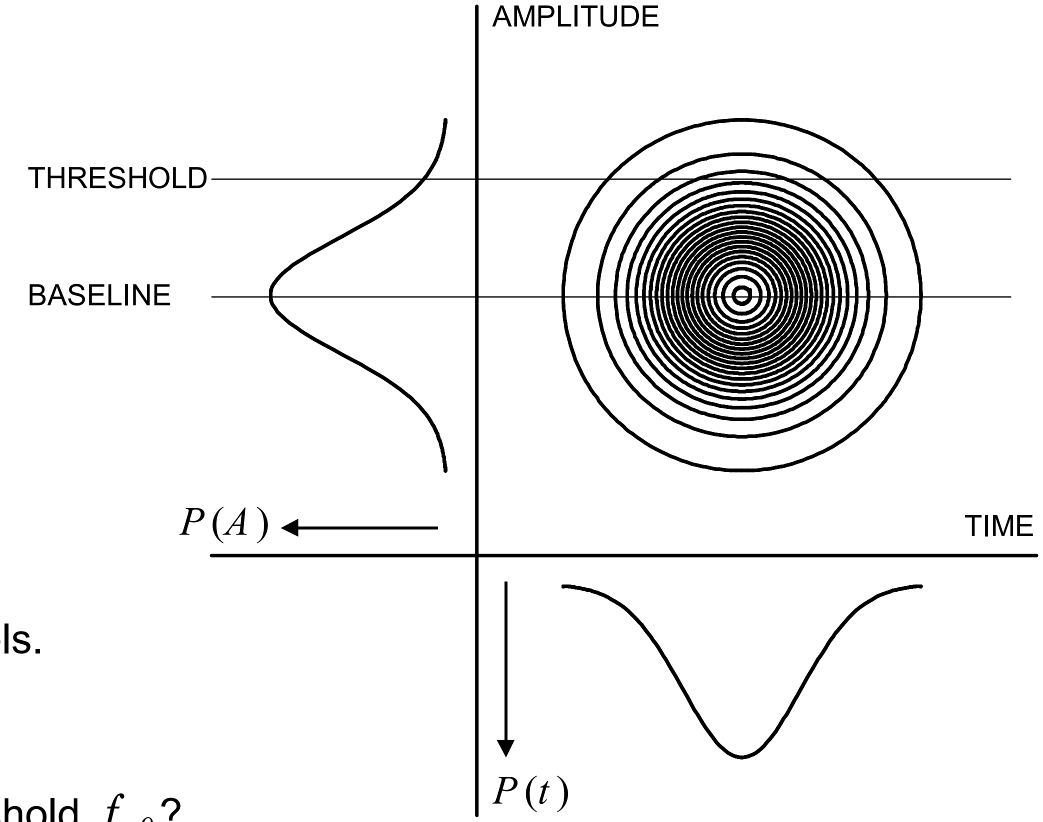
The rate of noise hits is determined by integrating the combined probability density function in the regime that exceeds the threshold.

This yields

$$f_n = f_{n0} \cdot e^{-Q_T^2 / 2Q_n^2}$$

Of course, one can just as well use the corresponding voltage levels.

What is the noise rate at zero threshold f_{n0}?



For a system with the frequency response $A(f)$ the frequency of zeros

$$f_0^2 = 4 \cdot \frac{\int_0^\infty f^2 A^2(f)\,df}{\int_0^\infty A^2(f)\,df}$$

(Rice, Bell System Technical Journal, **23** (1944) 282 and **24** (1945) 46)

Since we are interested in the number of positive excursions exceeding the threshold, f_{n0} is ½ the frequency of zero-crossings.

For an ideal band-pass filter with lower and upper cutoff frequencies f_1 and f_2 the noise rate

$$f_0 = 2\sqrt{\frac{1}{3}\,\frac{f_2^3 - f_1^3}{f_2 - f_1}}$$

For a *CR-RC* filter with $\tau_i = \tau_d$ the ratio of cutoff frequencies of the noise bandwidth is

$$\frac{f_2}{f_1} = 4.5$$

so to a good approximation one can neglect the lower cutoff frequency and treat the shaper as a low-pass filter, *i.e.* $f_1 = 0$.

Then $$f_0 = \frac{2}{\sqrt{3}} f_2$$

An ideal bandpass filter has infinitely steep slopes, so the upper cutoff frequency f_2 must be replaced by the noise bandwidth.

The noise bandwidth of an RC low-pass filter with time constant τ is $$\Delta f_n = \frac{1}{4\tau}$$

Setting $f_2 = \Delta f_n$ yields the frequency of zeros $$f_0 = \frac{1}{2\sqrt{3}\ \tau}$$

and the frequency of noise hits vs. threshold

$$f_n = f_{n0} \cdot e^{-Q_{th}^2/2Q_n^2} = \frac{f_0}{2} \cdot e^{-Q_{th}^2/2Q_n^2} = \frac{1}{4\sqrt{3}\ \tau} \cdot e^{-Q_{th}^2/2Q_n^2}$$

Thus, the required threshold-to-noise ratio for a given frequency of noise hits f_n is

$$\frac{Q_T}{Q_n} = \sqrt{-2\log(4\sqrt{3}\ f_n \tau)} \approx \sqrt{-2\log\left(\frac{f_n}{f_P}\right)},$$

where f_P is the peaking frequency of the shaper

Note that product of noise rate and shaping time $f_n\tau$ determines the required threshold-to-noise ratio, i.e. for a given threshold-to-noise ratio the noise rate is higher at short shaping times

$\Rightarrow$ The noise rate for a given threshold-to-noise ratio is proportional to bandwidth.

$\Rightarrow$ To obtain the same noise rate, a fast system requires a larger threshold-to-noise ratio than a slow system with the same noise level.

Efficiency vs. Occupancy

Frequently a threshold discriminator system is used in conjunction with other detectors that provide additional information, for example the time of a desired event.

In a collider detector the time of beam crossings is known, so the output of the discriminator is sampled at specific times.

The number of recorded noise hits then depends on

1. the sampling frequency (e.g. bunch crossing frequency) f_S
2. the width of the sampling interval Δt, which is determined by the time resolution of the system.

The product $f_S \Delta t$ determines the fraction of time the system is open to recording noise hits, so the rate of recorded noise hits is $f_S \Delta t\, f_n$.

Often it is more interesting to know the probability of finding a noise hit in a given interval, i.e. the occupancy of noise hits, which can be compared to the occupancy of signal hits in the same interval.

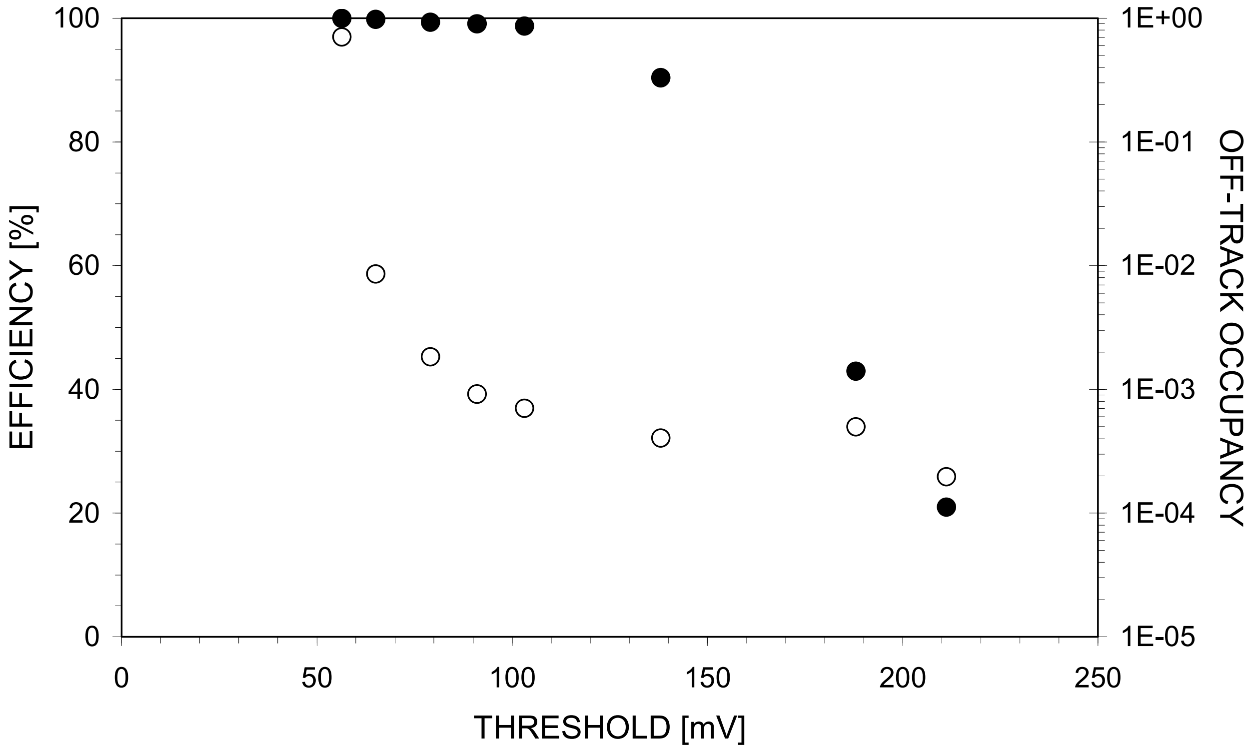
This is the situation in a storage pipeline, where a specific time interval is read out after a certain delay time (e.g. trigger latency)

The occupancy of noise hits in a time interval Δt:

$$P_n = \Delta t \cdot f_n = \frac{\Delta t}{2\sqrt{3}\ \tau} \cdot e^{-Q_T^2/2Q_n^2}$$

i.e. the occupancy falls exponentially with the square of the threshold-to-noise ratio.

Example of noise occupancy (open circles) and efficiency (solid circles) vs. threshold in a practical detector module:



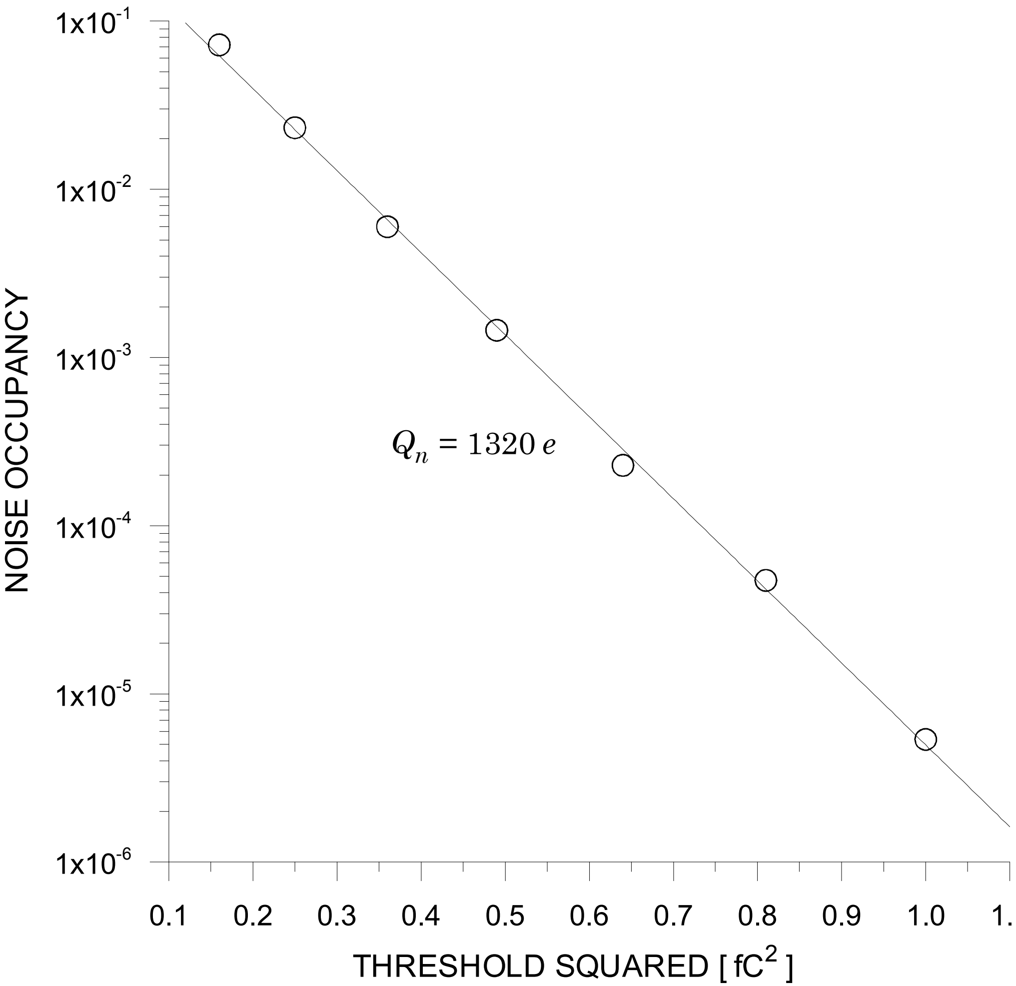
Note that an extended overlap region of high efficiency and low noise occupancy is desired.

The dependence of occupancy on threshold can be used to measure the noise level.

$$\log P_n = \log\left(\frac{\Delta t}{2\sqrt{3}\ \tau}\right) - \frac{1}{2}\left(\frac{Q_T}{Q_n}\right)^2,$$

so the *slope* of log P_n vs. Q_T^2 yields the noise level.

This analysis is *independent of the details of the shaper*, which affect only the offset.



2. Timing Measurements

Pulse height measurements discussed up to now emphasize accurate measurement of signal charge.

- Timing measurements optimize determination of time of occurrence.
- For timing, the figure of merit is not signal-to-noise, but slope-to-noise ratio.

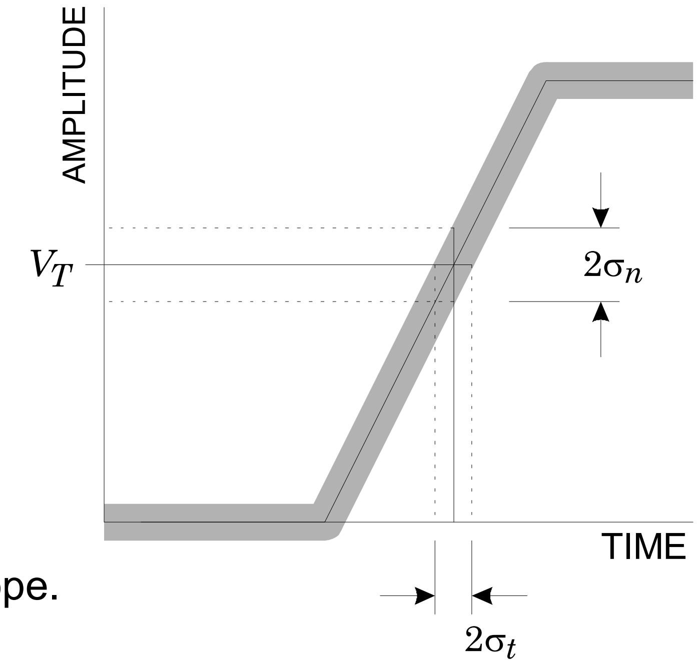
Consider the leading edge of a pulse fed into a threshold discriminator (comparator).

The instantaneous signal level is modulated by noise.

⇒ time of threshold crossing fluctuates

$$\sigma_t = \frac{\sigma_n}{\left.\dfrac{dV}{dt}\right|_{V_T}} \approx \frac{t_r}{S/N}$$

t_r = rise time



Typically, the leading edge is not linear, so the optimum trigger level is the point of maximum slope.

Pulse Shaping

Consider a system whose bandwidth is determined by a single RC integrator.

The time constant of the RC low-pass filter determines the

- rise time (and hence dV/dt)
- amplifier bandwidth (and hence the noise)

Time dependence: $V_o(t) = V_0(1 - e^{-t/\tau})$

The rise time is commonly expressed as the interval between the points of 10% and 90% amplitude

$$t_r = 2.2\ \tau$$

In terms of bandwidth

$$t_r = 2.2\ \tau = \frac{2.2}{2\pi\ f_u} = \frac{0.35}{f_u}$$

Example: An oscilloscope with 100 MHz bandwidth has 3.5 ns rise time.

For a cascade of amplifiers: $t_r \approx \sqrt{t_{r1}^2 + t_{r2}^2 + \ \ldots\ + t_{rn}^2}$

Choice of Rise Time in a Timing System

Assume a detector pulse with peak amplitude V_0 and a rise time t_c passing through an amplifier chain with a rise time t_{ra}.

1. amplifier rise time $\gg$ signal rise time:

$$\text{Noise} \propto \sqrt{f_u} \propto \sqrt{\frac{1}{t_{ra}}}$$

$$\frac{dV}{dt} \propto \frac{1}{t_{ra}} \propto f_u$$

increase in bandwidth $\Rightarrow$ improvement in dV/dt outweighs increase in noise.

2. amplifier rise time $\ll$ signal rise time

increase in noise without increase in dV/dt

Optimum: The amplifier rise time should be chosen to match the signal rise time.

Differentiation time constant: choose greater than rise time constant

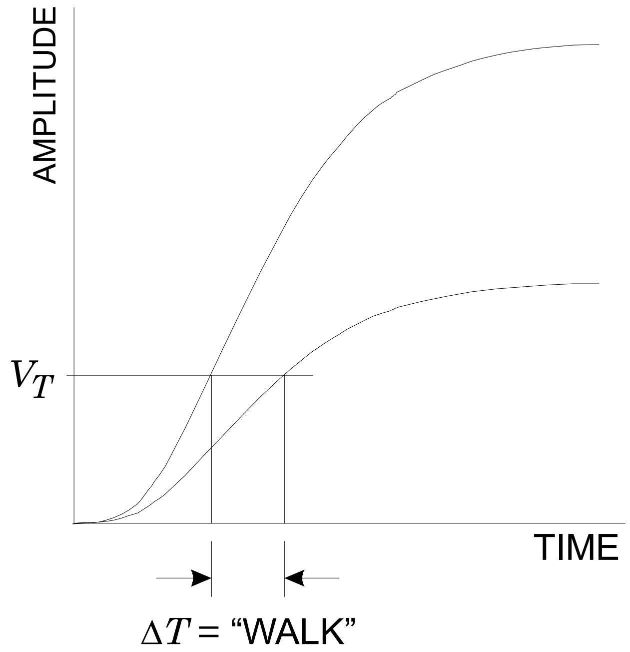
($\tau_{diff} = 10\tau_{\text{int}}$ incurs 20% loss in pulse height)

Time Walk

For a fixed trigger level the time of threshold crossing
depends on pulse amplitude.

⇒ Accuracy of timing measurement limited by

- jitter (due to noise)
- time walk (due to amplitude variations)



If the rise time is known, "time walk" can be compensated in software event-by-event by measuring the pulse height and correcting the time measurement.

This technique fails if both amplitude and rise time vary, as is common.

In hardware, time walk can be reduced by setting the threshold to the lowest practical level, or by using amplitude compensation circuitry, e.g. constant fraction triggering.

Lowest Practical Threshold

Single RC integrator has maximum slope at t= 0: $\frac{d}{dt}(1-e^{-t/\tau}) = \frac{1}{\tau}\; e^{-t/\tau}$

However, the rise time of practically all fast timing systems is determined by multiple time constants.

For small t the slope at the output of a single RC integrator is linear, so initially the pulse can be approximated by a ramp $\alpha\, t$.

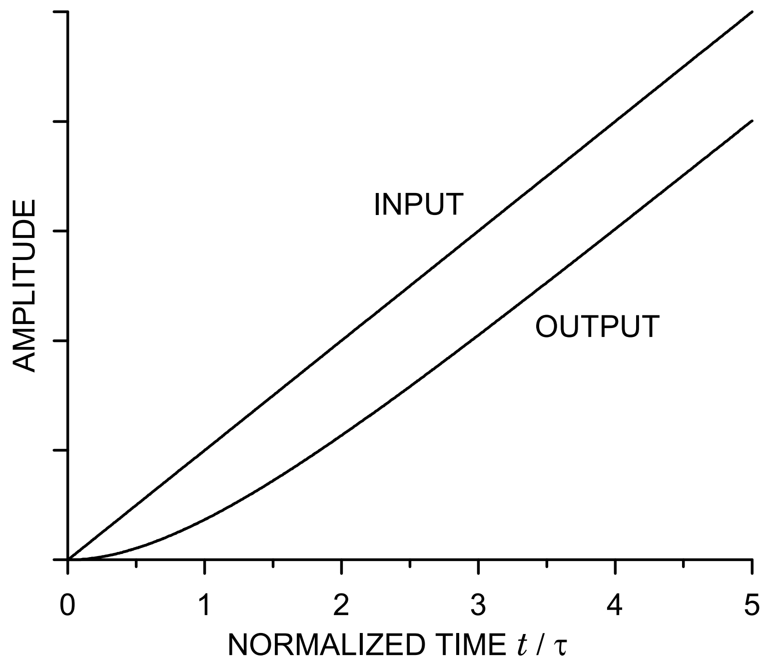
Response of the following integrator

$$V_i = \alpha\; t \quad \rightarrow \quad V_o = \alpha(t-\tau) - \alpha\;\tau\; e^{-t/\tau}$$

$\Rightarrow$ The output is delayed by τ
and curvature is introduced at small t.

Output attains 90% of input slope after $t = 2.3\tau$.

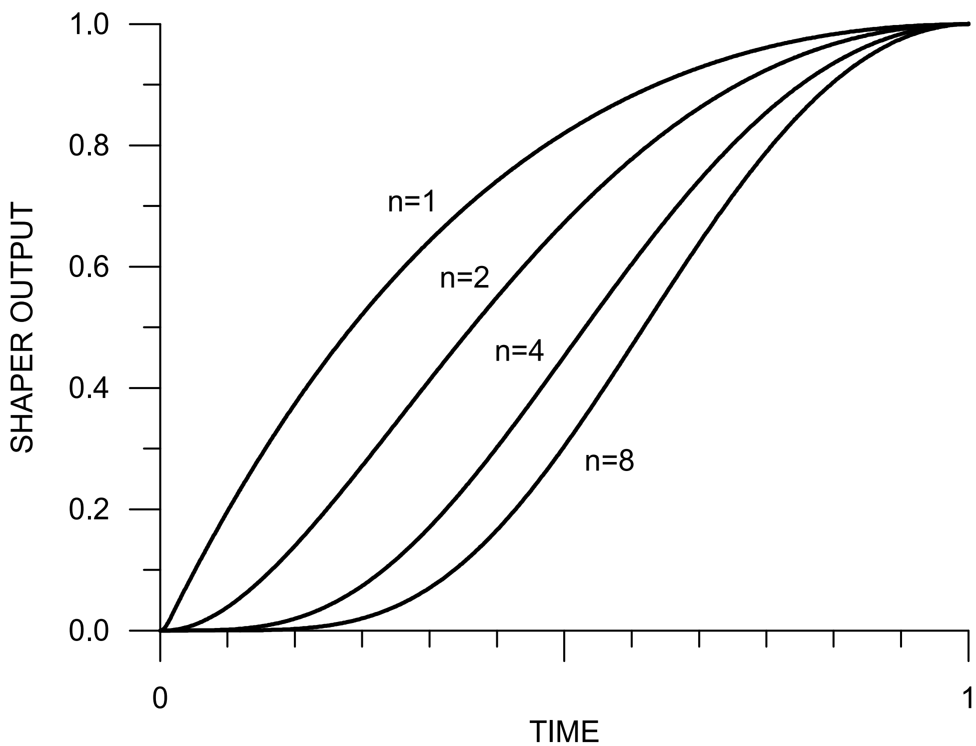
Delay for n integrators= $n\tau$



Additional RC integrators introduce more curvature at the beginning of the pulse.

Output pulse shape for multiple *RC* integrators

(normalized to preserve the peaking time, $\tau_n = \tau_{n-1} / n$)



Increased curvature at beginning of pulse limits the minimum threshold for good timing.

⇒ One dominant time constant best for timing measurements

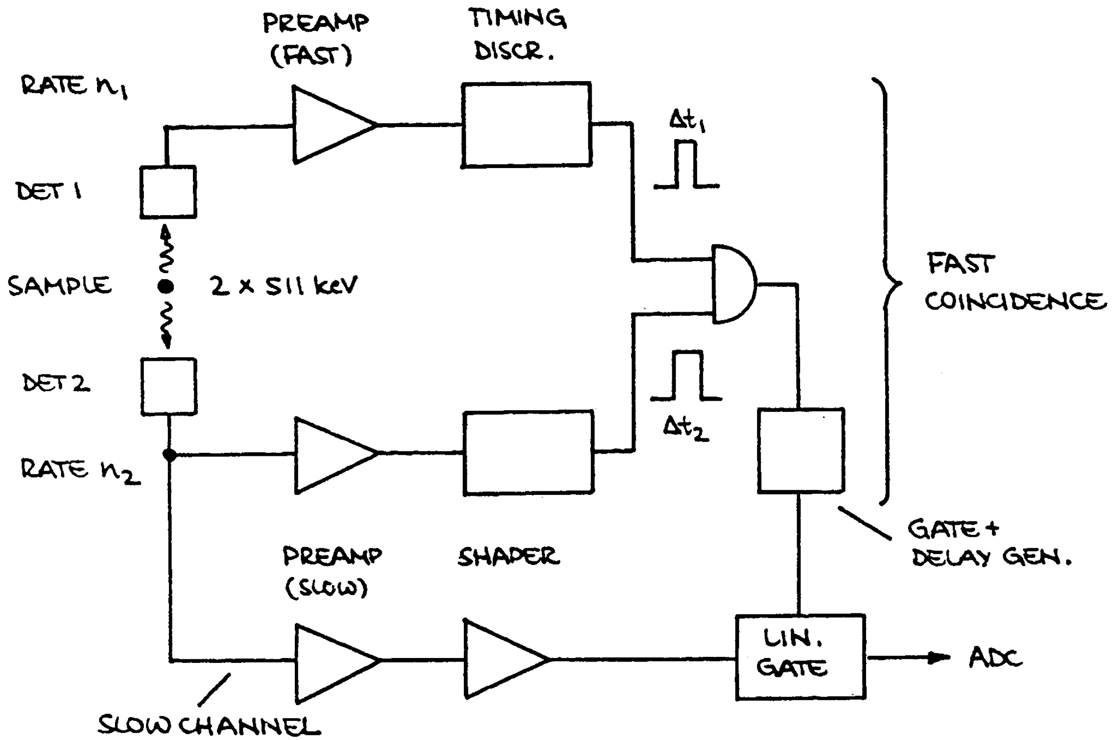
Unlike amplitude measurements, where multiple integrators are desirable to improve pulse symmetry and count rate performance.

Example: $\gamma - \gamma$ coincidence (as used in positron emission tomography)

Positron annihilation emits two collinear 511 keV photons.

Each detector alone will register substantial background.

Non-coincident background can be suppressed by requiring simultaneous signals from both detectors.



- Each detector feeds a fast timing channel.
- The timing pulses are combined in an AND gate (coincidence unit). The AND gate only provides an output if the two timing pulses overlap.
- The coincidence output is used to open a linear gate, that allows the energy signal to pass to the ADC.

This arrangement accommodates the contradictory requirements of timing and energy measurements. The timing channels can be fast, whereas the energy channel can use slow shaping to optimize energy resolution ("fast-slow coincidence").

Chance coincidence rate

Two random pulse sequences have some probability of coincident events.

If the event rates in the two channels are n_1 and n_2, and the timing pulse widths are Δt_1 and Δt_2, the probability of a pulse from the first source occurring in the total coincidence window is

$$P_1 = n_1 \cdot (\Delta t_1 + \Delta t_2)$$

The coincidence is "sampled" at a rate n_2 , so the chance coincidence rate is

$$n_c = P_1 \cdot n_2$$
$$n_c = n_1 \cdot n_2 \cdot (\Delta t_1 + \Delta t_2)$$

i.e. in the arrangement shown above, the chance coincidence rate increases with the *square* of the source strength.

Example: $n_1 = n_2 = 10^6\ \text{s}^{-1}$

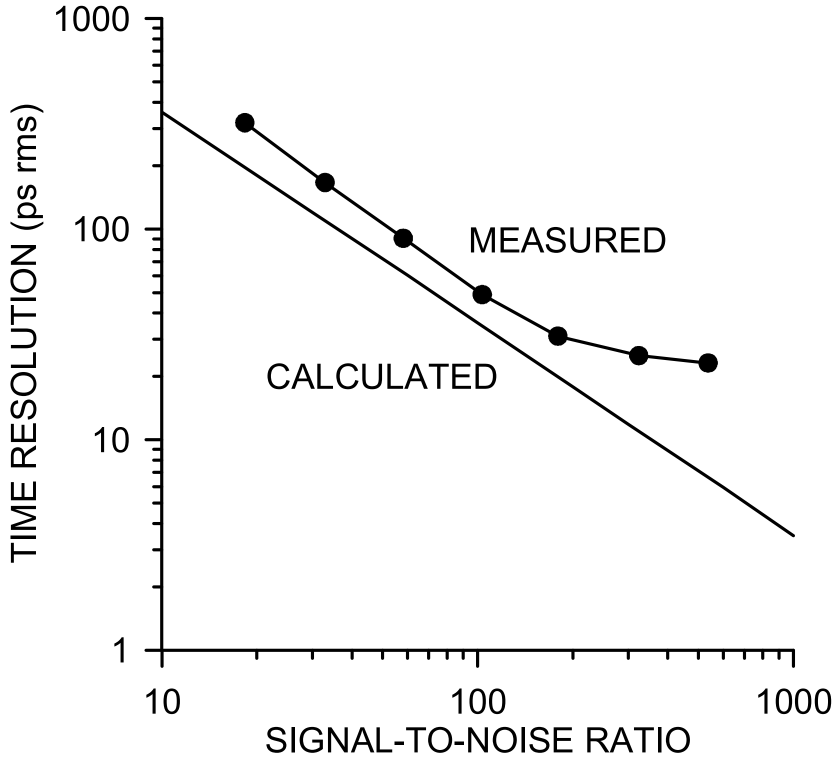
$$\Delta t_1 = \Delta t_2 = 5\ \text{ns} \quad \Rightarrow \quad n_c = 10^4\ \text{s}^{-1}$$

Fast Timing: Comparison between theory and experiment

Time resolution $\propto 1/(S/N)$

At S/N<100 the measured curve lies above the calculation because the timing discriminator limited the rise time.

At high S/N the residual jitter of the time digitizer limits the resolution.



For more details on fast timing with semiconductor detectors, see

H. Spieler, IEEE Trans. Nucl. Sci. **NS-29/3** (1982) 1142.

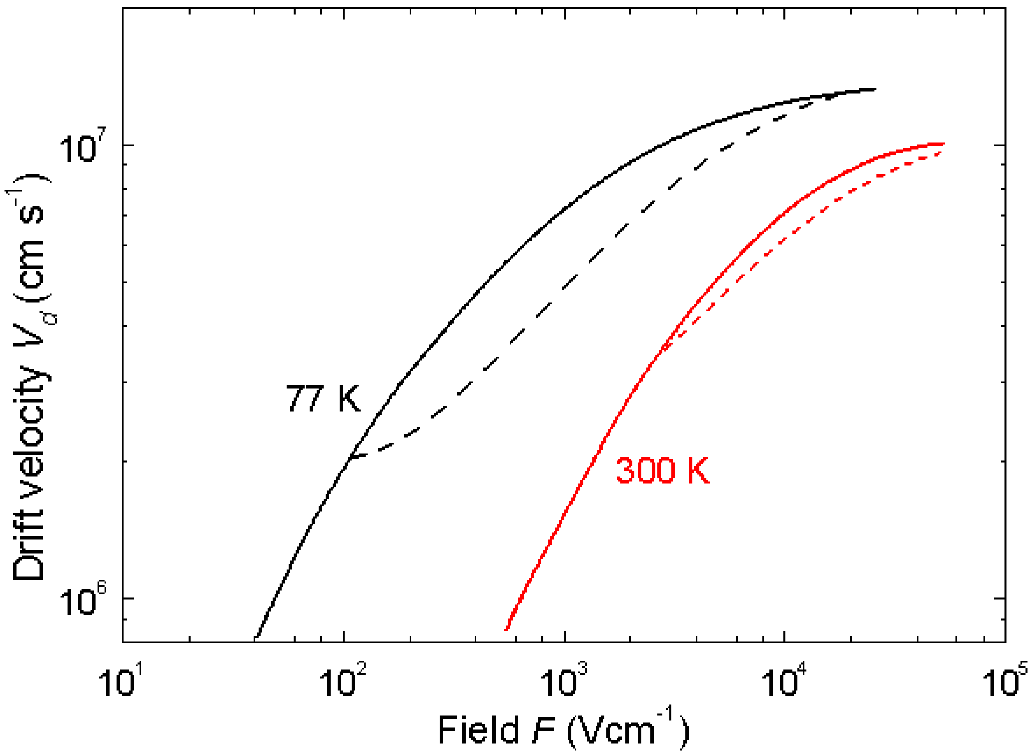
Improved Timing at Low Temperatures?

Carrier mobility increases
at low temperatures.

Electron drift velocity in Si:
(low doping levels)

solid: $E \| (111)$

dashed: $E \| (100)$



Jacobini et al. Solid State Elec 20/2 (1977) 77-89

At low fields ~10-fold increase, but saturation velocity at 77K only increases 30%,
so at the high fields optimal for timing only modest improvement.

Ionization coefficient α(77K)/α(300K) ≈ 2, so maximum bias voltage reduced (breakdown).

3. Digitization

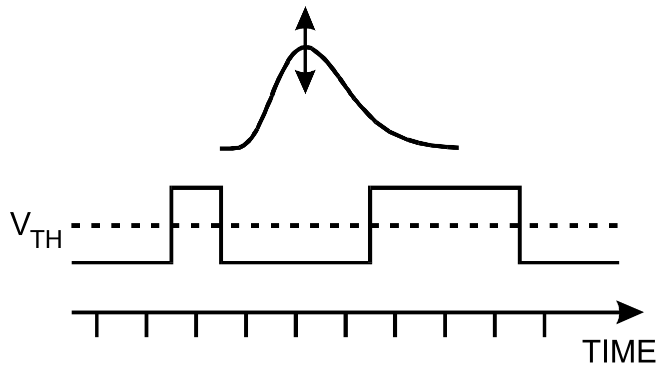
Elements of Digital Electronics

Basic differences

Analog signals have variable amplitude

Digital have constant amplitude, but variable timing

Presence of signal at specific times is evaluated:
(does the signal level exceed threshold?)



Transmission capacity of a digital link (bits per second)

Shannon's theorem:

$$C = B \cdot \log_2 \left(1 + \frac{S}{N} \right)$$

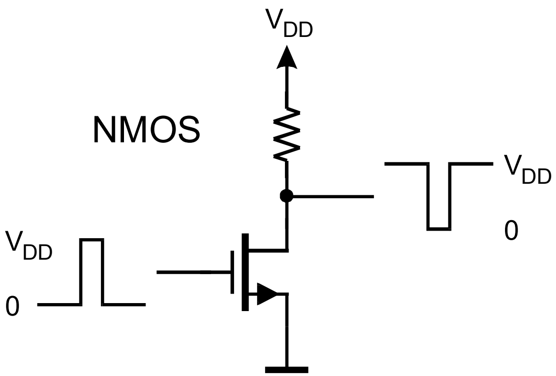
B = Bandwidth
S = Signal (pulse amplitude)
N = Noise

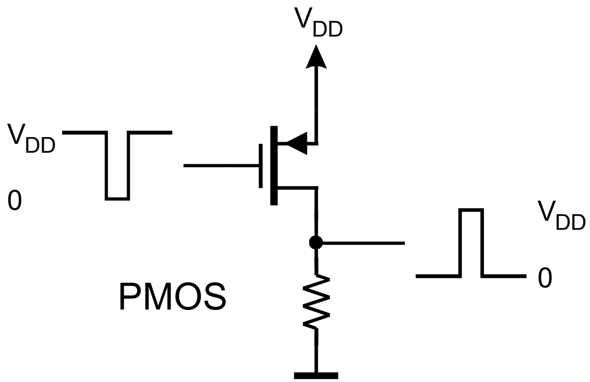
Noise enters, because near the switching threshold, digital elements are amplifiers.

If the noise is due to cross-talk from other digital signals,
increasing the pulse amplitude will not improve S/N

Digital electronics not just a matter of "yes" or "no" – real systems must also deal with "maybe".

LOGIC CIRCUITRY - Modern logic uses MOS technology.



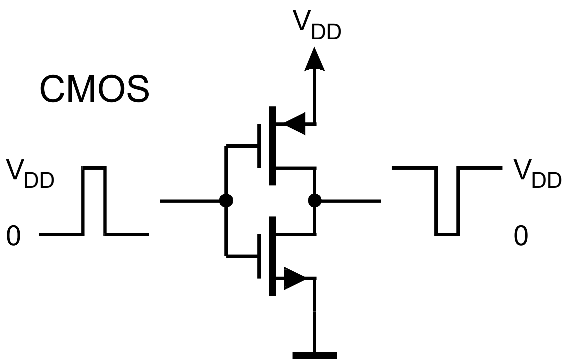


Transistor conducts when input is high.

PMOS: Transistor conducts when input is low.

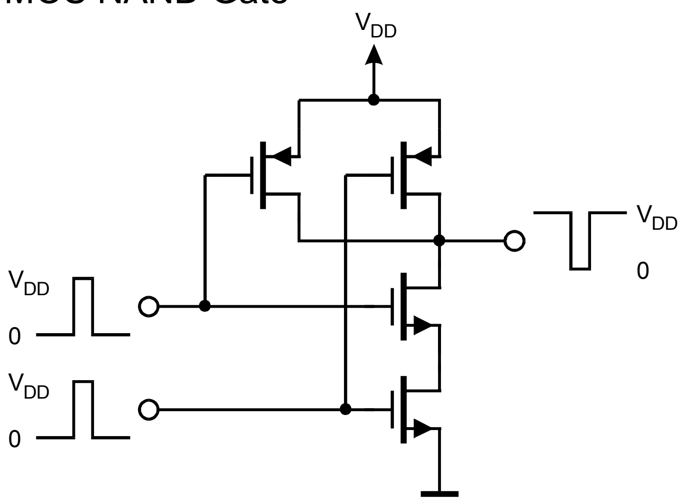
CMOS – combine NMOS and PMOS $\Rightarrow$ significant power reduction

CMOS Inverter



Current flows only during transition.

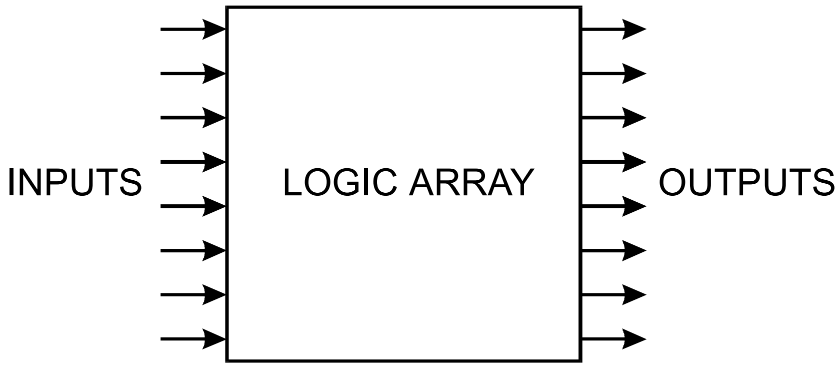
CMOS NAND Gate



LOGIC ARRAYS

Complex logic systems are not designed using individual gates.

Instead, logic functions are described in a high-level language (e.g. VHDL) and synthesized using design libraries (in custom ICs, “ASICs”) or programmable logic arrays.



Typical: 512 pads usable for inputs and outputs, ~10^6 gates, ~100K memory

Software also generates “test vectors” that can be used to test finished parts.

POWER DISSIPATION AND PROPAGATION DELAYS

Energy dissipated in wiring resistance R:

$$E = \int i^2(t) R \; dt$$

$$i(t) = \frac{V}{R} \exp\left(-\frac{t}{RC}\right)$$

$$E = \frac{V^2}{R} \int_0^{\infty} \exp\left(-2t/RC\right) dt = \frac{1}{2} C V^2$$

If pulses (rising + falling edge transitions) occur at frequency f,

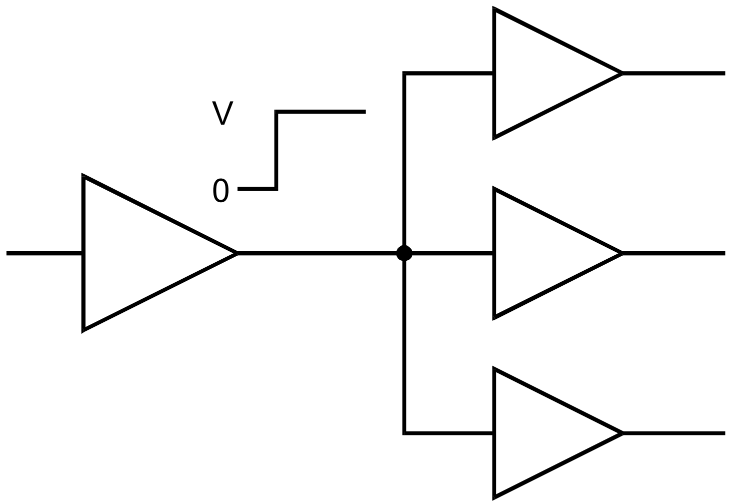
$$P = fCV^2$$

Power dissipation increases with clock frequency and (logic swing)^2.

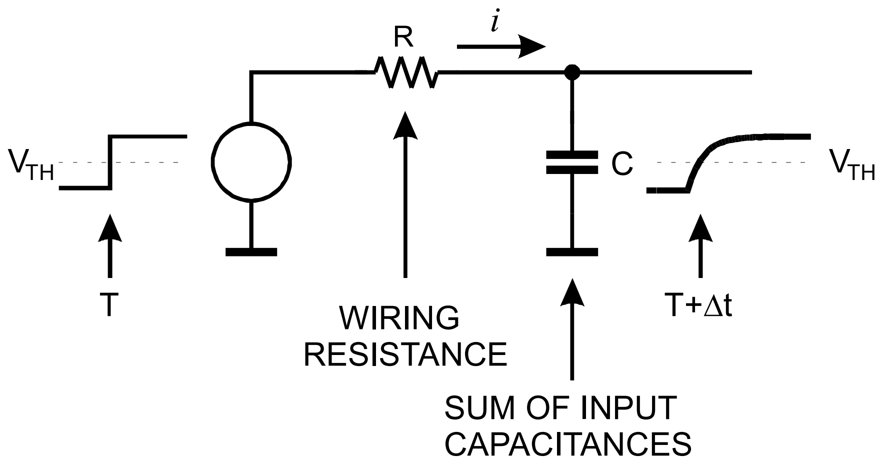
RC time constant also introduces time delay in addition to propagation delay of gates/buffers!

Depends on wiring resistance and total load capacitance.

CASCADED CMOS STAGES



EQUIVALENT CIRCUIT



Digitization of Pulse Height and Time – Analog to Digital Conversion

For data storage and subsequent analysis the analog signal at the shaper output must be digitized.

Important parameters for ADCs used in detector systems:

1. Resolution
   The "granularity" of the digitized output
2. Differential Non-Linearity
   How uniform are the digitization increments?
3. Integral Non-Linearity
   Is the digital output proportional to the analog input?
4. Conversion Time
   How much time is required to convert an analog signal to a digital output?
5. Count-Rate Performance
   How quickly can a new conversion commence after completion of a prior one without introducing deleterious artifacts?
6. Stability
   Do the conversion parameters change with time?

Instrumentation ADCs used in industrial data acquisition and control systems share most of these requirements. However, detector systems place greater emphasis on differential non-linearity and count-rate performance. The latter is important, as detector signals often occur randomly, in contrast to measurement systems where signals are sampled at regular intervals.

1. Resolution

Digitization incurs approximation, as a continuous signal distribution is transformed into a discrete set of values. To reduce the additional errors (noise) introduced by digitization, the discrete digital steps must correspond to a sufficiently small analog increment.

Simplistic assumption:

Resolution is defined by the number of output bits, e.g. 13 bits $\rightarrow \frac{\Delta V}{V} = \frac{1}{8192} = 1.2 \cdot 10^{-4}$

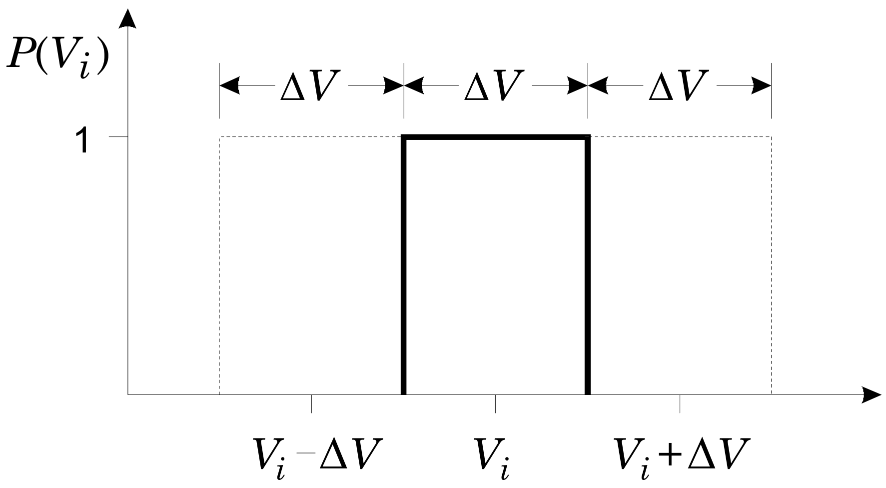
True Measure: Channel Profile

Plot probability vs. pulse amplitude that a pulse height corresponding to a specific output bin is actually converted to that address.

Ideal ADC:

Measurement accuracy:

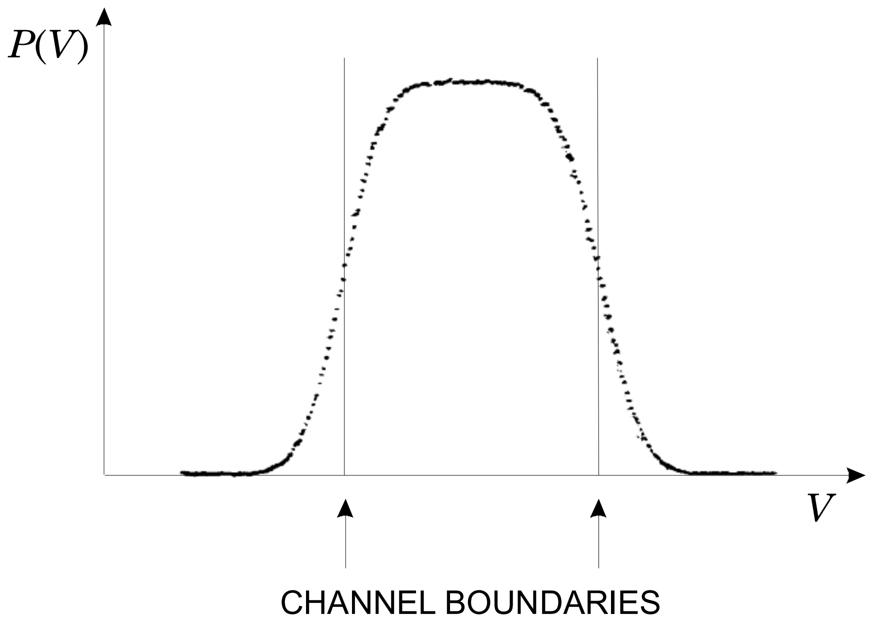
- If all counts of a peak fall in one bin, the resolution is ΔV.
- If the counts are distributed over several bins, peak fitting can yield a resolution of 10^{-1} – 10^{-2} ΔV, *if the distribution is known and reproducible* (not necessarily a valid assumption for an ADC).



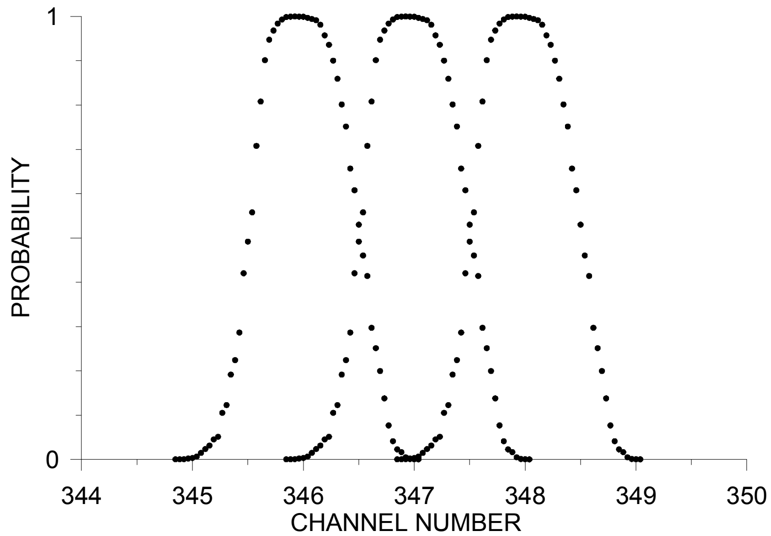
In reality, the channel profile is not rectangular as sketched above.

Electronic noise in the threshold discrimination process that determines the channel boundaries "smears" the transition from one bin to the next.

Measured channel profile (13 bit ADC)



The profiles of adjacent channels overlap.

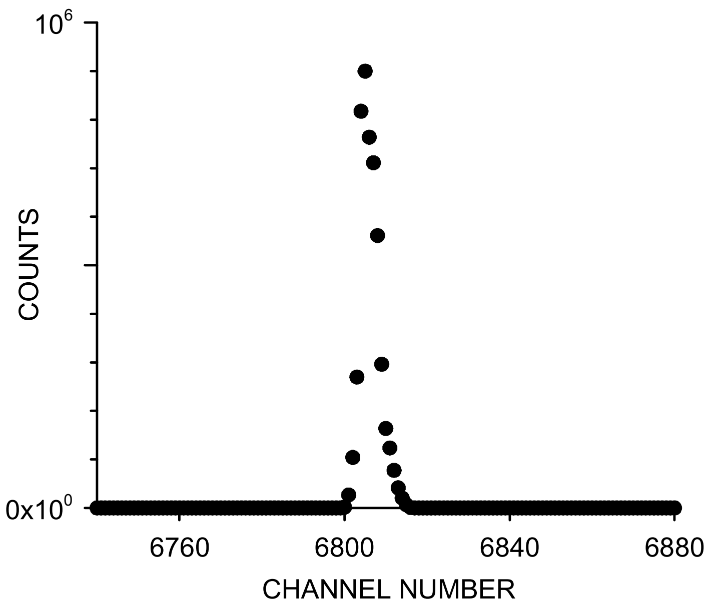


Channel profile can be checked quickly by applying the output of a precision pulser to the ADC.

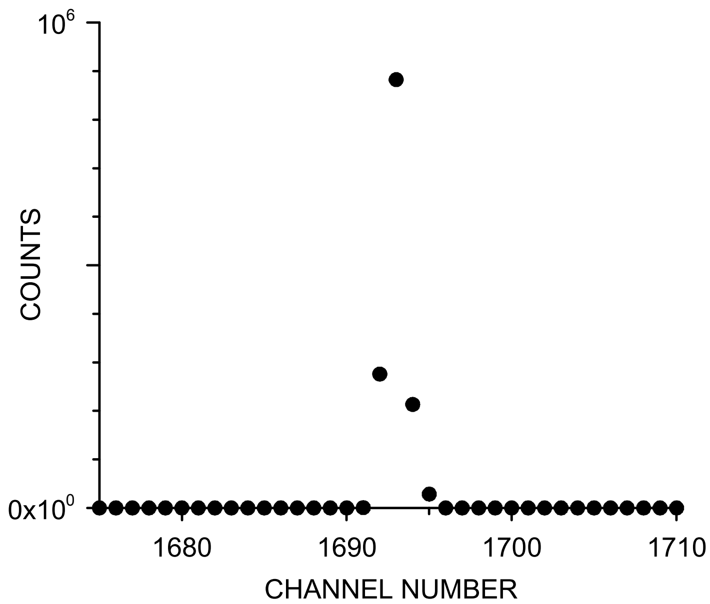
If the pulser output has very low noise, i.e. the amplitude jitter is much smaller than the voltage increment corresponding to one ADC channel or bin, all pulses will be converted to a single channel, with only a small fraction appearing in the neighbor channels.

Example of an ADC whose digital resolution is greater than its analog resolution:

8192 ch conversion range (13 bits)



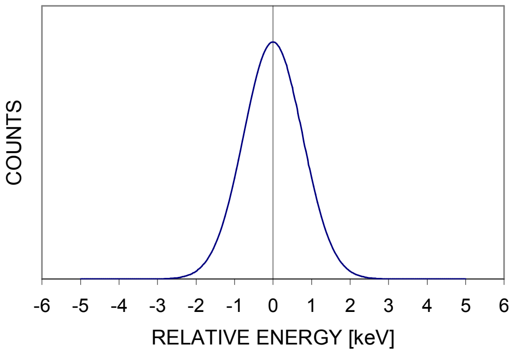
2048 ch conversion range (11 bits)



2K range provides maximum resolution – higher ranges superfluous.

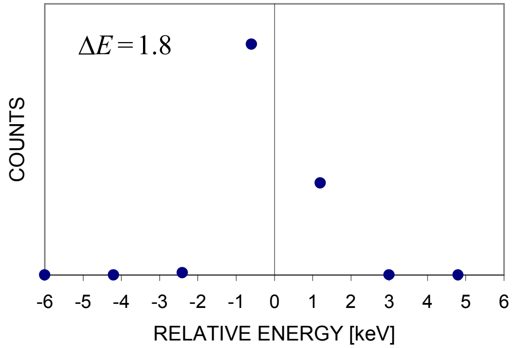
How much ADC Resolution is Required?

Example: Detector resolution ΔE
1.8 keV FWHM

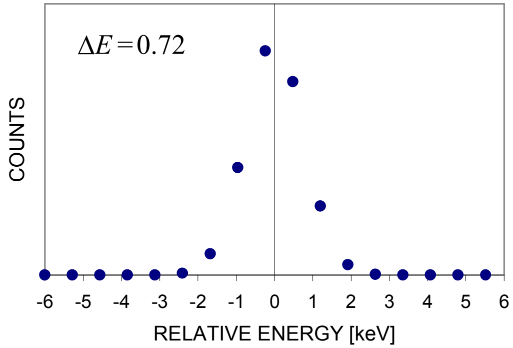


Digitized spectra for various ADC resolutions (bin widths)

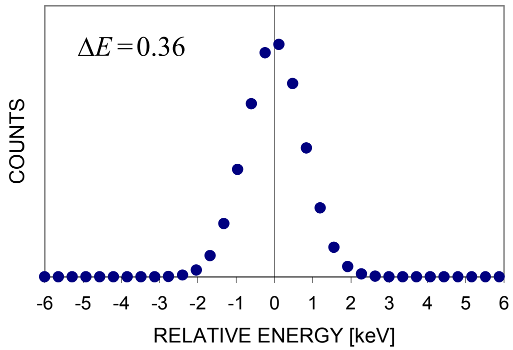
ΔE= 1.8 keV = 1 x FWHM



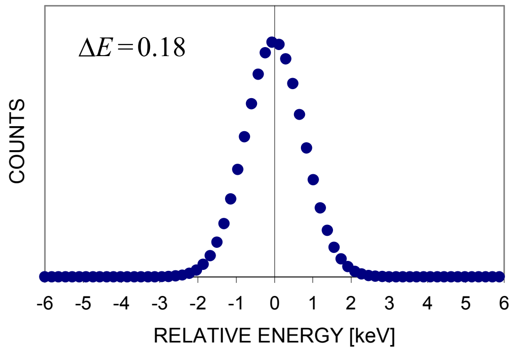
ΔE= 0.72 keV = 0.4 x FWHM



ΔE= 0.36 keV = 0.2 x FWHM



ΔE= 0.18 keV = 0.1 x FWHM



Fitting can determine centroid position to fraction of bin width even with coarse digitization,
if only a single peak is present and the line shape is known.

2. Differential Non-Linearity

Differential non-linearity is a measure of the non-uniformity of channel profiles over the range of the ADC.

Depending on the nature of the distribution, either a peak or an rms specification may be appropriate.

$$DNL = \max \left\{ \frac{\Delta V(i)}{\langle \Delta V \rangle} - 1 \right\} \quad \text{or} \quad DNL = \text{r.m.s.} \left\{ \frac{\Delta V(i)}{\langle \Delta V \rangle} - 1 \right\}$$

where $\langle \Delta V \rangle$ is the average channel width and

$\Delta V(i)$ is the width of an individual channel.

Differential non-linearity of < ±1% max. is typical,

but state-of-the-art ADCs can achieve 10^{-3} rms,

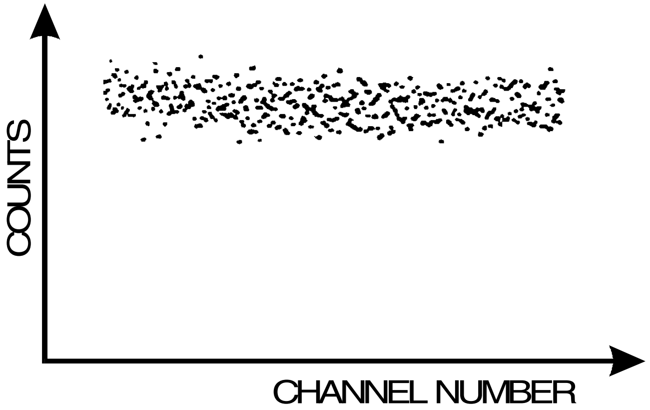
i.e. the variation is comparable to the statistical fluctuation for 10^6 random counts.

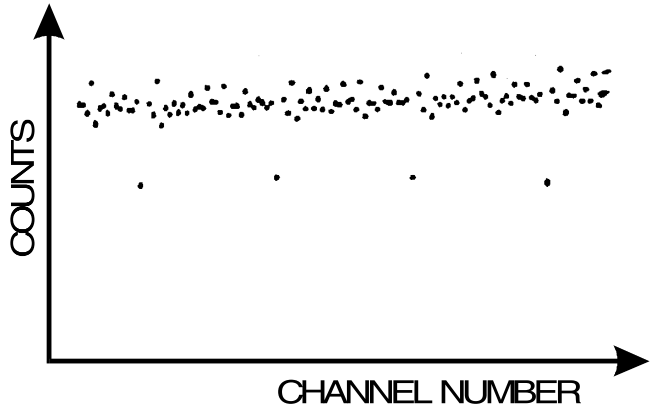
Typical differential non-linearity patterns

“white” input spectrum, suppressed zero

Vertical scale 10x larger than left

↓





An ideal ADC would show an equal number of counts in each bin.

The spectrum to the left shows a random pattern, but
note the multiple periodicities visible in the right hand spectrum.

Note: Instrumentation ADCs are often specified with an accuracy of ±0.5 LSB (least significant bit) or more, so

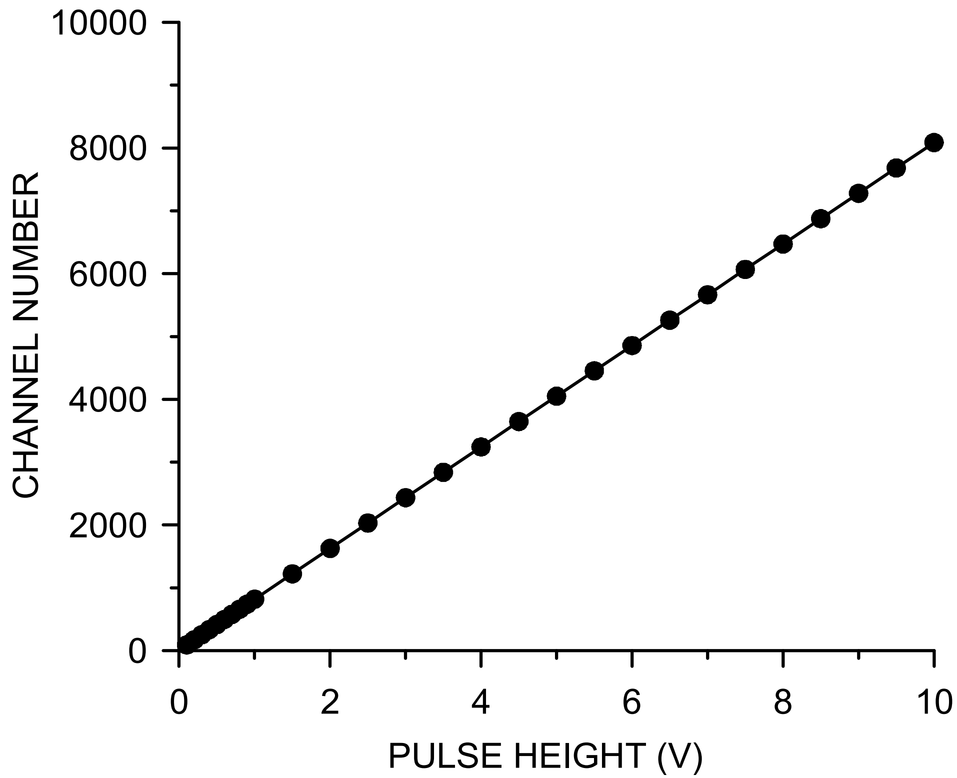
1. the differential non-linearity may be 50% or more,

2. the response may be non-monotonic

$\Rightarrow$ output may decrease when input rises.

3. Integral Non-Linearity

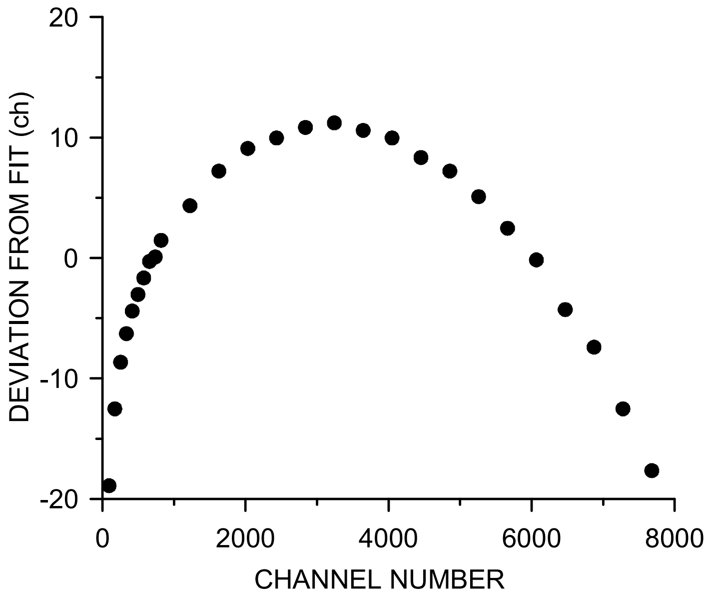
Integral non-linearity measures the deviation from proportionality of the measured amplitude to the input signal level.



The dots are measured values and the line is a fit to the data.

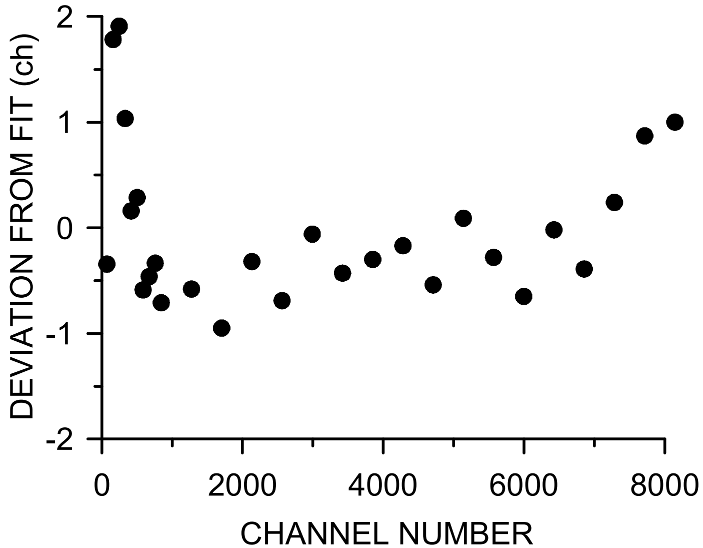
This plot is not very useful if the deviations from linearity are small.

Plotting the deviations of the measured points
from the fit yields a more useful result.



Integral non-linearity measured with a
400 ns wide input pulse

The linearity of an ADC can depend on the
input pulse shape and duration,
due to bandwidth limitations in the circuitry.



Increasing the pulse width to 3 μs
improved
the linearity significantly:

4. Conversion Time

During the acquisition of a signal the system cannot accept a subsequent signal (“dead time”)

Dead Time =

signal acquisition time	$\rightarrow$	time-to-peak + const.
+ conversion time	$\rightarrow$	can depend on pulse height
+ readout time to memory	$\rightarrow$	depends on speed of data transmission and buffer memory access

Dead time affects measurements of yields or reaction cross-sections. Unless the event rate << 1/(dead time), it is necessary to measure the dead time, e.g. with a reference pulser fed simultaneously into the spectrum.

The total number of reference pulses issued during the measurement is determined by a scaler and compared with the number of pulses recorded in the spectrum.

Does a pulse-height dependent dead time mean that the correction is a function of pulse height?

Usually not. If events in different part of the spectrum are not correlated in time, i.e. random, they are all subject to the same average dead time (although this average will depend on the spectral distribution).

- Caution with correlated events!
  Example: Decay chains, where lifetime is < dead time.
  The daughter decay will be lost systematically.

5. Count Rate Effects

Problems are usually due to internal baseline shifts with event rate or undershoots following a pulse.

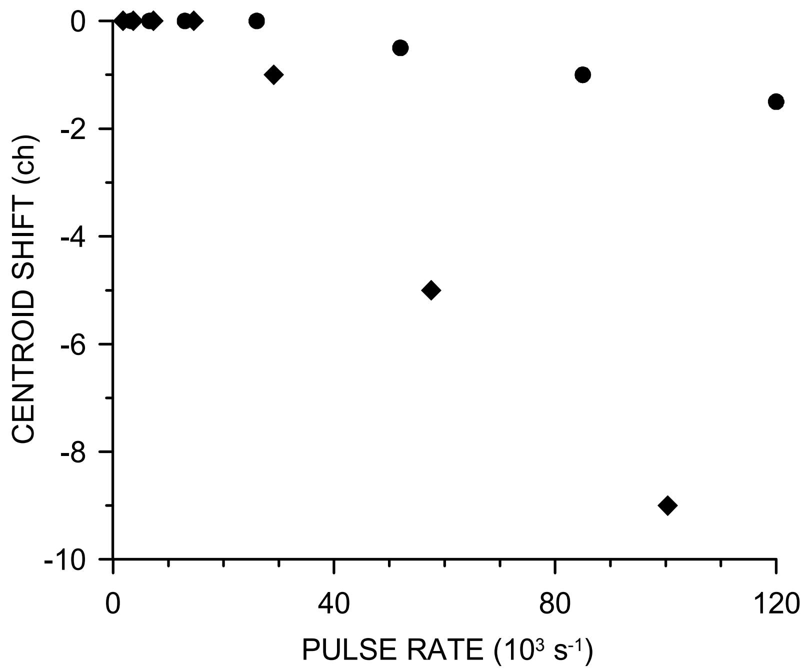
If signals occur at constant intervals, the effect of an undershoot will always be the same.

However, in a random sequence of pulses, the effect will vary from pulse to pulse.

⇒ spectral broadening

Baseline shifts tend to manifest themselves as a systematic shift in centroid position with event rate.

Centroid shifts for two 13 bit ADCs vs. random rate:



6. Stability

Stability vs. temperature is usually adequate with modern electronics in a laboratory environment.

- Note that temperature changes within a module are typically much smaller than ambient.

  However: Highly precise or long-term measurements require spectrum stabilization to compensate for changes in gain and baseline of the overall system.

  Technique: Using precision pulsers place a reference peak at both the low and high end of the spectrum.

  (Pk. Pos. 2) – (Pk. Pos. 1) $\rightarrow$ Gain, …

  then

  (Pk. Pos. 1) or (Pk. Pos. 2) $\rightarrow$ Offset

  Traditional Implementation: Hardware, spectrum stabilizer module

  Today, it is more convenient to determine the corrections in software.

  These can be applied to calibration corrections or used to derive an electrical signal that is applied to the hardware (simplest and best in the ADC).

Analog to Digital Conversion Techniques

1. Flash ADC

The input signal is applied to n comparators in parallel. The switching thresholds are set by a resistor chain, such that the voltage difference between individual taps is equal to the desired measurement resolution.

2^n comparators for n bits (8 bit resolution requires 256 comparators)

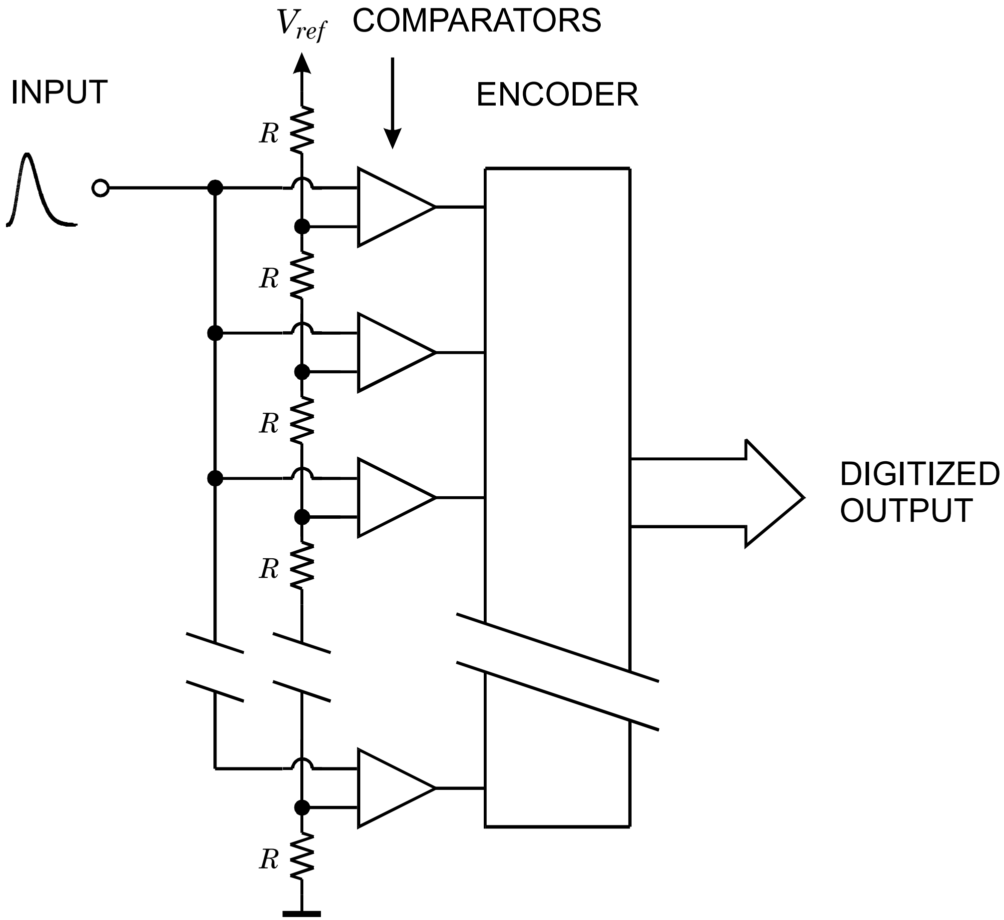
Feasible in monolithic ICs since the absolute value of the resistors in the reference divider chain is not critical, only the relative matching.

Advantage: short conversion time (<10 ns available)

Drawbacks:

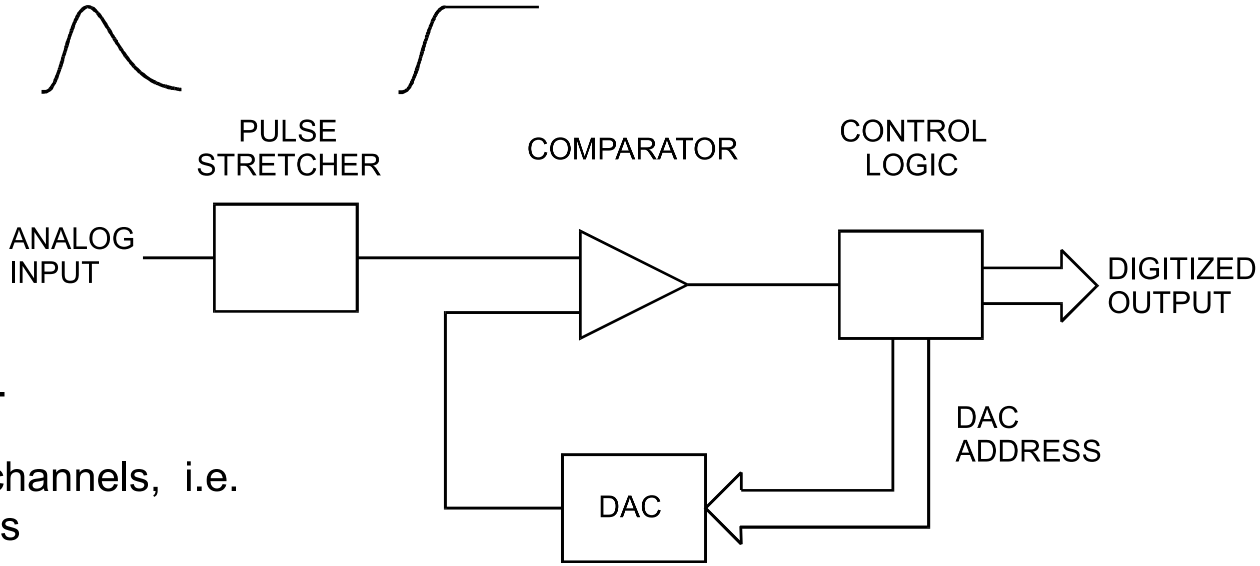
- limited accuracy (many comparators)
- power consumption
- Differential non-linearity ~ 1%
- High input capacitance

Speed is often limited by the analog driver feeding the input.



2. Successive Approximation ADC

Sequentially raise comparator threshold proportional to 2^n, 2^{n-1}, … 2^0 and set corresponding bit if the comparator output is high (DAC output < pulse height).



n conversion steps yield 2^n channels, i.e. 8K channels require 13 steps

Advantages: speed (~ μs)
high resolution
ICs (monolithic + hybrid) available

Drawback: Differential non-linearity (typ. 10 – 20%)

Reason: Resistors that set DAC output must be extremely accurate. For DNL < 1% the resistor determining the 2^{12} level in an 8K ADC must be accurate to < $2.4 \cdot 10^{-6}$.

DNL can be corrected by various techniques:

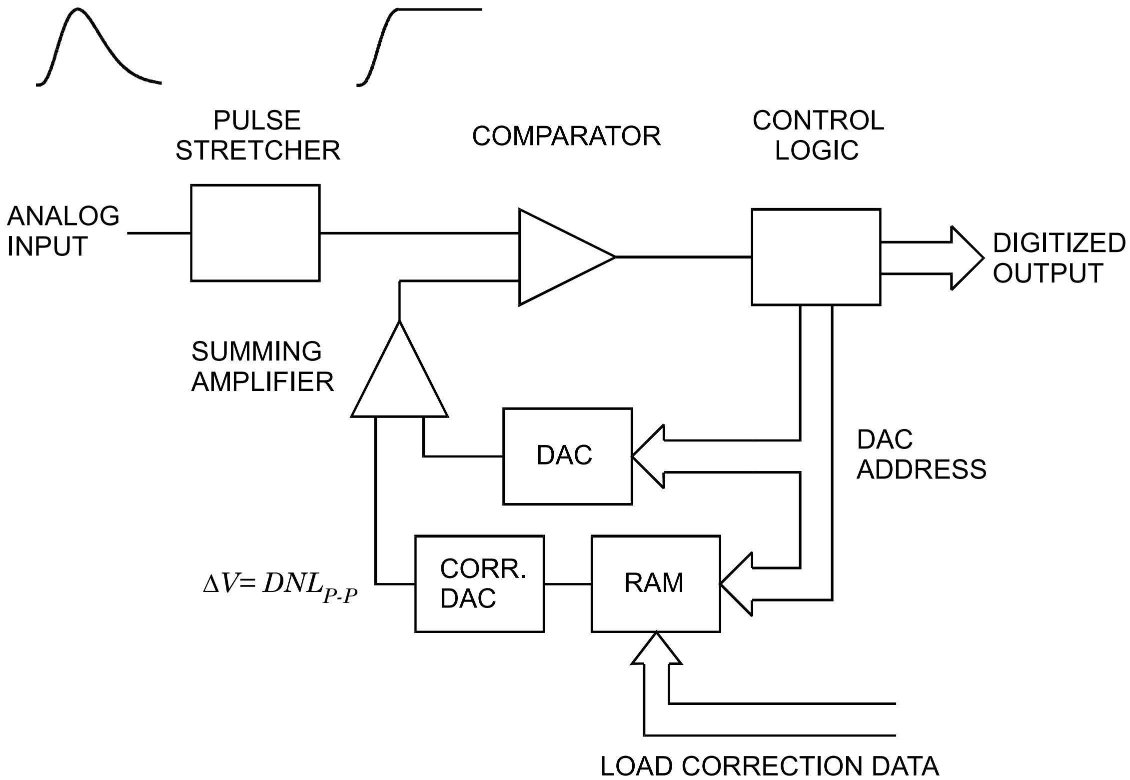
- averaging over many channel profiles for a given pulse amplitude ("sliding scale" or "Gatti principle")
- correction DAC ("brute force" application of IC technology)

The primary DAC output is adjusted by the output of a correction DAC to reduce differential non-linearity.

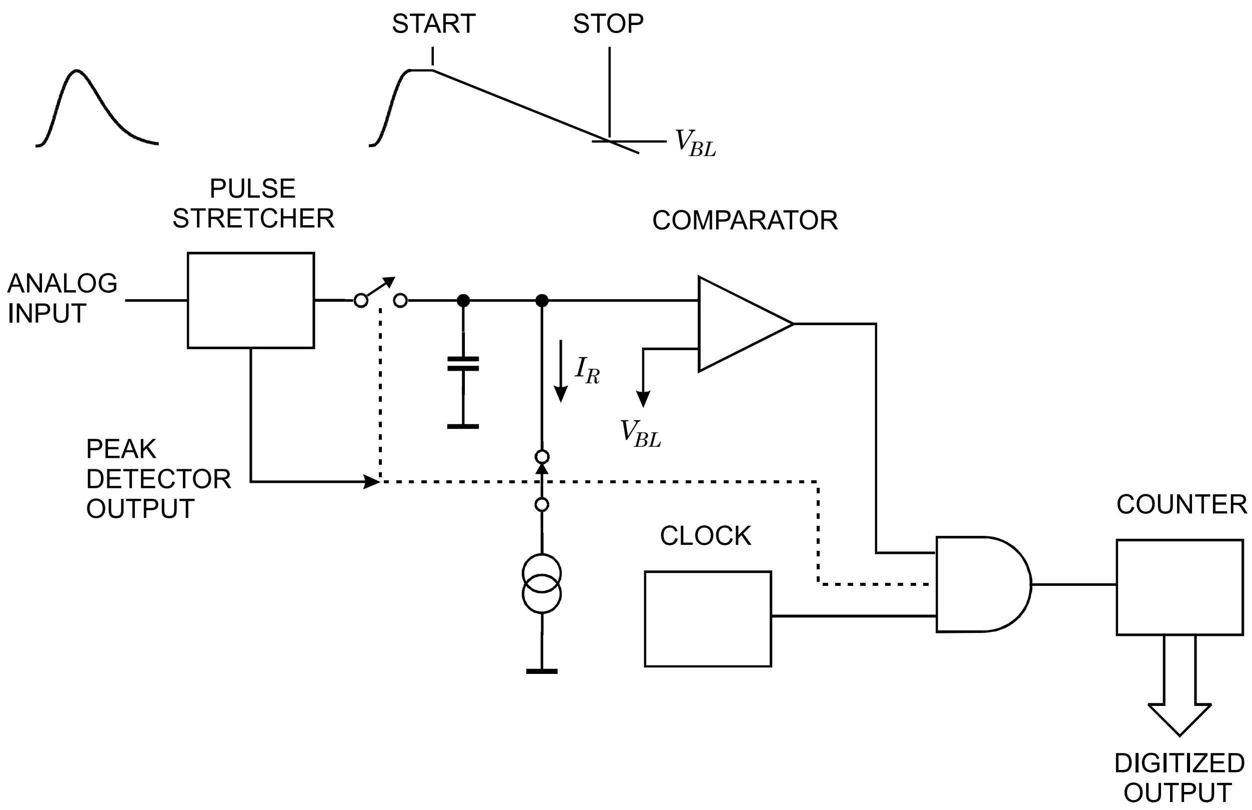
Correction data are derived from a measurement of DNL. Corrections for each bit are loaded into the RAM, which acts as a look-up table to provide the appropriate value to the correction DAC for each bit of the main DAC.

The range of the correction DAC must exceed the peak-to-peak differential non-linearity.

If the correction DAC has N bits, the maximum DNL is reduced by $1/2^{(N-1)}$ (if deviations are symmetrical).



3. Wilkinson ADC



The peak signal amplitude is acquired by a pulse stretcher and transferred to a memory capacitor.

Then, simultaneously,

1. the capacitor is disconnected from the stretcher,
2. a current source is switched on to linearly discharge the capacitor,
3. a counter is enabled to determine the number of clock pulses until the voltage on the capacitor reaches the baseline.

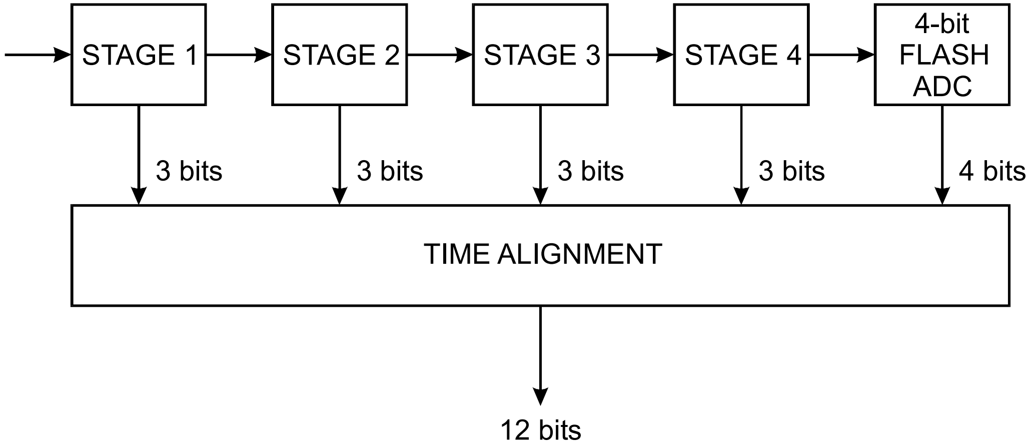
Advantage: excellent differential linearity (continuous conversion process)

Drawbacks: slow – conversion time = $n \cdot T_{clock}$ (n= channel number $\propto$ pulse height)
T_{clock}= 10 ns $\rightarrow T_{conv}$= 82 μs for 13 bits

Clock frequencies of 100 MHz typical, >400 MHz possible with excellent performance

“Standard” technique for high-resolution spectroscopy.

4. Pipelined ADCs

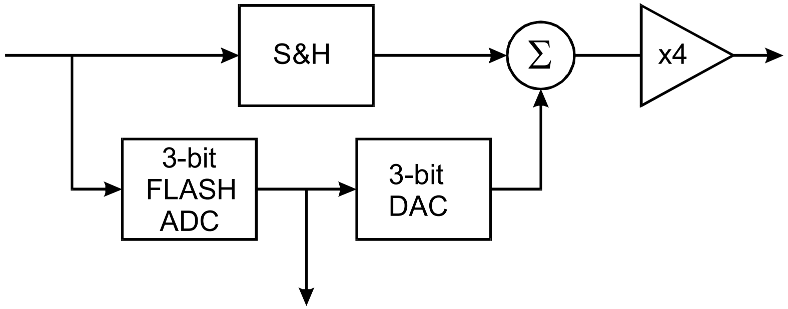


Most common architecture for high-speed high-resolution ADCs

Input to each stage is fed both to a sample and hold (S&H) and a 3-bit flash ADC.

The S&H maintains the signal level during conversion. The flash ADC quantizes its input to 3 bit accuracy. This output is fed to a DAC with 12 bit accuracy. The DAC's analog output is subtracted from the original signal and the difference signal is passed on to the next stage.

EACH STAGE



The last 4 bits are resolved by a 4-bit flash ADC.

As soon as a stage has passed its result to the next stage it can begin processing the next signal, so throughput is not determined by the total conversion time, but by the time per stage.

Since the interstage gain is only 4 (rather than 8 corresponding to 3 bits), each stage only contributes 2 bits of resolution. The extra bit is used for error correction.

Commercially available: 1 GS/s conversion rates with 8-bit resolution and a power dissipation of about 1.5 W.

Hybrid Analog-to-Digital Converters

Conversion techniques can be combined to obtain high resolution and short conversion time.

1. Flash + Successive Approximation or Flash + Wilkinson (Ramp Run-Down)

Utilize fast flash ADC for coarse conversion (*e.g.* 8 out of 13 bits)

Successive approximation or Wilkinson converter to provide fine resolution.
Limited range, so short conversion time: 256 ch with 100 MHz clock $\Rightarrow$ 2.6 μs

Results: 13 bit conversion in < 4 μs with excellent integral and differential linearity

2. Flash ADCs with Sub-Ranging

Not all applications require constant absolute resolution over the full range. Sometimes only *relative* resolution must be maintained, especially in systems with a very large dynamic range.

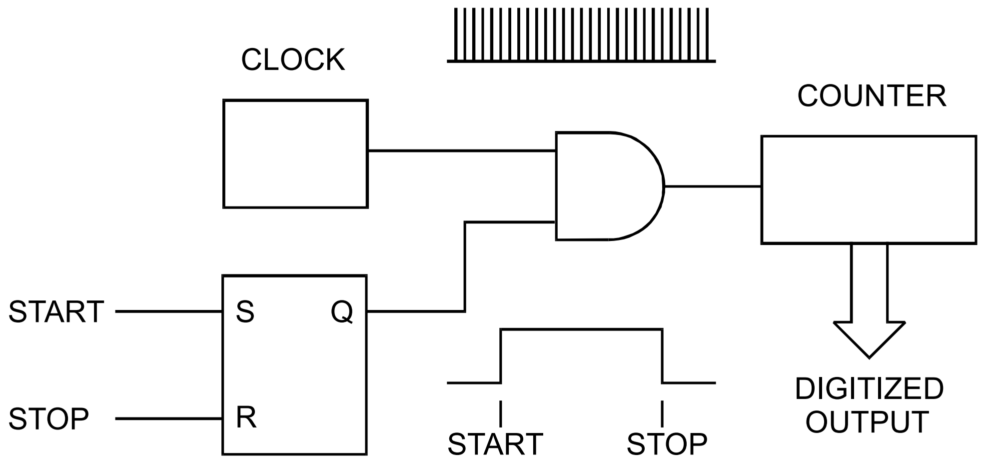
Precision binary divider at input to determine coarse range + fast flash ADC for fine digitization.

Example: Fast digitizer that fits in phototube base (FNAL)

17 to 18 bit dynamic range
Digital floating point output (4 bit exponent, 8+1 bit mantissa)
16 ns conversion time

Time Digitizers

1. Counter



Simplest arrangement: Count clock pulses between start and stop.

Limitation: Speed of counter
Current technology limits speed of counter system to about 1 GHz

$\Rightarrow$ Δt = 1 ns

Advantages: Simplicity
Multi-hit capability

2. Analog Ramp

Commonly used in high-resolution digitizers (Δt = 10 ps)

Principle:
Charge capacitor through switchable current source

Start pulse: turn on current source

Stop pulse: turn off current source

$\Rightarrow$ Voltage on storage capacitor

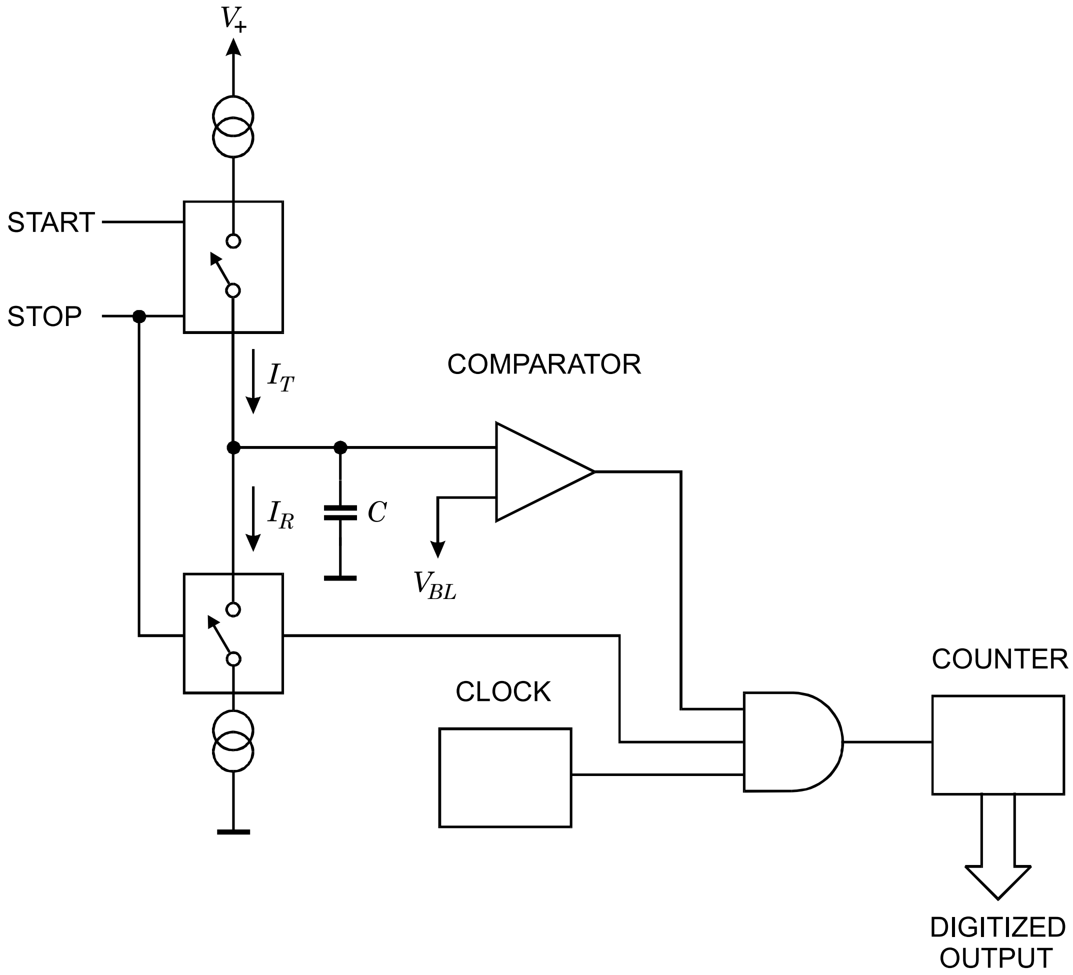
Use Wilkinson ADC with smaller discharge current to digitize voltage.

Drawbacks: No multi-hit capability

Deadtime

Advantages: High resolution (~ps)

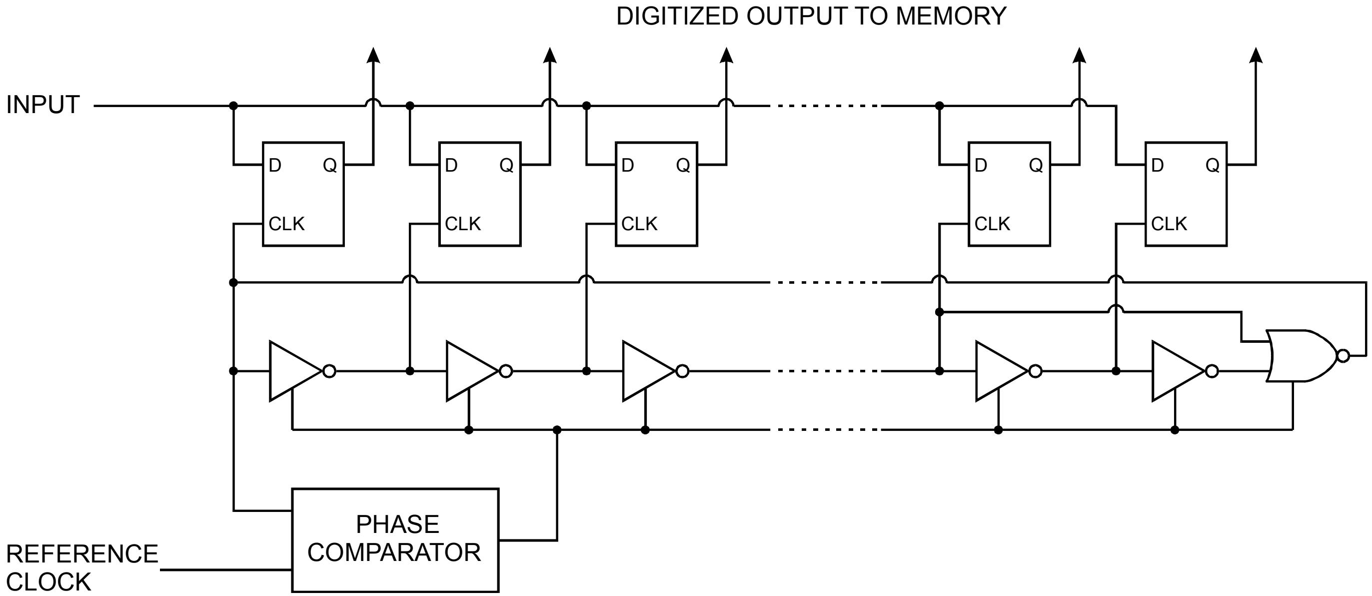
Excellent differential linearity



3. Digitizers with Clock Interpolation

Most experiments in HEP require multi-hit capability, no deadtime

Commonly used in HEP ICs for time digitization (Y. Arai, KEK)



Clock period interpolated by inverter delays (U1, U2, …).

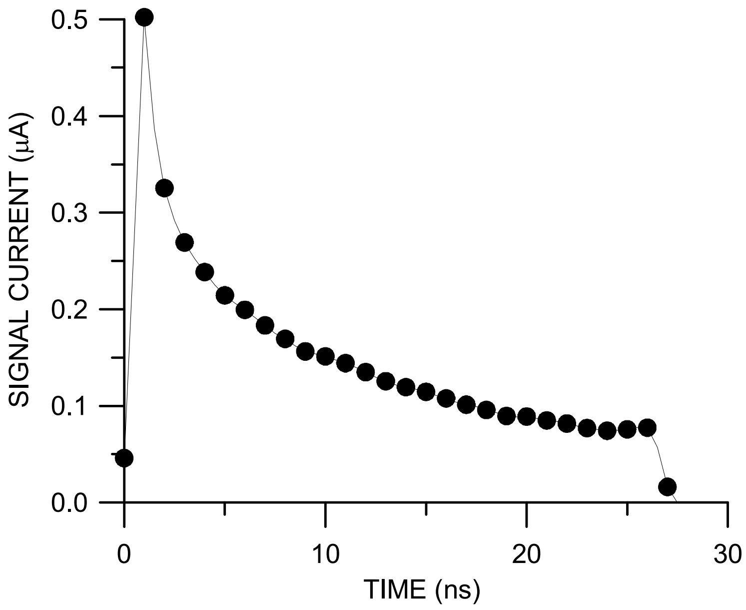
Delay can be fine-tuned by adjusting operating point of inverters. Stabilized by delay locked loop.

Devices with 250 ps resolution fabricated and tested.

see Y. Arai et al., IEEE Trans. Nucl. Sci. **NS-45/3** (1998) 735-739 and references therein.

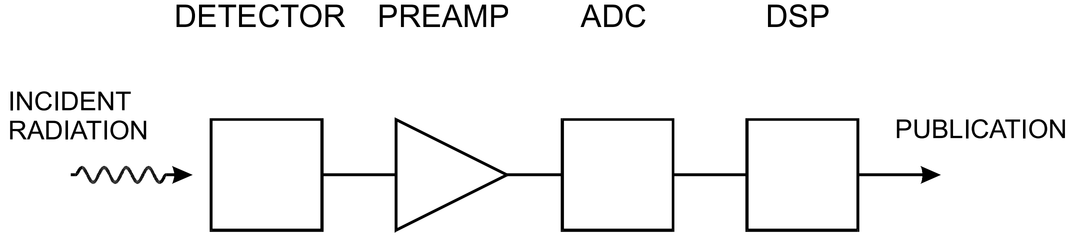
4. Digital Signal Processing

Sample detector signal with fast digitizer to reconstruct pulse:



Then use digital signal processor to perform mathematical operations for desired pulse shaping.

Block Diagram

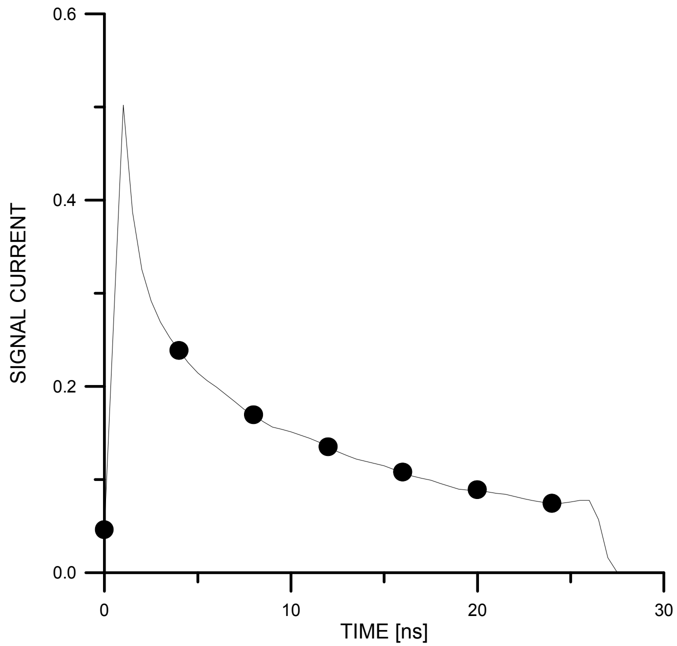


DSP allows great flexibility in implementing filtering functions

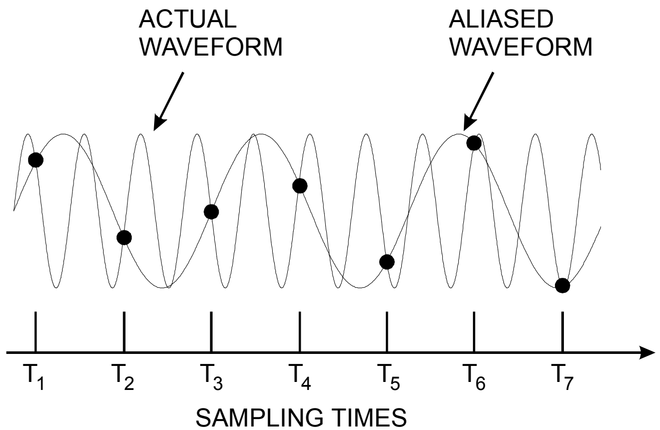
However: increased circuit complexity
increased demands on ADC, compared to traditional shaping.

Important to choose sample interval sufficiently small to capture pulse structure.

Sampling interval of 4 ns misses initial peak.



With too low a sampling rate high frequency components
will be “aliased” to lower frequencies:

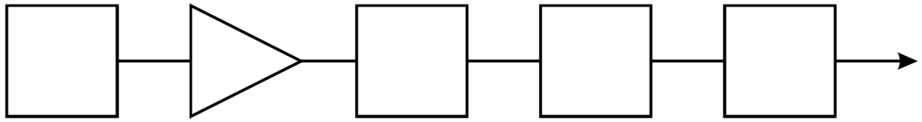


Applies to any form of sampling
(time waveform, image, ...)

Nyquist condition:

Sampling frequency > 2x highest signal frequency

⇒ Fast ADC required + Pre-Filter to limit signal bandwidth



- Dynamic range requirements for ADC may be more severe than in analog filtered system (depending on pulse shape and pre-filter).
- Digitization introduces additional noise ("quantization noise")

  If one bit corresponds to an amplitude interval Δ, the quantization noise

$$\sigma_v^2 = \int_{-\Delta/2}^{\Delta/2} \frac{v^2}{\Delta}\, dv = \frac{\Delta^2}{12}\ .$$

  (differential non-linearity introduces quasi-random noise)

- Electronics preceding ADC and front-end of ADC must exhibit same precision as analog system, i.e. baseline and other pulse-to-pulse amplitude fluctuations less than order Q_n /10, i.e. typically 10^{-4} in high-resolution systems. For 10 V FS at the ADC input this corresponds to < 1 mV.

⇒ ADC must provide high performance at short conversion times. Today this is technically feasible for some applications, e.g. detectors with moderate to long collection times (γ and x-ray detectors).

Digital Filtering

Filtering is performed by convolution: $$S_o(n) = \sum_{k=0}^{N-1} W(k) \cdot S_i(n-k)$$

$W(k)$ is a set of coefficients that describes the weighting function yielding the desired pulse shape.

A filter performing this function is called a Finite Impulse Response (FIR) filter.

This is analogous to filtering in the frequency domain:

In the frequency domain the result of filtering is determined by multiplying the responses of the individual stages:

$$G(f) = G_1(f) \cdot G_2(f)$$

where $G_1(f)$ and $G_1(f)$ are complex numbers.

The theory of Fourier transforms states that the equivalent result in the time domain is formed by convolution of the individual time responses:

$$g(t) = g_1(t) * g_2(t) \equiv \int_{-\infty}^{+\infty} g_1(\tau) \cdot g_2(t-\tau) d\tau \,,$$

analogously to the discrete sum shown above.

Benefits of digital signal processing:

- Flexibility in implementing filter functions
- Filters possible that are impractical in hardware
- Simple to change filter parameters
- Tail cancellation and pile-up rejection easily incorporated
- Adaptive filtering can be used to compensate for pulse shape variations.

Where is digital signal processing appropriate?

- Systems highly optimized for Resolution
  High counting rates
- Variable detector pulse shapes

Where is analog signal processing best (most efficient)?

- Fast shaping
- Systems not sensitive to pulse shape (fixed shaper constants)
- High density systems that require small circuit area or low power

Both types of systems require careful analog design.

Progress in fast ADCs (precision, reduced power) will expand range of DSP applications