VII. Detector Systems – Conflicts and Compromises

Conflicts

Custom integrated circuits essential for vertex detectors in HEP.

Requirements

1. low mass to reduce scattering
2. low noise
3. fast response
4. low power
5. radiation tolerance

reduction in mass $\Rightarrow$ thin detector

radiation tolerance $\Rightarrow$ thin detector

thin detector $\Rightarrow$ less signal $\Rightarrow$ lower noise required

lower noise $\Rightarrow$ increased power

fast response $\Rightarrow$ increased power

increased power $\Rightarrow$ more mass in cabling + cooling

immunity to external pickup $\Rightarrow$ shielding $\Rightarrow$ mass

+ contain costs

How to deal with these conflicting requirements?

Example: Silicon Detectors at the LHC

LHC Parameters:

Colliding proton beams
7 TeV on 7 TeV (14 TeV center of mass)
Luminosity: 10^{34} $cm^{-2}s^{-1}$
Bunch crossing frequency: 40 MHz
Interactions per bunch crossing: 23
Charged particles per unit of rapidity: 150

$\Rightarrow$ hit rate $n' = \frac{2 \cdot 10^9}{r_\perp^2} \left[\mathrm{cm^{-2}s^{-1}} \right]$, where $r_\perp$ = distance from beam axis

If the detector subtends ± 2.5 units of rapidity, the total hit rate in the detector is $3 \cdot 10^{10}$ s^{-1}

Hit rate at $r_\perp = 14$ cm: ~ 10^7 $cm^{-2}s^{-1}$

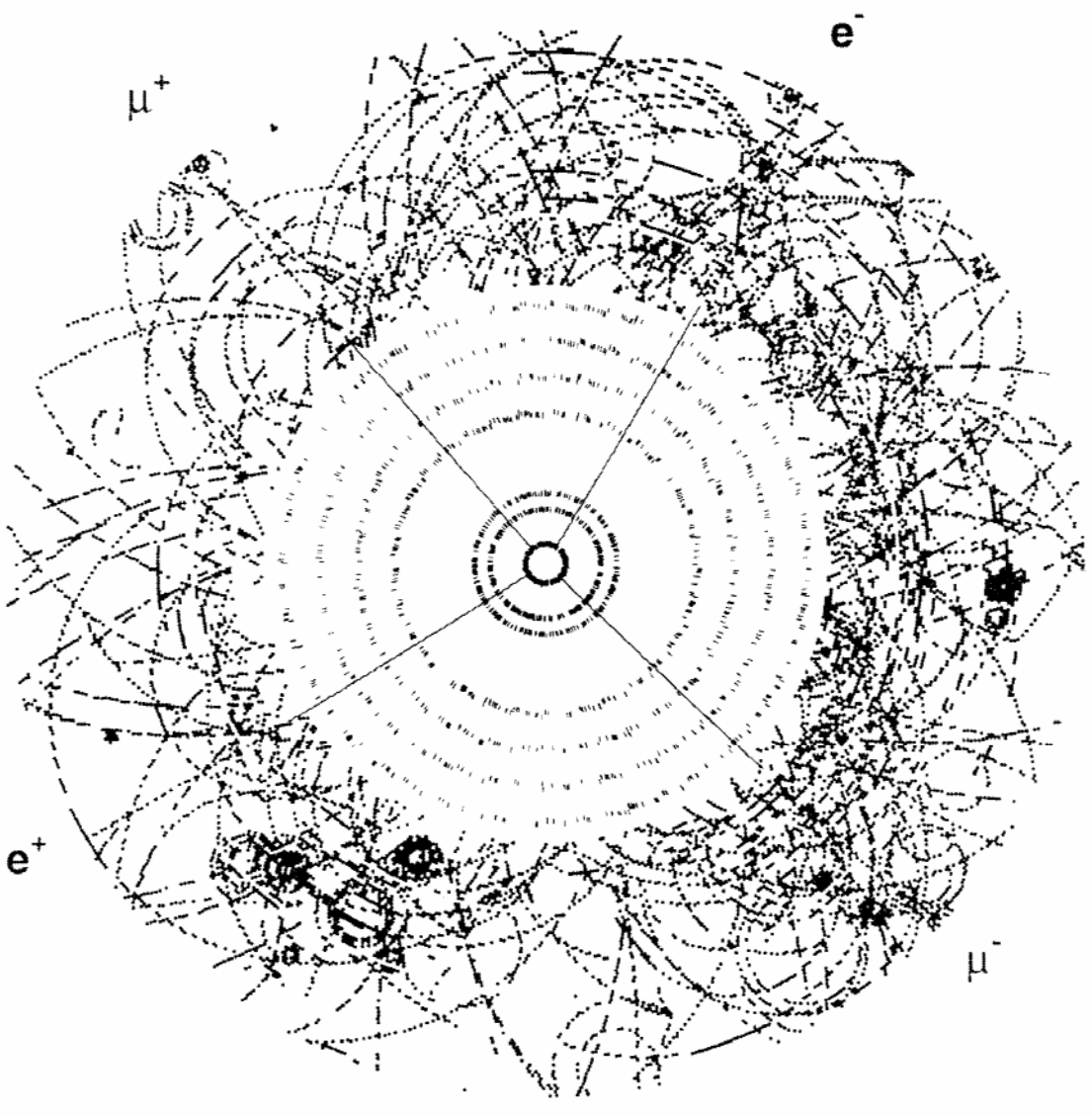
Overall detector to include
1. Vertexing for B-tagging
2. Precision tracking in magnetic field
3. Calorimetry (EM + hadronic)
4. Muon detection

"Typical Event" – Axial View

$H \rightarrow ZZ^* \rightarrow \mu^+\mu^-e^+e^-$
(m_H= 130 GeV)

Appears worse than it is

– tracks spread azimuthally, but high track density at forward angles.



Radiation Damage

Two sources of particles

a) beam collisions

b) neutron albedo from calorimeter

Fluences per year (equivalent 1 MeV neutrons)

r ~ 10 cm typ. $5 \cdot 10^{13}$ cm^{-2}

r ~ 30 cm typ. $2 \cdot 10^{13}$ cm^{-2}

Ionizing Dose per year

r ~ 10 cm 30 kGy (3 Mrad)

r ~ 30 cm 4 kGy (400 krad)

In reality, complex maps are required of the radiation flux, which is dependent on local material distribution.

How to cope with ...

- High total event rate
  a) fast electronics
     high power required for both noise and speed
  b) segmentation
     reduce rate per detector element
     for example, at r= 30 cm the hit rate in an area of $5 \cdot 10^{-2}$ cm^2 is about 10^5 s^{-1}, corresponding to an average time between hits of 10 μs.

     ⇒ longer shaping time allowable

     ⇒ lower power for given noise level

- Large number of events per crossing
  a) fast electronics (high power)
  b) segmentation
     if a detector element is sufficiently small, the probability of two tracks passing through is negligible
  c) single-bunch timing
     reduce confusion by assigning hits to specific crossing times

⇒ Segmentation is an efficient tool to cope with high rates.

With careful design, power requirements don't increase.

⇒ Fine segmentation feasible with semiconductor detectors

- "μm-scale" patterning of detectors
- monolithically integrated electronics mounted locally

Large number of front-end channels requires simple circuitry

Single bunch timing ⇒ collection times <25 ns

Radiation damage is a critical problem in semiconductor detectors:

a) detector leakage current $I_R = I_{R0} + \alpha \Phi A d$

⇒ shot noise $Q_{ni}^2 = 2 q_e I_R F_i T_S$

⇒ self-heating of detector $I_R(T) \propto T^2 e^{-E/2k_B T}$

reduce current by cooling

reduce shaping time

reduce area of detector element

b) Increase in depletion voltage (buildup of acceptor-like states ⇒ negative space charge)

⇒ thin detector

⇒ allow for operation below full depletion

⇒ less signal

Requires lower noise to maintain minimum S/N

⇒ decrease area of detector element (capacitance)

Use of a highly-developed technology, i.e. Si rather than “exotic” materials, provides performance reserves and design flexibility to cope with radiation damage.

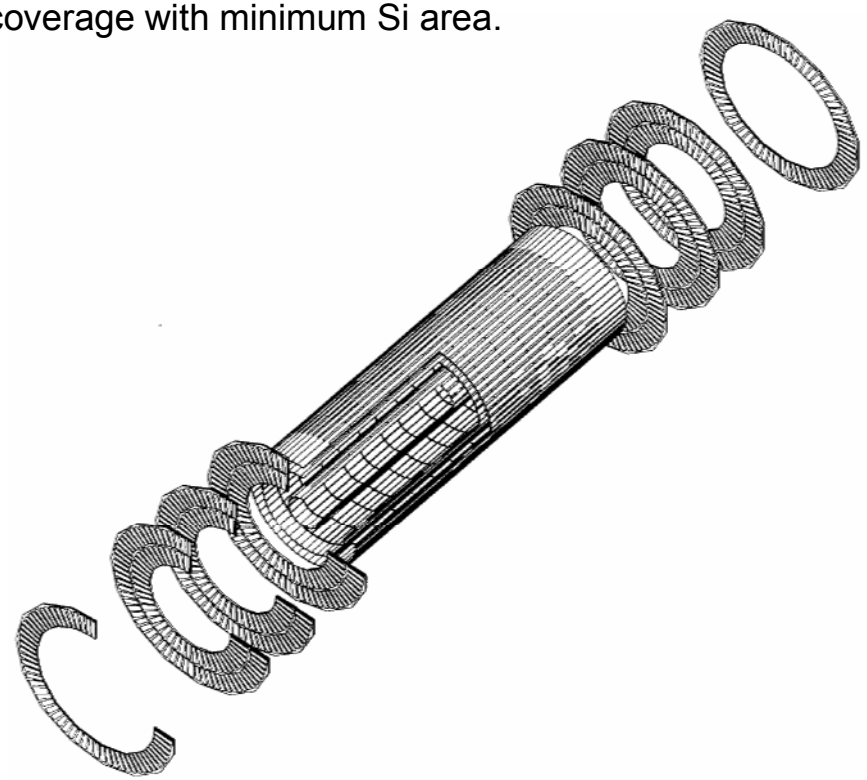
Layout

Full coverage provided by a combination of barrel and disk layers.

Coverage provided by a) barrel in central region

b) disks in forward regions

to provide maximum coverage with minimum Si area.



Pixels at small radii (4, 11, 14 cm) to cope with

- high event rate (2D non-projective structure)
- radiation damage
  small capacitance ~ 100 fF
  $\Rightarrow$ low noise $Q_n \approx 200\ e$

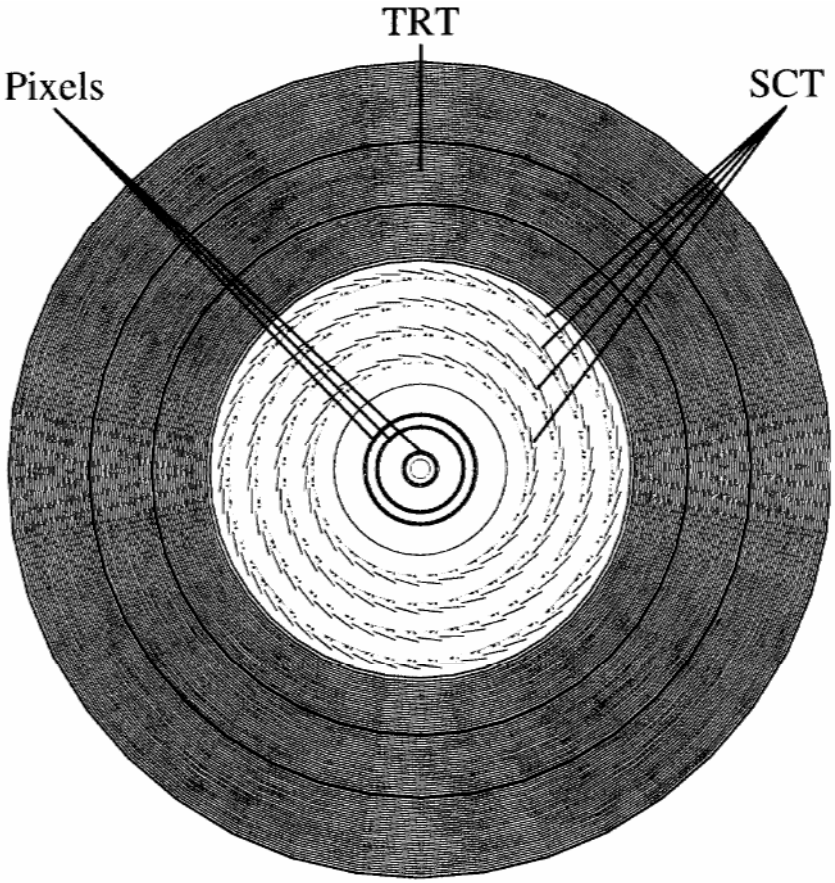
Strips at larger radii (30, 37, 45, 52 cm)
minimize material, cost

Pixels and strips provide primary pattern recognition capability

ATLAS uses straw drift chambers at outer radius (56 – 107 cm)

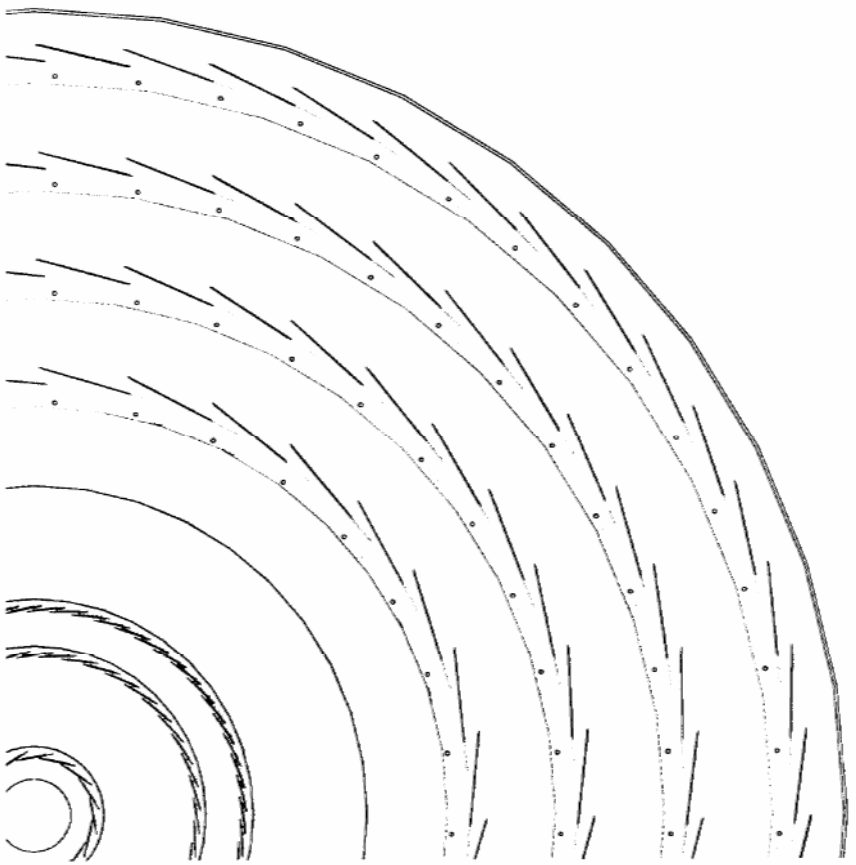
~70 layers yield 40 space points at large r and augment pattern recognition by continuous tracking (least expensive solution)

CMS uses all-silicon tracker
(210 m^2 of Si with ~10^7 channels)

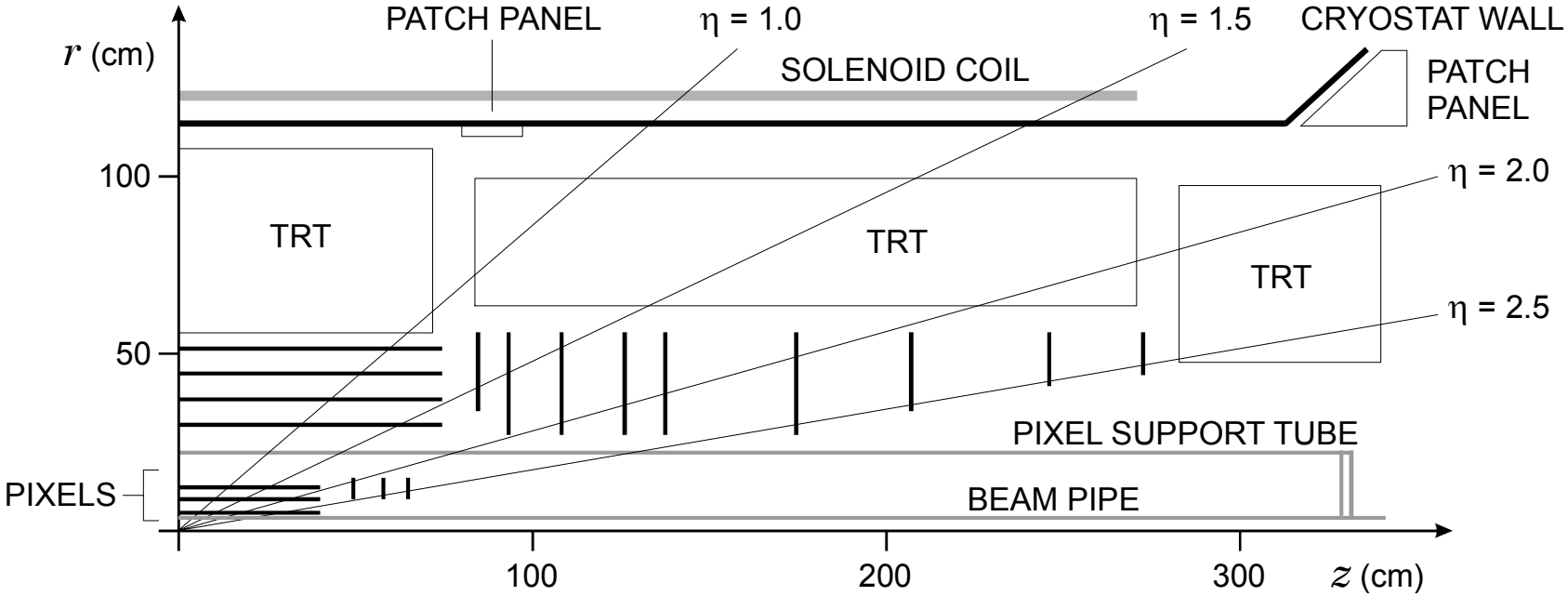


Detector modules arranged in cylindrical shells (barrels).

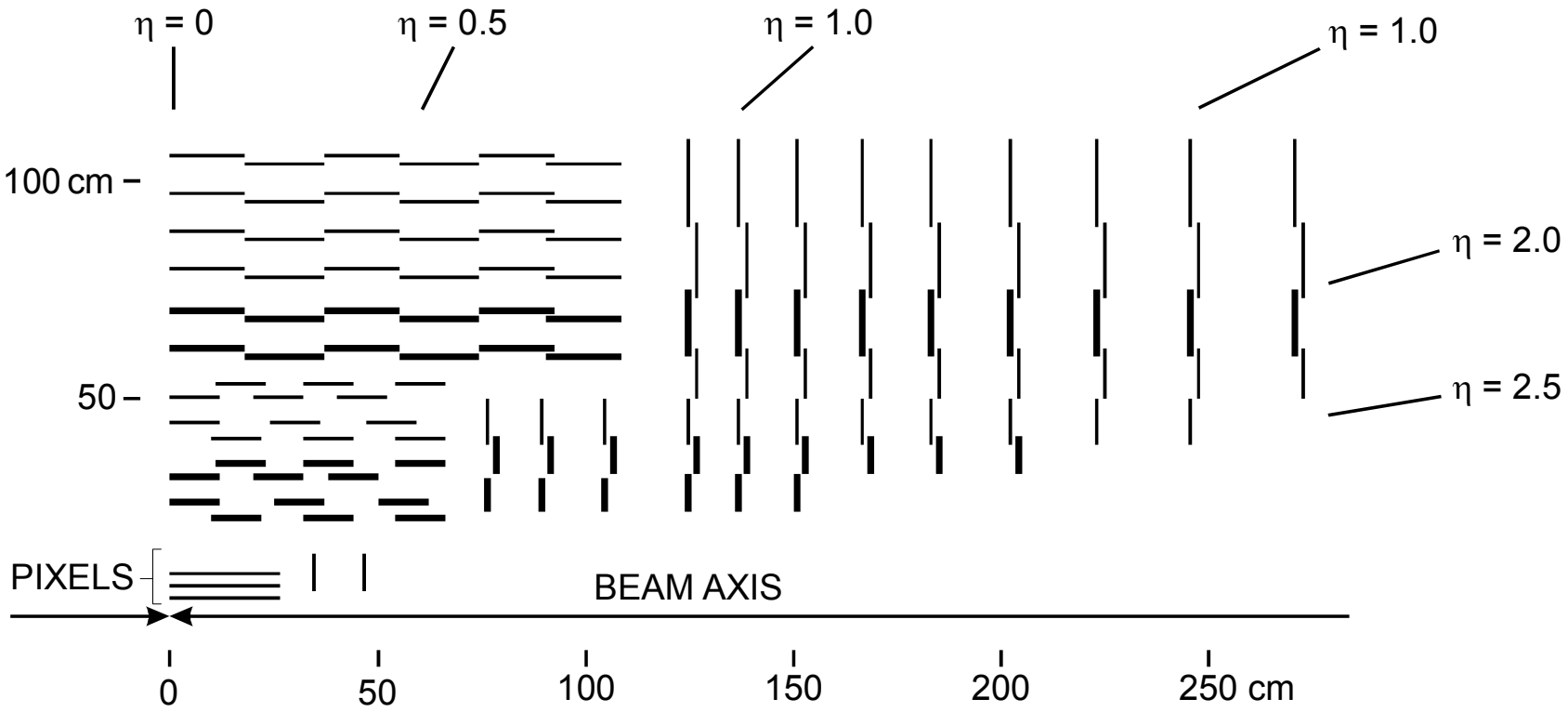
Modules are “shingled” to provide full coverage and overlap to facilitate relative position calibration.



ATLAS Silicon Tracker Layout (strips + pixels)



CMS Tracker Layout



Thick lines denote double-sided modules (back-to-back single-sided detectors).

Segmentation ⇒ Large number of data channels

Total number of channels and area (ATLAS):	Pixels	1.4×10^8 channels	2.3 m^2
	Strips	6.2×10^6 channels	61 m^2
	Straws	4.2×10^5 channels	

But, only a small fraction of these channels are struck in a given crossing

Occupancy for pixels, 50 μm x 300 μm:	4 cm Pixel Layer	4.4×10^{-4}
	11 cm Pixel Layer	0.6×10^{-4}

Occupancy for strip electrodes with 80 μm pitch, 12 cm length:

30 cm Strip Layer	6.1×10^{-3}
52 cm Strip Layer	3.4×10^{-3}

Utilize local sparsification – i.e. on-chip circuitry that recognizes the presence of a hit and only reads out those channels that are struck.

⇒ data readout rate depends on hit rate, not on segmentation

First implemented in SVX chip

S.A. Kleinfelder, W.C. Carrithers, R.P. Ely, C. Haber, F. Kirsten, and H.G. Spieler, A Flexible 128 Channel Silicon Strip Detector Instrumentation Integrated Circuit with Sparse Data Readout, IEEE Trans. Nucl. Sci. **NS-35** (1988) 171

Readout

Strips + Pixels: many channels

Essential to minimize
- power
- material (chip size, power cables, readout lines)
- cost (chip size)
- failure rate (use simple, well controlled circuitry)

ATLAS criterion is to obtain adequate position resolution, rather than the best possible

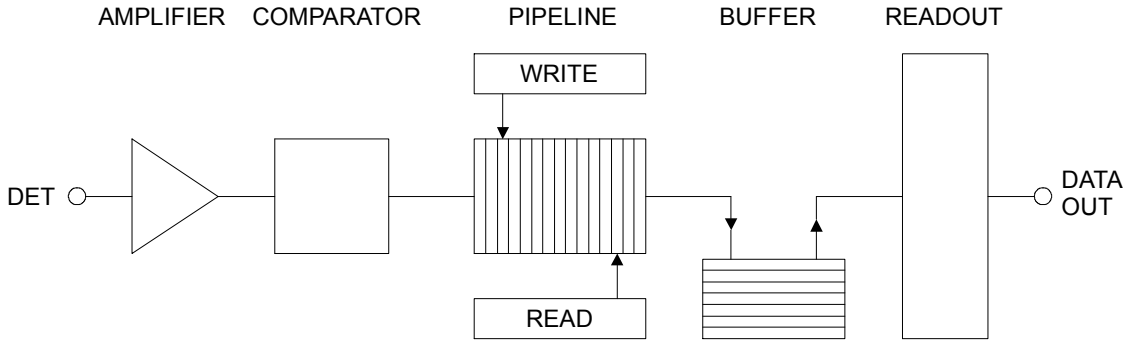
⇒ Binary Readout
- detect only presence of hits
- identify beam crossing

Architecture of ATLAS strip readout

Unlike LEP detectors …

Crossing frequency >> readout rate

Data readout must proceed simultaneously with signal detection (equivalent to DC beam)

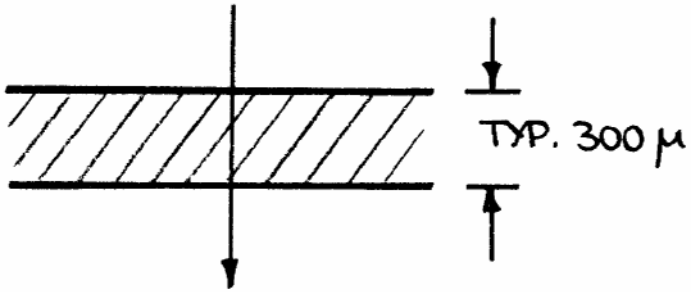


Single 128-channel BiCMOS chip (BJT + CMOS on same chip) in radiation-hard technology.

Required Signal-to-Noise Ratio

Acceptable noise level established by signal level and noise occupancy

1. Signal Level



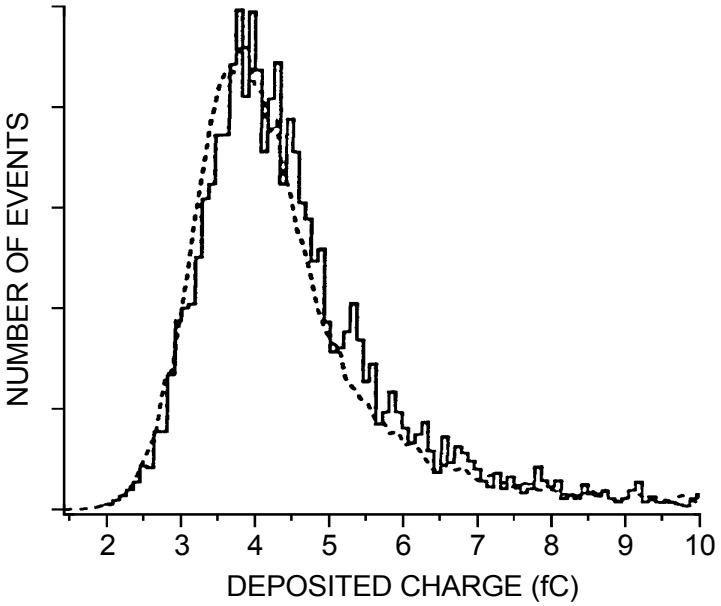
For minimum ionizing particles:

Q_s = 22000 *el* (3.5 fC)

Signals vary event-by-event according to Landau distribution

Measured Landau distribution in a 300 μm thick Si detector
(Wood et al., Univ. Oklahoma)

The Landau distribution peaks at the most probable energy loss Q_0 and extends down to about 0.5 Q_0 for 99% efficiency.



Assume that the minimum energy is $f_L Q_0$.

Tracks passing between two strips will deposit charge on both strips.
If the fraction of the signal to be detected is f_{sh}, the circuit must be sensitive signal as low as

$$Q_{\min} = f_{sh} f_L Q_0$$

2. Threshold Setting

It would be desirable to set the threshold much lower than Q_{min}, to be insensitive to threshold variations across the chip.

A lower limit is set by the need to suppress the noise rate to an acceptable level that still allows efficient pattern recognition.

As discussed in Part IV, the threshold-to-noise ratio required for a desired noise rate f_n in a system with shaping time T_S is

$$\frac{Q_T}{Q_n} = \sqrt{-2\log(4\sqrt{3} f_n T_S)}$$

Expressed in terms of occupancy P_n in a time interval Δt

$$\frac{Q_T}{Q_n} = \sqrt{-2\log\left(4\sqrt{3}_n T_S \frac{P_n}{\Delta t}\right)}$$

In the strip system the average hit occupancy is about 5 x 10^{-3} in a time interval of 25 ns. If we allow an occupancy of 10^{-3} at a shaping time of 20 ns, this corresponds to

$$Q_T / Q_n = 3.2$$

The threshold uniformity is not perfect. The relevant measure is the threshold uniformity referred to the noise level. For a threshold variation ΔQ_T, the required threshold-to-noise ratio becomes

$$\frac{Q_T}{Q_n} = \sqrt{-2\log\left(4\sqrt{3}_n T_S \frac{P_n}{\Delta t}\right)} + \frac{\Delta Q_T}{Q_n}$$

If $\Delta Q_T / Q_n = 0.5$, the required threshold-to-noise ratio becomes $Q_T / Q_n = 3.7$.

To maintain good timing, the signal must be above threshold by at least Q_n, so $Q_T / Q_n > 4.7$.

Combining the conditions for the threshold

$$\left(\frac{Q_T}{Q_n}\right)_{min} Q_n \le Q_{min} \quad \text{and signal} \qquad Q_{min} = f_{sh} f_L Q_0$$

yields the required noise level $$Q_n \le \frac{f_{sh} f_L Q_0}{(Q_T / Q_n)_{\min}}$$

If charge sharing is negligible $f_{sh} = 1$, so with $f_L = 0.5$, $Q_0 = 3.5$ fC and $(Q_T / Q_n)_{\min} = 4.7$

$$Q_n \le 0.37 \text{ fC} \quad \text{or} \quad Q_n \le 2300\ e$$

If the system is to operate with optimum position resolution, i.e. equal probability of 1- and 2-hit clusters, then $f_{sh} = 0.5$ and

$$Q_n \le 0.19 \text{ fC} \quad \text{or} \quad Q_n \le 1150\ e$$

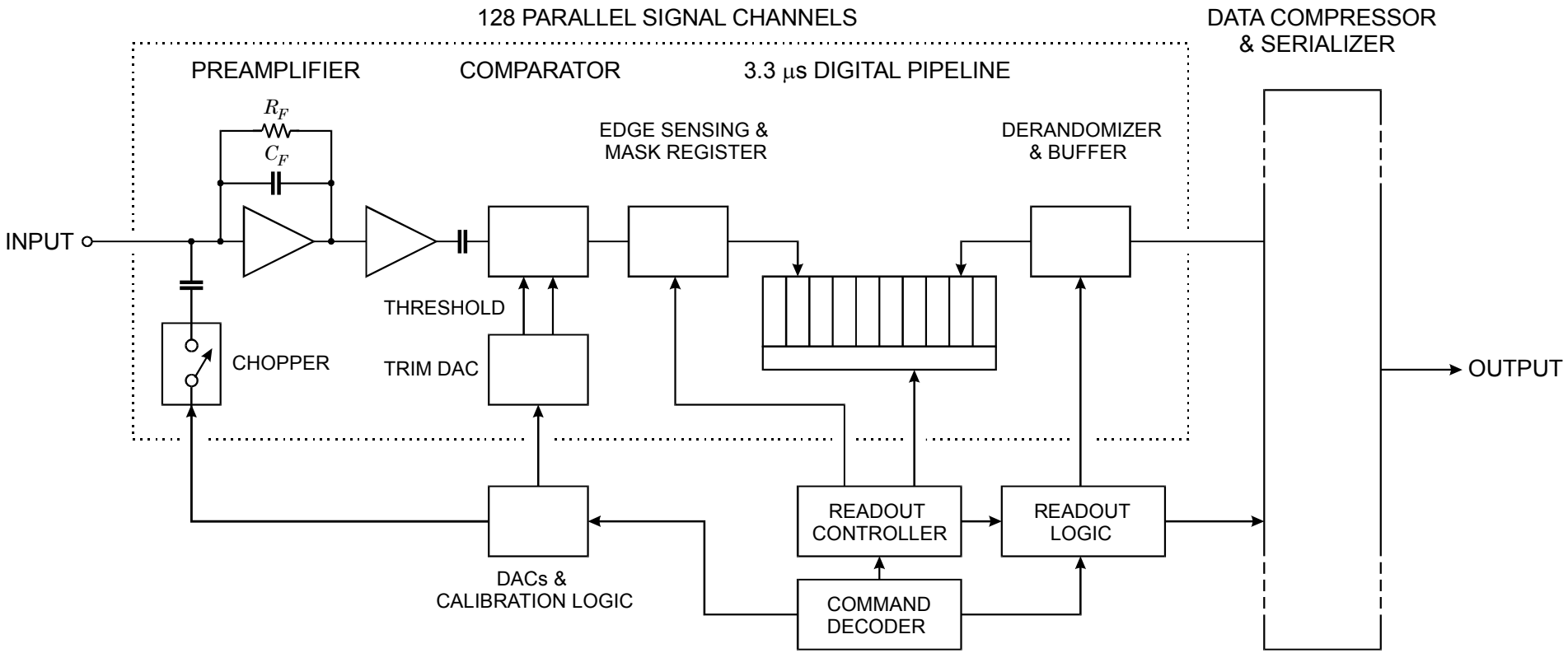
ATLAS requires $Q_n \le 1500\ e$.

ATLAS Strip Readout

ATLAS has adopted a single chip implementation (ABCD chip).

- 128 ch, bondable to 50 μm strip pitch
- bipolar transistor technology, rad-hard
  ⇒ minimum noise independent of shaping time
- peaking time: ~20 ns (equivalent CR-RC^4)
- double-pulse resolution (4 fC – 4 fC): 50 ns
- noise, timing: following slides
- 1.3 to 1.8 mW/ch (current in input transistor adjustable)
- on-chip DACs to control threshold + operating point
- Trim DACs on each channel to reduce channel-to-channel gain and threshold non-uniformity
- Readout allows defective chips to be bypassed
- Optical fiber readout with redundancy
- die size: 6.4 x 4.5 mm^2

Block Diagram of ATLAS Strip Readout



ATLAS Silicon Strip Detector Module
(mounted in fabrication fixture)

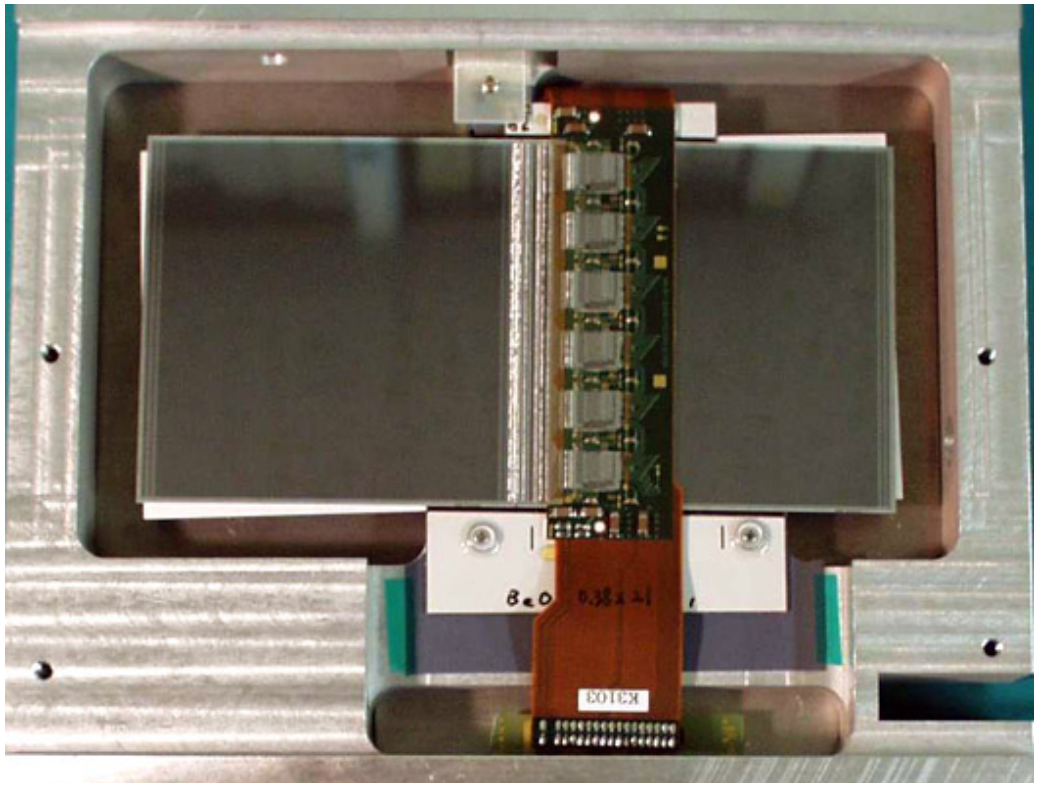
Two 6 x 6 cm^2 single-sided Si strip detectors butted edge-to-edge to form 12 cm long detector

Two 6 x 12 cm^2 detectors glued back-to-back and rotated to one another by 40 mrad to form small-angle stereo

Readout ICs – 128 channels each – mounted on detectors and connected at middle (reduce thermal noise of strip electrode resistance).

Strip pitch: 80 μm
no. of channels: 2 x 768

Binary readout with on-chip pipeline and readout sparsification



Kapton pigtail connects to local opto-module for clock, control, data transmission

Two-Dimensional Detectors

At low track densities (e.g. LEP):
Crossed strips on opposite sides of Si wafer

n readout channels $\Rightarrow$ n^2 resolution elements

Problem: ambiguities with multiple hits

n hits in acceptance field $\Rightarrow$

n x-coordinates and n y-coordinates

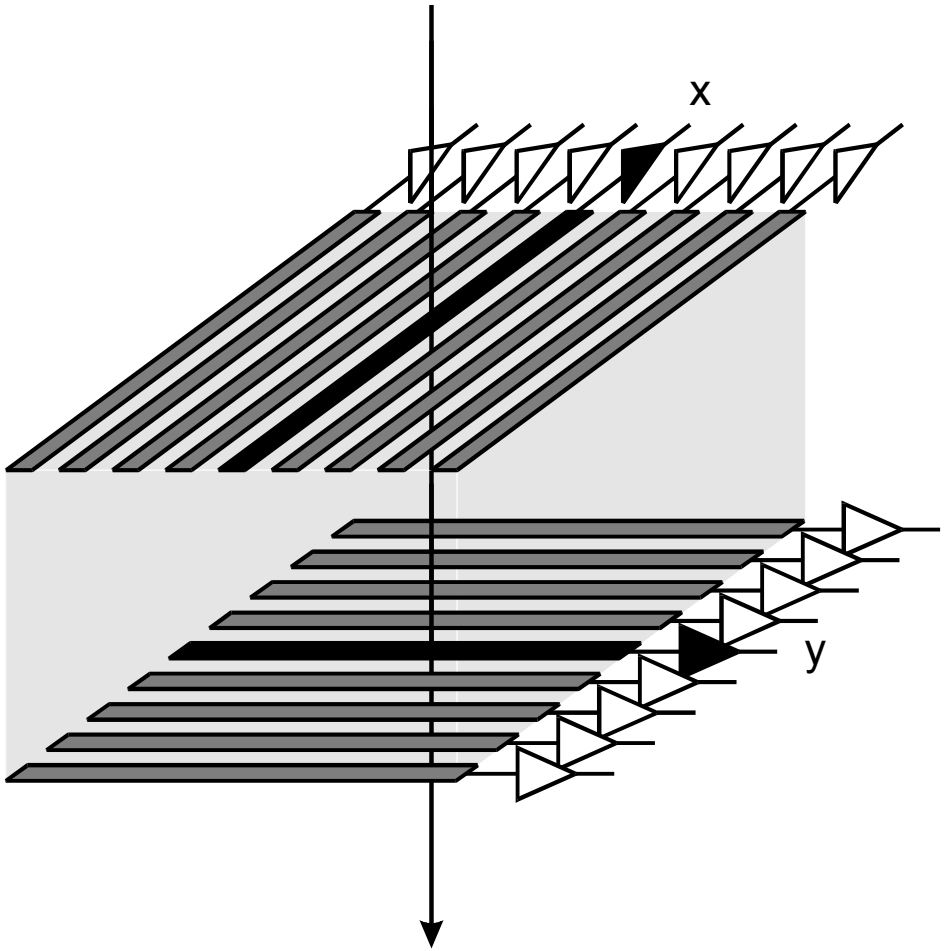
$\Rightarrow$ n^2 combinations

of which $n^2 - n$ are "ghosts"

ATLAS strips reduce ambiguities by using small angle stereo (40 mrad).

Not sufficient at small radii –

need non-projective 2D detector



Pixel Detectors with Random Access Readout

(K. Einsweiler et al.)

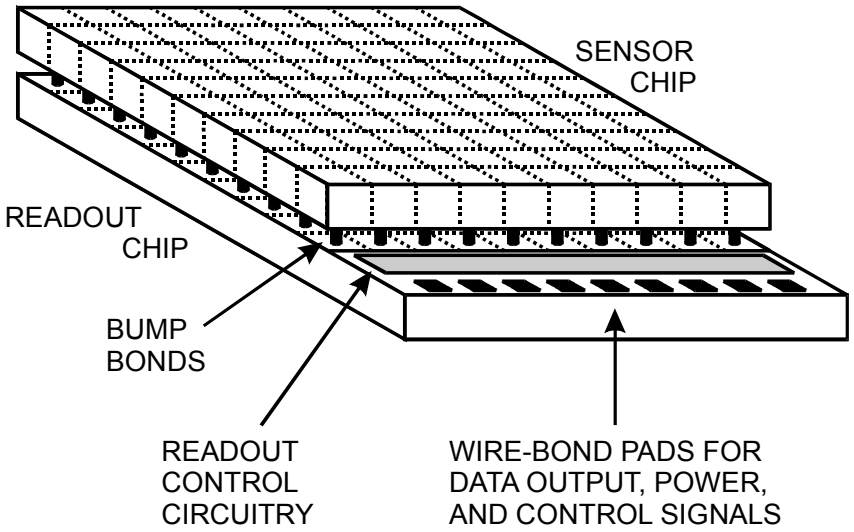
"Smart Pixels"

Quiescent state:
no clocks or switching in pixel array

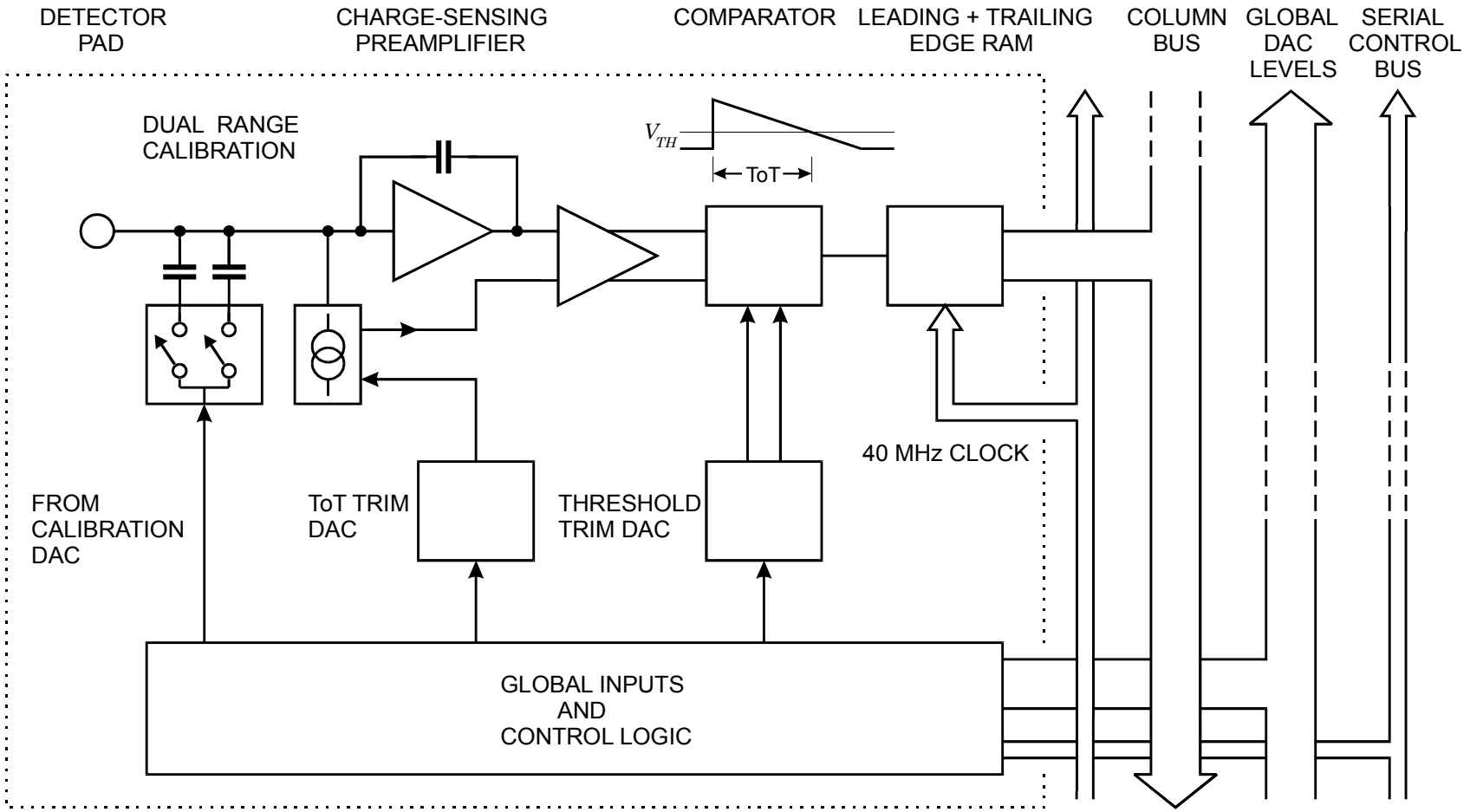
Pixel circuitry only issues signals when struck.

Struck pixels send address + time stamp
to peripheral register

On receipt of trigger selectively read out pixels.



Block Diagram of Pixel Cell



Each pixel cell includes:

Q-amplifier + shaper per pixel

threshold comparator per pixel

trim-DAC per pixel for fine adjustment of threshold

matching of comparator input transistors inadequate, so fine adjustment via trim DAC per pixel

threshold = global threshold + fine adjustment per pixel

time-over-threshold analog digitization

test pulse per pixel (dual range)

bad pixels can be masked

Pixel Readout

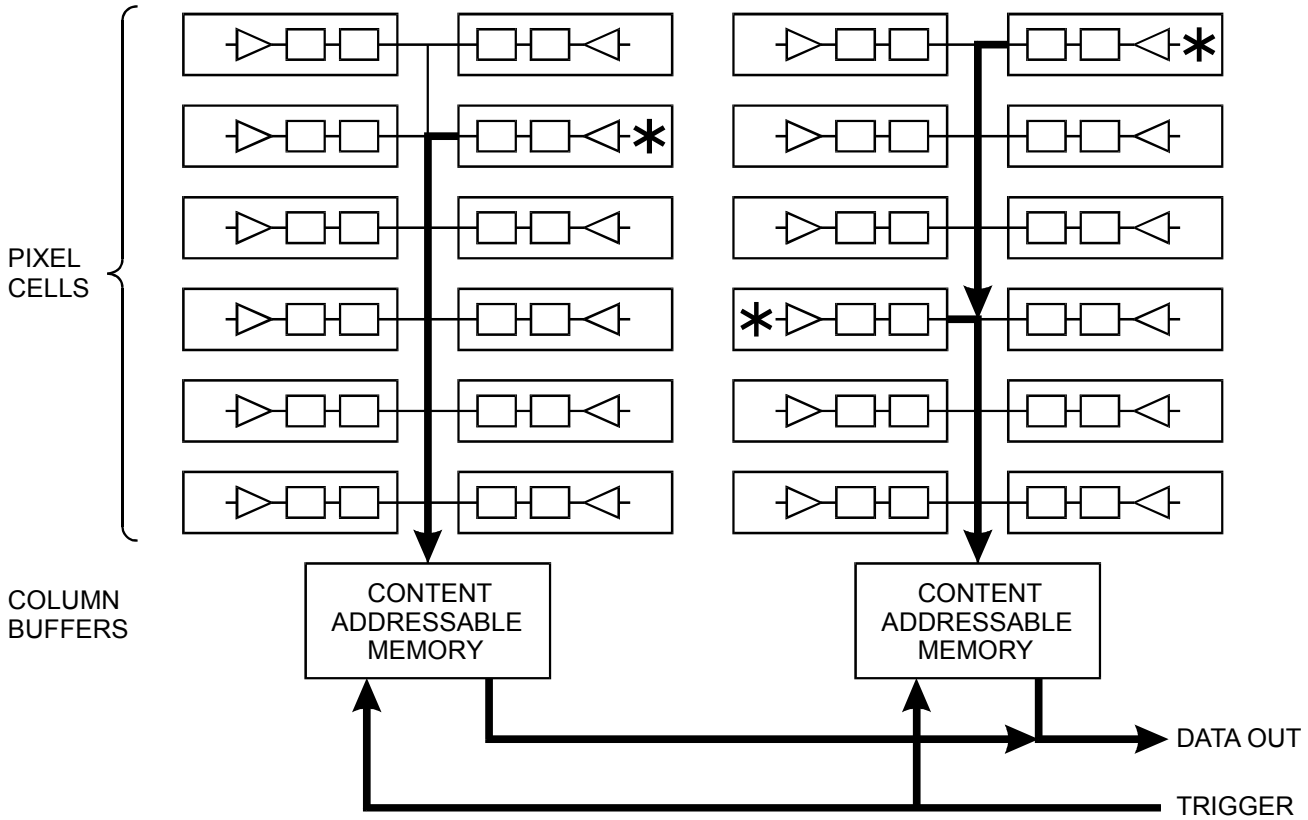
When a pixel is struck, the leading and trailing edge times are sent to the column periphery.

At the end of each column pair a content addressable memory records the hit data.

Pixels are arranged "back-to-back" to minimize coupling from digital lines to the front-end.

On-chip data transmission is differential

Upon receipt of a level 1 trigger the buffers are checked for valid events (correct crossing time) and hits from rejected beam crossings are cleared.



Pixel size: 50 μm x 400 μm

size historical:
could be 50 μm x 200 μm

Power per pixel: < 40 μW

Final chip: 18 columns x 160 pixels
(2880 pixels)

Module size: 16.4 x 60.4 mm^2

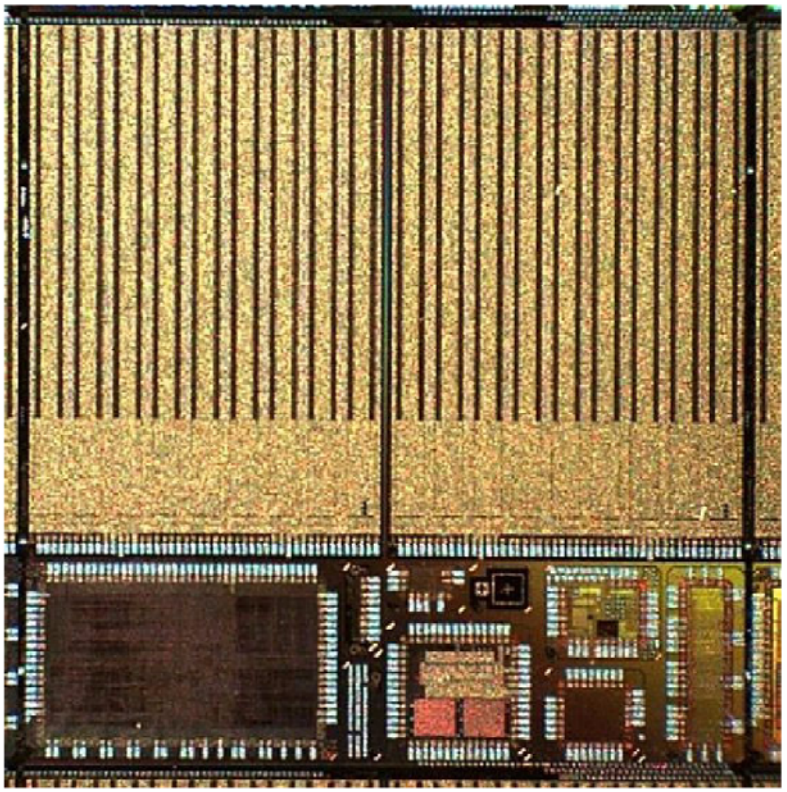
16 front-end chips per module

46080 pixels per module

fabricated in 0.25 μm CMOS

~ 3.5 $\cdot 10^6$ transistors

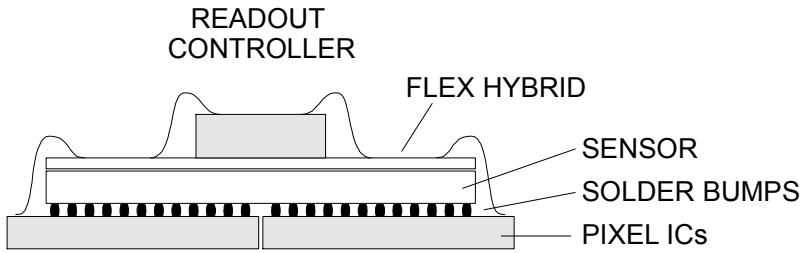
functional to > 100 Mrad



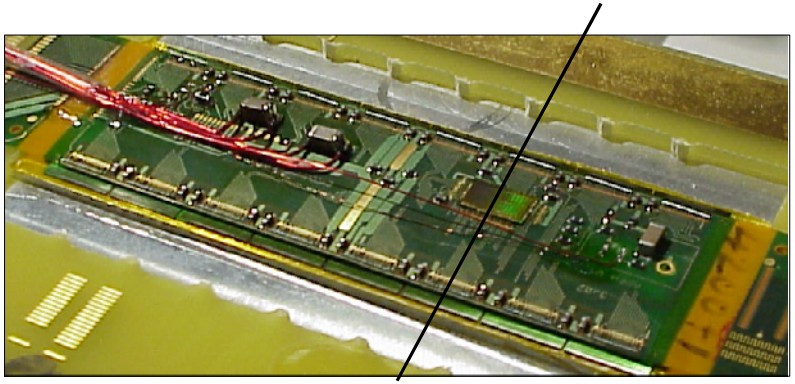
Measured noise level: ~200 e (threshold < noise)

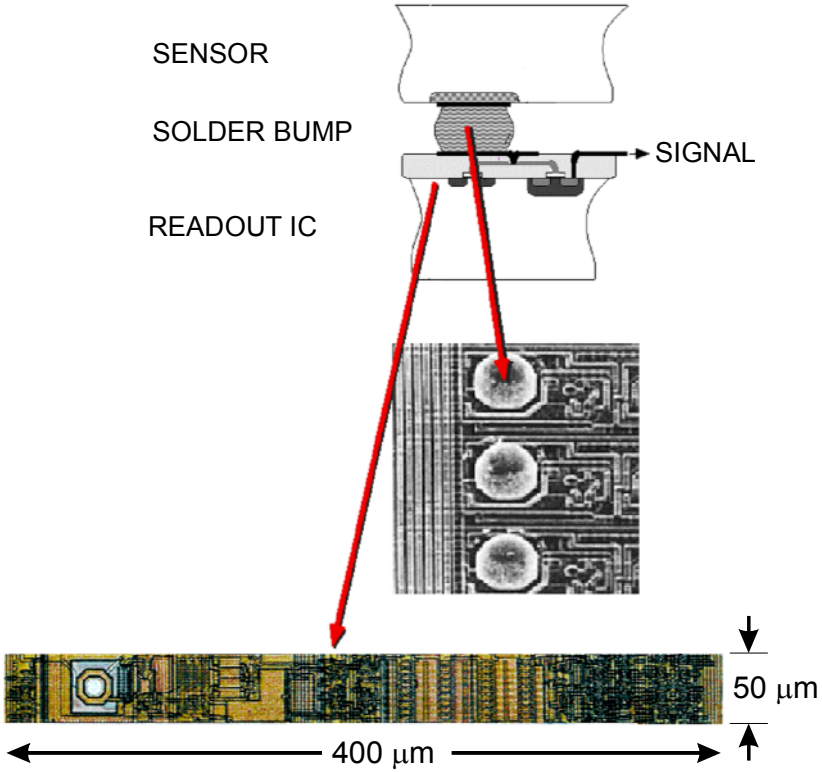
Radiation resistant to higher fluences than strips because
low noise provides large performance reserves. Tested to >100 Mrad and fluence of 10^{15} cm^{-2}.

ATLAS Pixel Module



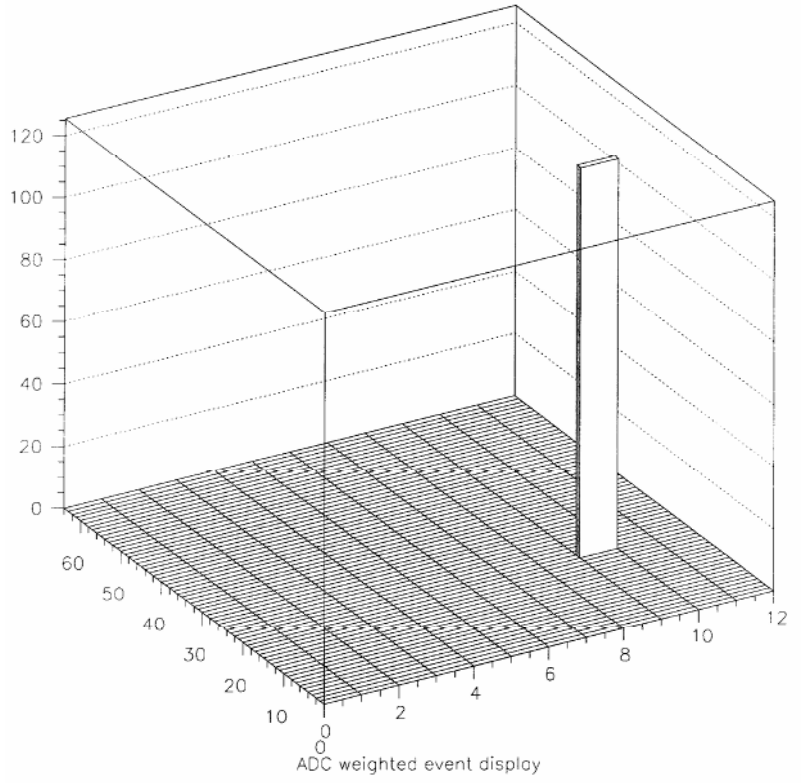
SCHEMATIC CROSS SECTION (THROUGH HERE)



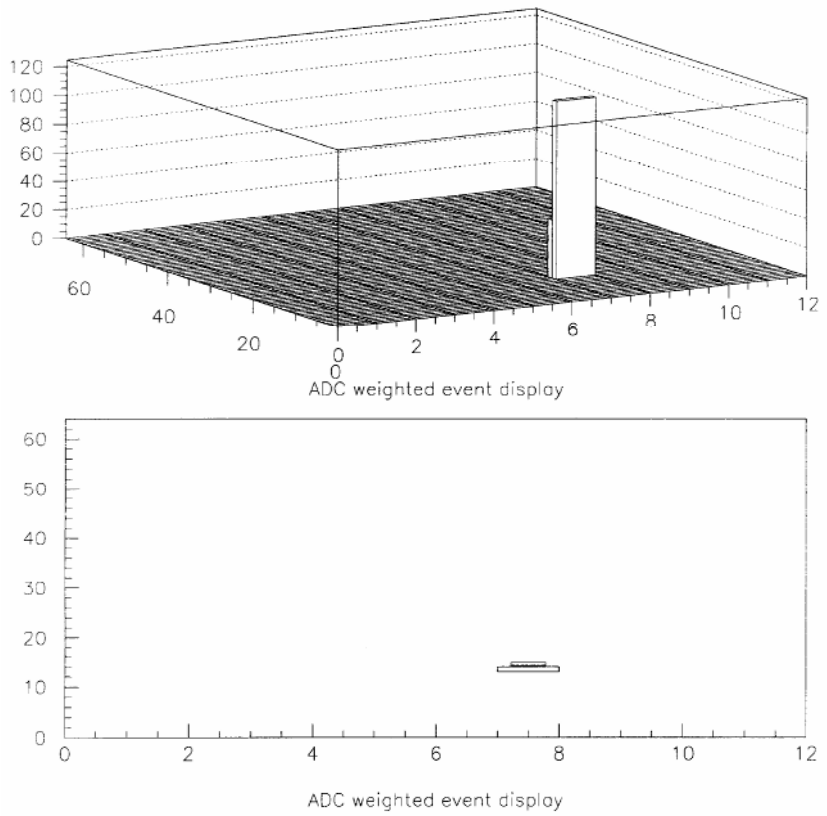


Test Beam Results

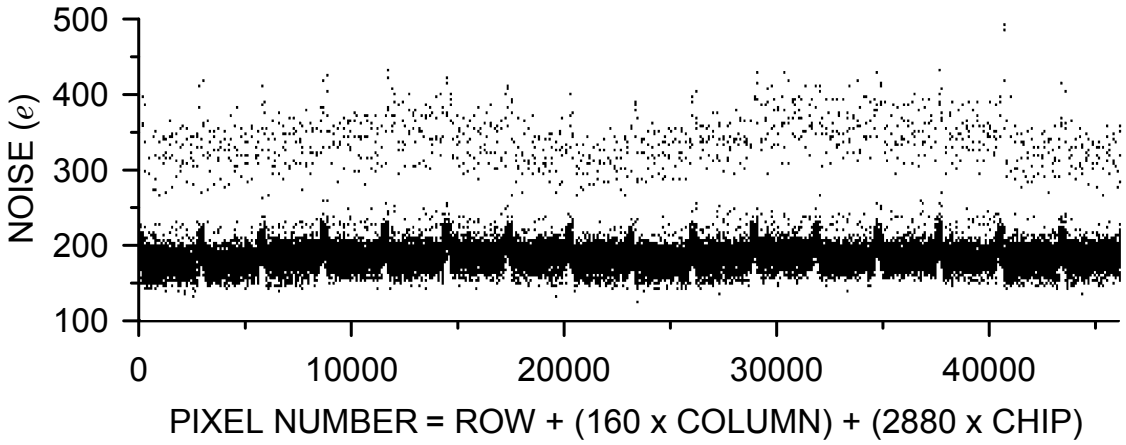
Track through single pixel



Charge sharing



Measured Noise Distribution in a Module



Three groups are visible:

1. nominal pixels
2. extended pixels that bridge columns between ICs (“spikes” every 2880 pixels)
3. ganged pixels to bridge rows between ICs (upper band)

After trim-DAC correction the threshold the threshold spread is $\sigma = 60\ e$, < noise level.

Advantages of Pixels at LHC

2D segmentation

⇒ Pattern recognition at small radii

Low capacitance

⇒ high S/N

⇒ allows degradation of both detector signal and electronic noise due to radiation damage

small detector elements

⇒ detector bias current per element still small after radiation damage

Drawback:

Engineering complexity order of magnitude greater than previous chips

Question: What is the ultimate limit of radiation resistance?

Current design could survive 5 – 10 years at nominal LHC luminosity.

Luminosity upgrade? Much R&D necessary.